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REAL-TIME FOCAL-PLANE ARRAY IMAGE PROCESSOR

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ABSTRACT

A focal-plane-array chip designed for real-time, general-purpose, image preprocessing is reported. A 48 X 48 pixel detector array and a 24 X 24 processing element processor array are monolithically integrated on the chip. The analog, charge-coupled device-based VLSI chip operates in the charge domain and has sensing, storing, and computing capabilities. It captures the image data and performs local neighborhood operations. The processor array is digitally programmable and uses a single-instruction, multiple-data parallel architecture. Various image preprocessing tasks such as level shifting, gain adjustment, thresholding, smoothing, sharpening, and edge detection can be implemented and A/D conversion can be performed prior to output. Frame-to-frame operations such as motion detection and tracking can be implemented as well. The chip was fabricated with a double-poly, double-metal process in a commercial CCD foundry. The prediction of the performance is based on numerical analysis and experimental results of testing a prototype charge-coupled computer. Operating at a modest clock frequency of 25 MHz, the chip is projected to achieve an internal throughput as high as 576 Mops with a 54 dB dynamic range (9-bit equivalent accuracy). The simulation of an edge detection algorithm implemented by the chip is presented. The power dissipation is estimated to be 20 mW and the total size of the 59-pad chip is 9.4 X 9.4 mm^2.

1. INTRODUCTION

Strong civilian and military interests in real-time vision have developed over the years because of its many important and critical applications. Autonomous vehicles, an example of a system that utilizes real-time vision, can be employed in underwater inspection, space exploration, agriculture, transportation, and defense. Automated on-line inspection and measurement are rapidly finding their way into industry. Space surveillance and remote sensing are other examples of systems that utilize real-time vision. Defense real-time vision systems include munition and guidance. Depending on the application, the vision system must be lightweight and/or low-power, while retaining the high throughput necessary for achieving real-time operation.

Image preprocessing tasks can be performed using local neighborhood operations on image array picture elements (pixels). Generally, these preprocessing functions consume the greatest portion of time required by the vision process. In the course of effecting the preprocessing tasks, each pixel may undergo as many as 100 to 500 simple arithmetic operations per frame. The frame rate may range from 1 Hz in low speed systems, to 100 Hz in systems operating on a par with human vision, to 1000 to 10,000 Hz in high performance systems. The number of operations required in a 100 Hz frame rate system with a modest array size of 100 X 100 pixels could easily exceed hundreds of millions of operations per sec (Mops). Advances in very high speed integrated circuits (VHSIC) may allow serial computing systems to achieve such high throughput, but a parallel computing approach can be used to alleviate the performance requirements. Unfortunately, massively parallel computing systems are presently incompatible with the portability needs of a mobile system. Furthermore, the advantages of massively parallel systems are often offset by the problem of loading and unloading the parallel data from a serial data stream at sufficiently high data rates.

Since the image data arrives in a parallel manner and is transduced to an electrical form in parallel, it seems natural to perform spatially parallel image preprocessing on the image plane itself (as proposed by Fossum[1], Joseph et al.[2], and Beaudet[3].) It also seems natural to integrate the sensing and computing circuits on the focal plane. Charge-coupled device (CCD) structures are well-suited for such a system. Because of its analog nature, the image data can be compactly represented in the charge domain, requiring a single electrode for storage. The image data are refreshed at the frame rate; therefore the dynamic nature of CCD signal representation is generally not a concern. Charge-transfer devices already have established themselves as a technology of choice for image data readout. The difficulty lies in the design of the charge-domain circuits.

In order to recognize the significance of integrating sensing and computing circuits on the focal plane, the following example is considered. A 128 X 128 pixel imager operates at a frame rate of 50 Hz. Each pixel may undergo as many as 250 operations per frame to implement an image processing task. The throughput requirement to process the data collected by the imager in real-time is approximately 200 Mops. A charge-coupled analog processing element (PE) operating at a modest frequency of 25 MHz yields a throughput of 1 Mops, assuming that 25 cycles are required per operation. A 14 X 14 PE array is needed to meet the 200 Mops requirement, ignoring multiplexing time. The above array sizes could be generalized to N X N pixels and M X M PEs. The size of the pixel subarray supported by each PE is n X n, where n = N/M. The integration of the two arrays, the detector array and the processor array, is the crucial step toward achieving real-time focal-plane image processing.

In this paper, the approach of integrating sensing and computing circuits is explored. A CCD focal plane array analog image processor is reported. The IRET (in real-time) chip is designed for real-time, general-purpose, image preprocessing. Testing of IRET is currently underway. The estimated performance and simulation of IRET is described as well.

2. SENSING AND COMPUTING CIRCUITS INTEGRATION

The integration of the sensing and processing arrays can be classified as either planar or vertical. In planar integration, two-dimensional integrated circuit technology is used to integrate the two arrays on the same chip (the same plane). Two different architectures may be adopted. The first one is the unit cell array architecture. In this architecture, an array of unit cells is formed. Each unit cell is an integration of a set of computing circuits (the PE) and a subarray of detectors which is supported by that PE. In the example given above, the unit cell array size is 14 X 14 and the detector subarray size is 9 X 9. The proximity of the computing and sensing circuits makes the otherwise difficult task of communicating between them an easy one. On the other hand, the drawback of such an approach is the low fill factor, that is; the area devoted to sensing within each unit cell is small compared to the total area of the unit cell. Calculations show, using available design rules, that a unit cell can be designed with a uniform detector pitch of 55 um and a detector size of 22 um. The resulting fill factor is 16 % and the estimated size of the chip is 8 X 8 mm^2.

The second architecture of planar integration is the two-array architecture. In this architecture, the two arrays are spatially separated from each other. Each array is designed independently making it easier to optimize the design of each. The fill factor could be close to 100 %. The routing of the signal from the sensing array to the processing array could be realized employing different schemes. A direct approach is to output the signal from the imager in the conventional serial fashion. A circuit is designed to reconstruct n X n blocks from the serial data stream and each block is transmitted to the corresponding PE in the processor array. The shortcoming of this scheme is the serial section which may impede the speed performance of the parallel architecture. A parallel approach can be used to route the signal from the imager to the processor. In this approach, an output line is used for each n X n block of the imager and the M X M output lines are fed to the M X M PEs. The fill factor may fall slightly under unity but the parallel nature of the architecture is preserved. Other schemes in which the number of lines connecting the sensor array to the processor array ranges from 1 to M X M could be used as a tradeoff between the fill factor and the parallelism of the architecture.

In vertical integration, three-dimensional integrated circuit technology is used to vertically integrate the sensor and processor arrays. Four different versions of vertical integration can be considered. The first one employs the flip-chip solder-bump technology (Goldman and Totta[4]). Each array is designed and fabricated on a single chip. The two chips, face-to-face, are vertically connected using an array of solder-bumps. The fill factor of the back-illuminated imager chip could be close to 100 %. The routing of signal from the imager chip to the processor chip is achieved through the vertical connections between them. The maturity of the area array solder-bump technology makes it a first choice for vertical integration.

The second version of vertical integration utilizes the amorphous silicon photodetection technology. A two-dimensional integrated circuit containing the processor array is fabricated. Then, an amorphous silicon sensor array is deposited (ion cluster beam deposition) on the top of the processor array (Kataoka[5]). Because of its cost effectiveness and capability of handling large area sensors, the amorphous silicon photodetection technology is a strong competitor of the solder-bump technology for vertical integration.

The third version of vertical integration uses the Z-plane technology. While approaching manufacturing viability, the Z-plane technology provides a unique way for integrating the sensor and processor arrays (Carson[6]). Thinned two-dimensional integrated circuits, each containing a row of PEs, are stacked to form the processor array. The imager array is perpendicularly connected to the stack so that each row of the imager array is attached to one of the chips in the stack (one row of the processor array.) Each pixel in the imager array is connected to a corresponding PE in the processor array. In this version of vertical integration, each PE supports one pixel (n=1); therefore the frame rate range for real-time vision is wide (several KHz). The real-estate available for each PE is relatively large and more complex computing circuitry can be added. Different application areas of the Z-plane technology for focal-plane image processing are discussed by Kemeny et al.[7]. The drawback of this technology is the lack of direct communications between PEs in neighboring rows (stacked chips.) This can only be achieved through the use of a backplane which is cumbersome and can consume significant power.

The fourth and final version of vertical integration employs the three-dimensional monolithic integrated circuit technology, the ultimate realization of vertical integration. Stacked active integrated circut layers can be used to achieve the vertical integration of the two arrays. The top layer contains the sensor array while the processor array is contained on a second layer or partitioned on two or more layers. The three-layer strucuture reported by Nishimura et al.[8] demonstrated the feasibility of vertically integrating the two arrays using this technology. Though complex and expensive, three-dimensional monolithic integrated circuit technology represnts the future of sensor and processor arrays integration.

3. IRET ARCHITECTURE AND DESIGN

IRET was conceived as a vehicle for testing the integrability of the sensing and processing arrays. Planar integration of the two arrays was adopted in IRET because three-dimensional integrated circuit technology essential for vertical integration was not available to us. The unit cell array architecture was the choice for IRET first generation because it is less complex than the two-array architecture. A detector array of 48 X 48 pixels and a processor array of 24 X 24 PEs are integrated monolithically on IRET. The unit cell of the integrated array consists of one PE and a subarray of 2 X 2 pixels. The PE is a set of various computing and communicating elements, and each PE supports 4 pixels. Figure 1 is a photograph of IRET bonded in a 68-pin package.

IRET is desiged with a single-instruction, multiple-data (SIMD) architecture. In this approach, each PE in the array carries out the same instruction, but on a different piece of data depending on the position of the cell in the array. Each PE does not have to be ultra-fast to achieve real-time processing as in the case of serial approaches. A modest clock frequency of 25 MHz and a modest array size of 24 X 24 PEs achieve a total throughput as high as 576 Mops.

The size of the detector subarray supported by each PE, n, is very significant. Increasing n enhances the fill factor and improves the spatial resolution of the imager. However, n is limited by the throughput of each PE. A realistic estimate of 1 Mops/PE throughput yields n = 9 with 250 operations per pixel per frame at 50 frames per second. The unit cell size is estimated to be 495 X 495 um^2 with a detector pitch of 55 um and a detector area of 22 X 22 um^2. The choice of n = 2 reduced the complexity of the design and yielded a unit cell size of 360 X 360 um^2 with a detector pitch of 180 um and a detector area of 22 X 22 um^2.

CCD technology is the heart of this architecture (Fossum[9,10]). The capabilities of CCDs enabled integrating sensing, computing, and storing elements on the same chip. Despite the different functional orientations of these elements, they are all analog and operate in the charge domain. There is no need for A/D or D/A conversion between different stages. CCDs are digitally programmable through the sequence of applied clock waveforms and so is the array processor. The compactness of CCDs was essential in achieving high density layout. The dynamic nature of CCDs is a key factor in the estimated low power dissipation. Details of the several tradeoff issues that were involved in the design of IRET can be found elsewhere (Eid and Fossum[11,12]).

In addition to the conventional way of transfering charge in the semiconductor channel (channel charge transfer), IRET employs the unconventional way of transfering charge over wires connecting two or more semiconductor channels (wire charge transfer) described by Fossum[13]. This provides flexible layout and achieves the compactness requirement dictated by parallel architecture.

The unit cell has sensing, computing, and communicating circuits, and a central bus. As shown in Fig. 2, all circuits in the unit cell are connected to the bus through switches. Communication between different elements in the same unit cell is achieved through the bus by applying a sequence of clock signals to the switches. Communication between different unit cells is achieved through a transceiver. The transceiver is a CCD circuit that can be programmed to transceive signals to or from a horizontal, vertical, or diagonal nearest neighbor unit cell. A serial-parallel CCD shift register is used to stack signals coming from the detector subarray. This bidirectional stack can be used for storing purposes.

The unit cell has four CCD computing circuits. Two of them are differencers similar to that reported by Fossum and Barker[14]. One differencer is gated by a magnitude comparator similar to that reported by Colbeth et al.[15]. The fourth computing circuit in the unit cell is a splitter similar to that reported by Bencuya and Steckl[16]. Figure 3 is a microphotograph of the unit cell.

4. PERFORMANCE

The basic functions of IRET are: capture of the image data, performing local neighborhood operations, and output of a serial data stream that represents the processed image. It performs the local neighborhood operations using basic arithmetic functions such as addition, subtraction, splitting, and magnitude comparison. It also uses conditional addition and subtraction; that is, addition and subtraction conditioned on magnitude comparison.

IRET is a general-purpose image processor. It can be programmed to implement various image preprocessing tasks[12], each being a convolution of the image data array with a kernel. The kernel has a central element and some surrounding ones. The shape and size of the kernel may differ depending on the nature of the task. IRET can be programmed to perform A/D conversion on the processed data prior to output.

IRET was fabricated with a double-polysilicon, double-metal process by a commercial CCD foundry service. Preliminary tests of IRET showed that there is a short circuit in the unit cell between the bus and power lines due to a design rule violation. Efforts are being made to clear the gap between these two lines. Meanwhile, testing of different shift registers yielded a channel charge transfer efficiency of 0.99999 and a wire charge transfer efficiency of 0.999 at target frequencies[13]. The prediction of the performance of IRET is based on numerical analysis and experimental results of testing a prototype charge-coupled computer[9].

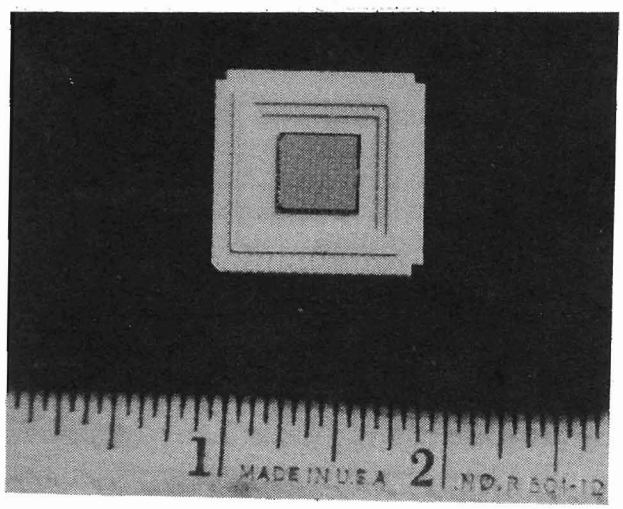

Fig. 1. IRET chip (9.4 X 9.4 mm^2) in 68-pin package.

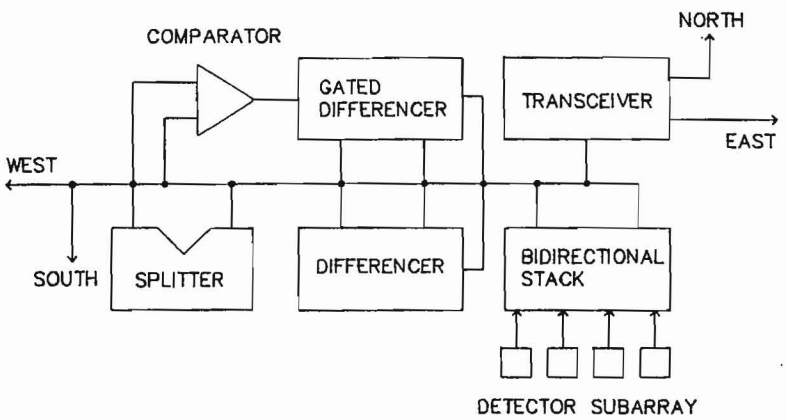

Fig. 2. Block diagram of the unit cell.

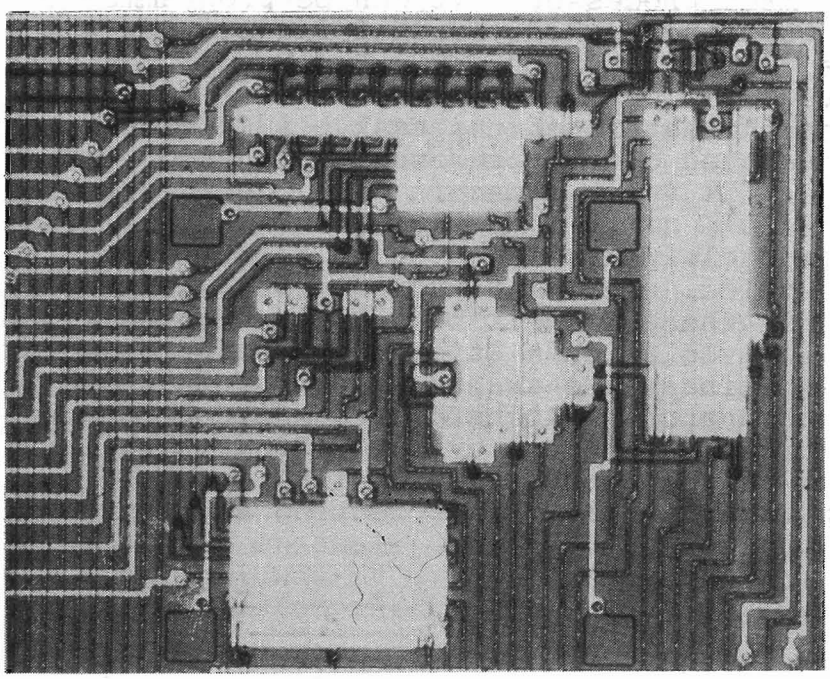

Fig. 3. IRET unit cell (360 X 360 um^2).

The assumption that the CCDs will operate with 40 nsec characteristic clock widths is a conservative one. At most, 25 clock cycles are needed to execute any of the basic operations. Thus, the throughput of each PE is estimated to be 1 Mops and the total throughput of the 24 X 24 PE array is estimated to be 576 Mops. On the average, 250 operations per pixel per frame are needed to implement an image preprocessing task. Since each PE supports 4 pixels, 1000 operations per PE per frame are needed. The 1 Mops per PE throughput yields a frame rate of 1000 frames per sec. This frame rate is high and covers a wide range of applications. However, IRET will not operate at this high frame rate because of the relatively limited handling capability of the output shift register and amplifier. IRET will operate at a nominal frame rate of 50 frames per sec, so the nominal clock frequency will be 1.25 MHz. The total throughput at the nominal point of operation will be 28.8 Mops.

The detectors are expected to have a 60 dB dynamic range (10-bit equivalent accuracy.) At 250 operations per pixel per frame, the total noise associated with computation is of the same order of magnitude as the noise associated with sensing the image data (shot noise.) Thus, the overall dynamic range is estimated to be 54 dB (9-bit equivalent accuracy).

The CCDs on IRET are designed to have a maximum signal of one million electrons per pixel. On the average, they are estimated to consume 0.8 pJ per transfer at 10 V clock voltage swing. At the nominal operating point, the clock frequency is 1.25 MHz and the 24 X 24 PEs are expected to dissipate 1 mW. At full operation, the clock frequency is 25 MHz and total power dissipation is estimated to be 20 mW.

5. SIMULATION

A simulator for IRET was developed. The IRET simulator takes into account the inefficiency of channel charge transfer and wire charge transfer. It considers the different sources of noise: input shot noise of the sensor array and thermal noise due to charge transfer, charge resetting, and charge filling and spilling. It also takes into account the inaccuracy of the different computing circuits due to misalignment of fabrication masks, thermal noise, and any other source. An edge detection algorithm was implemented on the simulator. The channel and the wire charge transfer efficiencies were assumed to be 0.9999 and 0.99, respectively. The inaccuracy of the computing circuits was assumed to be 1%.

Figure 4 shows the edge as detected by IRET simulator versus the original image. The same edge detection algorithm was implemented by a digital computer. Figure 5 shows the edge as detected by IRET simulator versus that by the digital computer. The simulated performance of IRET is comparable to that of the digital computer. The inaccuracy of the computing circuits was exaggerated to 10 % and the edge detection algorithm was once again implemented by IRET simulator. Figure 6 shows the edge as detected by the simulator with 1 % computing circuits inaccuracy versus 10 % computing circuits inaccuracy. There is no visually perceived difference between the two cases, though the display unit and/or the halftoning routine may have limited the visual perception of any numerical difference.

6. CONCLUSIONS

The design of a CCD focal plane array analog image processor chip (IRET) has been described. The capabilities of IRET to implement various real-time image preprocessing tasks have been theoretically demonstrated and its performance has been predicted. An IRET simulator was developed and the simulated performance shows good promise. IRET features high throughput, programmability, compactness, and low power dissipation.

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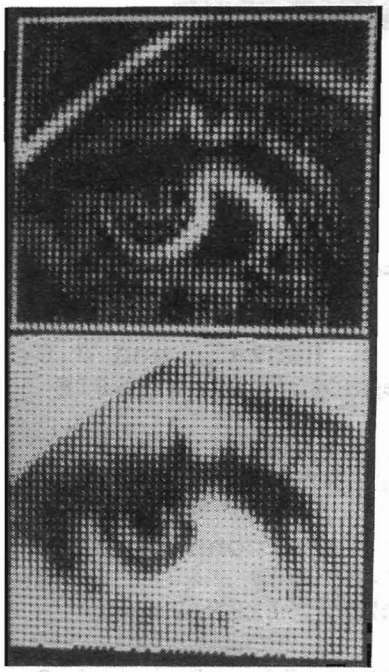

Fig. 4. IRET edge (top) and original image (bottom).

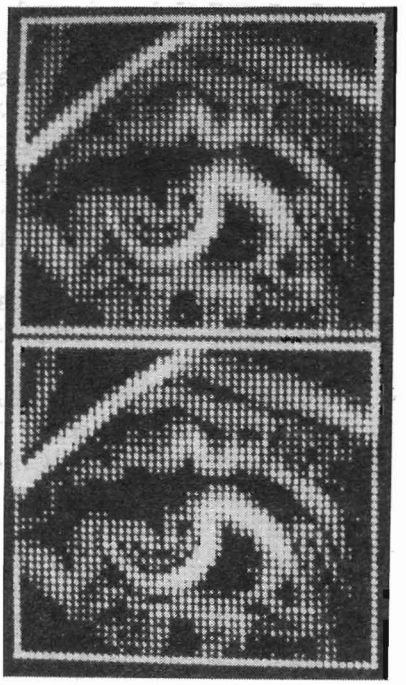

Fig. 5. IRET edge (top) and digital edge (bottom).

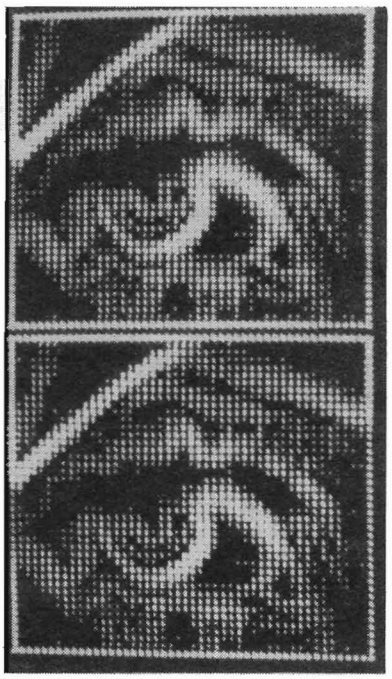

Fig. 6. IRET edge (top) and large error edge (bottom).

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