Wire Transfer of Charge Packets Using a CCD-BBD Structure for Charge-Domain Signal Processing

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Abstract—**A structure for the virtual transfer of charge packets across metal wires is described theoretically and is experimentally verified. The structure is a hybrid of charge-coupled device (CCD) and bucket-brigade device (BBD) elements and permits the topological crossing of charge-domain signals in low power signal processing circuits. A test vehicle consisting of 8-, 32-, and 96-stage delay lines of various geometries implemented in a double-poly, double-metal foundry process was used to characterize the wire-transfer operation. Transfer efficiency ranging between 0.998 and 0.999 was obtained for surface n-channel devices with clock cycle times in the range from 40 ns to 0.3 ms. Transfer efficiency as high as 0.9999 was obtained for buried n-channel devices. Good agreement is found between experiment and simulation.**

I. Introduction

CHARGE-coupled devices (CCD's) are presently the dominant technology for both image acquisition and readout. In the readout operation, charge is passed from under one electrode to the next by applying a sequence of clocking voltages. The charge transfer efficiency (CTE) is defined as the fraction of charge successfully transferred and in state-of-the-art CCD's, the CTE, η, can be as high as 0.99999 or more. In a large imager (e.g., 512 × 512), each packet must undergo several thousand transfers before reaching the output amplifier. In this case, the net transfer efficiency for a charge packet is η^m, where m is the total number of transfers. For example, if $m = 3000$ and $\eta = 0.99999$, the net transfer efficiency is of the other of 0.97. Such signal degradation is generally acceptable.

Recently there has been interest in placing analog image processing circuitry on the same chip as the imager [1]–[7]. Such circuitry might be used for noise reduction, spatial smoothing, nonuniformity correction, filtering, convolution, nonlinear local neighborhood operations, or image compression. The circuitry must be low-power and consume relatively little real estate. The use of the analog charge domain through CCD technology promises to fulfill these needs. However, since the CCD transfers charge between adjacent electrodes, the intimate, contiguous integration of circuitry makes the topological crossing of signal paths nearly impossible to achieve. Thus signal processing with CCD's has largely been confined to temporal filtering operations, with the CCD functioning primarily as an analog delay line.

A closely related technology to the CCD is the bucket-brigade device (BBD) [8]. While the BBD stores charge under MOS electrodes, it differs from the CCD in several respects. In the BBD, electrodes overlap heavily doped regions of the semiconductor with the signal charge residing as majority carriers at the semiconductor surface. In the CCD, charge is stored as minority carriers at the surface of a moderately doped substrate (surface channel) or as majority carriers in a mostly depleted region buried below the surface (buried channel). A further distinction between the two technologies is that in the BBD charge is virtually transferred using a heavily doped junction between the electrodes (i.e., approximately the same number of carriers is recovered from the junction), while in the CCD charge is physically transported through an otherwise depleted region by the use of fringing fields between very closely spaced electrodes. The transfer efficiency of the BBD is generally much poorer than a CCD (typically 0.997) and also generally operates at lower frequencies (under 1 MHz).

In this paper, a hybrid structure combining features of the BBD and the CCD is described. Termed a wire-transfer structure, its main purpose is to permit topological crossing of charge-domain signals across metallic wires at high frequencies (0.1–100 MHz). Although the CTE of the wire-transfer structure is less than that of the CCD, the total number of transfers in the signal processing circuitry is much less than that occurring in image readout. Thus the total signal degradation occurring in the signal processing circuitry can be less than that occurring during image readout.

II. Wire-Transfer Operation

A. Concept

The wire-transfer structure is shown schematically in Fig. 1. For this discussion, a surface n-channel configuration is used, but p-channel or buried-channel configurations could be used as well. Two short CCD registers are shown connected by an output diode junction, a metal wire interconnect, and an input diode junction. It should be noted that unlike a BBD, no overlap between the heavily doped regions and the electrodes is desired. Initially, in the left (or output) register is a charge packet Q_{sig} that is to be transferred to the right (or input) register. Note that the initial voltage on the junctions corresponds to the channel under the first electrode of the input register ($B1$) being just pinched off. The charge is transferred in the usual CCD fashion from well $P2$ to $P3$ and charge sharing causes the voltage to rise on the junctions. The voltage on electrode $P3$ is then ramped down at a constant rate causing the ejection of the charge packet from under it. The channel under $B1$ and $B2$ is charged and a nearly constant current flows into the receiving well under electrode $P1$.

When the voltage on electrode $P3$ is fully ramped so that no charge remains under it, the junctions discharge into the input register with a time constant dictated by the total capacitance of the junctions and wiring. Ideally, the discharge ceases when

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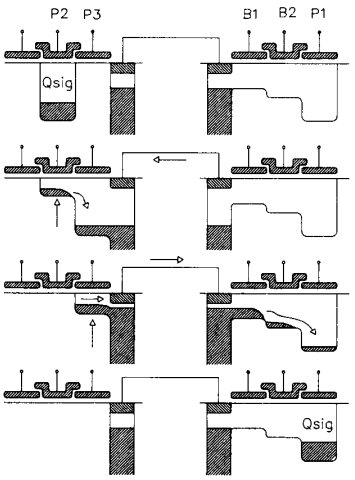


Fig. 1. Illustration of the wire-transfer process.

the channel under $B1$ returns to the pinchoff condition. Since the junction voltage is now equal to its initial value, it follows that the total charge injected into the input register is Q_{sig}. It is noted that the charge transfer is virtual, that is, approximately the same number of charge carriers is injected into the receiving well as were output from under $P3$.

The maximum operating speed of the wire-transfer process can be designed to match that of the CCD. If the length and width of the barrier electrode ($B1$) have approximately the same dimensions as the electrodes in the CCD channel, electrode $B1$ need not be biased much above the MOS threshold voltage to accommodate the current source, provided the transition rate of the electrode $P3$ bias does not exceed the characteristic CCD transfer time. Electrode $B2$ is similarly designed. As in two-phase CCD's, low channel potentials under these electrodes increases bucket capacity of the structure. Buried-channel configurations may be expected to operate faster than surface-channel configurations reflecting the general speed difference between surface-channel and buried-channel CCD's [9]. Thus, wire-transfer in GaAs buried-channel (MESFET) CCD's might be expected to operate at over 1 GHz.

B. Analysis

The analysis of the wire-transfer structure is similar to that of the BBD [8]–[13]. It is assumed that the structure is designed and operated such that the major effects which limit the CTE are subthreshold current conduction under electrode $B1$ and charge trapping in the vicinity of the junctions. While it will be shown that the former is readily relieved through the use of a bias charge (or "fat zero"), traps in the junction regions are a function of fabrication and not easily rectified.

The approach taken is to examine the subthreshold current flowing from the diode junctions and consequent change in junction voltage. Coupled with the node capacitance, the subthreshold current is shown to result in a trapping and emission process which degrades CTE. To begin the analysis, the current flowing under electrode $B1$ is modeled as [14]

$$I = I_s e^{-\beta V_n} \tag{1}$$

where V_n is the voltage of the junction relative to the junction pinchoff voltage, β is defined as q/kT, and I_s is the characteristic current of the subthreshold conduction process scaling with the gate length of $B1$. Counter to intuition, analysis will reveal I_s to be a noncritical parameter. With the total capacitance of the junctions, interconnect wiring and other parasitics lumped as a constant C_n, it is readily shown that if the node (i.e., junction) is initially at voltage V_{n0}, then after time t, the node discharges and the voltage rises to voltage $V_n(t)$ given by

$$V_n(t) = 1/\beta \ln [\beta I_s t/C_n + e^{\beta V_{n0}}]. \tag{2}$$

In wire transfer, the node is initially biased by the current source I_{cs} generated by the ramping of electrode $P3$ such that

$$I_{cs} = C_b \, dV/dt \tag{3}$$

where C_b is the bucket capacitance under $P3$. Since the node voltage induced by this current source is generally small (approximately 100 mV), the subthreshold current expression of (1) can be approximately applied. Thus the node voltage under current source bias V_{ncs} is simply

$$V_{ncs} = 1/\beta \ln [I_s/I_{cs}] \tag{4}$$

and is generally negative (relative to the pinchoff condition). In wire transfer, the discharge process continues for some characteristic clock cycle period T_c so that combining (4) and (2) yields

$$V_n(T_c) - V_{ncs} = 1/\beta \ln [\beta I_{cs} T_c/C_n + 1]. \tag{5}$$

If m cycles pass without additional charge transferred into the node, the node voltage continues to rise to approximately

$$V_n(mT_c) - V_{ncs} = 1/\beta \ln [\beta I_{cs} m T_c/C_n + 1] \tag{6}$$

which is independent of the characteristic subthreshold current I_s. If the charge packet is now transferred into this discharged node, the charge retained by the node Q_{loss} after the packet is transferred out is determined simply by the node capacitance and the difference in voltage between (5) and (6). It is noted that the quantity $I_{cs}T_c$ is of the order of the CCD bucket capacity. Thus the quantity $\beta I_{cs} T_c/C_n$ is the ratio of the bucket capacity to a charge packet equal to C_n/β. Since this ratio is much greater than unity, one obtains the surprisingly simple result

$$Q_{\text{loss}} \simeq C_n/\beta \ln [m] \tag{7}$$

which is proportional to the node capacitance and temperature. This result emphasizes the requirement for small node capacitances if losses are to be minimized.

A shift register configuration using the wire-transfer structure is shown in Fig. 2. Although it is unlikely that such a shift register would be used in an actual signal processor, it is a useful vehicle for exploring the characteristics of the wire-transfer operation. Each shift register stage has five electrodes. Electrode $B1$ functions as the primary barrier gate for setting the quiescent node voltage and is typically dc biased. Electrode $B2$ serves to screen the potential under electrode $B1$ from any variation induced by charge residing under electrode $P1$ and is generally clocked. Electrodes $B1$ and $B2$ resemble the tetrode arrangement for the BBD [15]–[17]. Electrodes $P1$, $P2$, and $P3$ are the CCD-like portion of the wire-transfer structure. Operation of each stage proceeds like that illustrated in Fig. 1, with the addition of a CCD transfer cycle between electrode $P1$ and $P2$.

The transfer of charge from electrode P_{k-1} to electrode $P1_k$ is now considered. Let the charge under electrode $P1_{k-1}$ be Q_{k-1} and the voltage on the node between $P1_{k-1}$ and $P1_k$ be

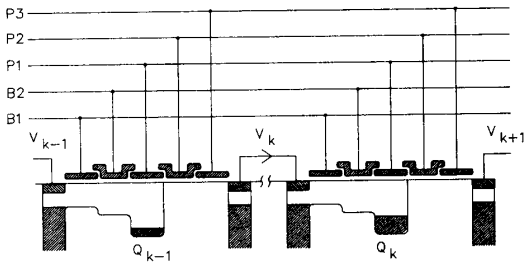


Fig. 2. Schematic cross section of a shift register implemented using the wire-transfer structure. Gate $B1$ is typically dc-biased at a low level, while gate $B2$ is clocked approximately 1 V higher than the bias on $B1$. Gates $P1$–$P3$ are clocked as conventional 3-phase CCD's.

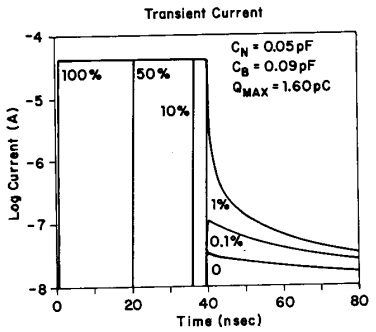


Fig. 3. Calculated current transient under the $B1$ electrode for various charge packet sizes.

V_k. The charge is first transferred to under $P3$ with CCD CTE of η_c so that the charge under electrode $P3_{k-1}$ is $\eta_c^2 Q_{k-1}$. The charge is then wire-transferred to under electrode $P1_k$ in two steps. First, the bucket under $P3_{k-1}$ is ramped to eject its charge in a current-source mode. At the end of this step, the node has been recharged to voltage V_k' such that

$$V_k' = V_k - \eta_c^2 Q_{k-1}/C_n \tag{8}$$

where C_n is the capacitance of the node (assumed constant). The recharged voltage V_k' saturates at V_{ncs} since the current source matches the receiving bucket injection current at this bias. The charge injected by the current source Q_{cs} into the receiving bucket under $P1_k$, Q_{cs}, is approximately given by

$$Q_{cs} = \eta_w\{\eta_c^2 Q_{k-1} - C_n[V_k - V_{ncs}]\} \tag{9}$$

where η_w is the wire-transfer efficiency. It should be noted that if V_k' fails to reach V_{ncs}, than Q_{cs} is taken to be zero.

In the second step, the node discharges and the voltage rises to V_k'' determined by (2) above. The charge transferred to the receiving bucket in this step is

$$Q_{\text{disch}} = \eta_w\{C_n[V_k'' - V_k']\} \tag{10}$$

so that the total charge transferred $Q_{\text{tr}} = Q_{cs} + Q_{\text{disch}}$ is simply

$$Q_{\text{tr}} = \eta_w\{\eta_c^2 Q_{k-1} + C_n[V_k'' - V_k]\}. \tag{11}$$

Noise in wire transfer is similar to that of BBD's [12]. The fundamental source of noise is in the discharge process. However, since the total charge transferred is the integral of the noisy discharge current, the rms noise charge Q_n varies as the square root of the total charge discharged. Thus

$$Q_n \simeq (qQ_{\text{disch}})^{1/2}. \tag{12}$$

The maximum value of Q_n is obtained for the maximum value of Q_{disch}, which is Q_{mtp} as given below in (13) and appears as a kTC-type noise. While not reduced by a fat zero, the noise is a small fraction of the signal for large charge packets since most of the packet is transferred during the first step of the process as Q_{cs}.

C. Simulators

In order to check the accuracy of these charge-domain expressions, a computer program was written to simulate the wire-transfer process in the time (current) domain. Excellent agreement was obtained between the simulation and the charge-domain expression above. The injection current is shown as a function of time in Fig. 3. Note that with the exception of very small charge packets, the final current or node voltage is independent of charge packet size. This helps insure high CTE.

A second computer simulation program was written to simulate the transfer of charge in an m-stage shift register using the charge-domain expressions derived above. The program included the nonlinear capacitance of the node. A charge packet was injected into the shift register which was preceded by m empty packets. The resultant output is significantly different in character than that found using a simple proportional-loss model (the usual CTE model). In the latter, an exponentially decaying tail is predicted. In the case of wire transfer, the tail decays much more slowly. Furthermore, the first trailing packet reaches a limiting value and saturates (if η_w is unity). This can be shown analytically by considering (11) in the case where V_k is set by a prior, relatively large charge packet. In this case, V_k is given by (5) and one seeks the value of Q_{k-1} such that $V_k'' = V_k$. This insures that $Q_{\text{tr}} = Q_{k-1}$ and a steady state is reached. After some algebra, one obtains the maximum trailing packet Q_{mtp} as

$$Q_{mtp} = C_n/\beta \ln[\beta I_{cs} T_c/C_n] \tag{13}$$

which scales approximately linearly with node capacitance but which is relatively insensitive to T_c. One can also reach the same result intuitively by arguing that in steady state, the injected charge packet just fills the node to $V_k' = V_{ncs}$, and the node discharges to $V_k'' = V_k$. The charge packet required for steady state is simply the voltage expressed by (5) multiplied by the node capacitance. Thus an alternative interpretation of Q_{mtp} is that it is the minimum charge packet required for a "fat zero." In general, Q_{mtp} is quite small and the use of such a "thin zero" prevents transfer inefficiency due to subthreshold effects.

III. Experimental

A. Layout and Fabrication

To experimentally verify the wire-transfer concept and theory, a test vehicle was designed and sent to a commercial CCD foundry for fabrication. The test vehicle consists of eight wire-transfer shift registers of various configurations, and a conventional 96-stage, 4-phase CCD shift register. A double-poly, double-metal, n-channel surface technology was used with a transfer electrode length of 3.5 μm corresponding to a theoretical CCD transfer time of 20 ns for a CTE of 0.999 [18]. The channel width was 50 μm, yielding a bucket capacity of 425 000 carriers/V. The devices were fabricated on a p/p^+ substrate with the p-layer nominally 10 $\Omega \cdot$ cm. All shift registers have a fill-and-spill input stage at the front end and terminate with a

two-stage source-follower output amplifier with dual-gate reset, on-chip load and on-chip sample-and-hold. The amplifier was designed to drive a 1-MΩ–22-pF oscilloscope directly. The nominal shift register had 32 stages (each as shown in Fig. 2) with a $B1$ gate length of 3.0 μm and a $B2$ gate length of 2.5 μm in accordance with the nominal minimum design rules of the foundry. The input and output junctions were 2 μm × 50 μm with additional area for contacts. An 8-stage and a 96-stage shift register with the same geometry were included. The 96-stage register is snaked resulting in a few interconnect wiring lengths of several hundred micrometers. Two 32-stage shift registers with altered geometry to explore design sensitivity were also included. One has $B1/B2$ lengths of 2.5/2.5 μm (smaller barrier) and the other has $B1/B2$ of 3.5/3.0 μm. Each of these five shift registers uses the second level of metal for interconnect between stages. The total node capacitance for each interconnect (including junction capacitance) was estimated to be 0.05 pF. Two other shift registers were included to test the effect of node capacitance. One has additional second-level metal wiring capacitance (0.02 pF) to simulate an interconnect length of 150 μm and the second has an intentional bootstrap capacitance (0.01 pF) between the node and $B1$ in an attempt to reduce the effect of transient substrate currents on node bias. A photograph of the test vehicle is shown in Fig. 4(a), and a closeup of the nominal shift register stage in Fig. 4(b).

B. Test Procedure

Several wafers from several lots were tested at the wafer level using a wafer prober. Two wafers were selected for dicing and packaging. The packaged devices were tested in a shielded test box using clock voltages derived from a Pulse Instruments PI-5800 timing generator and PI-453 MOS CCD clock drivers. These drivers have a maximum slew rate of approximately 0.2 V/ns.

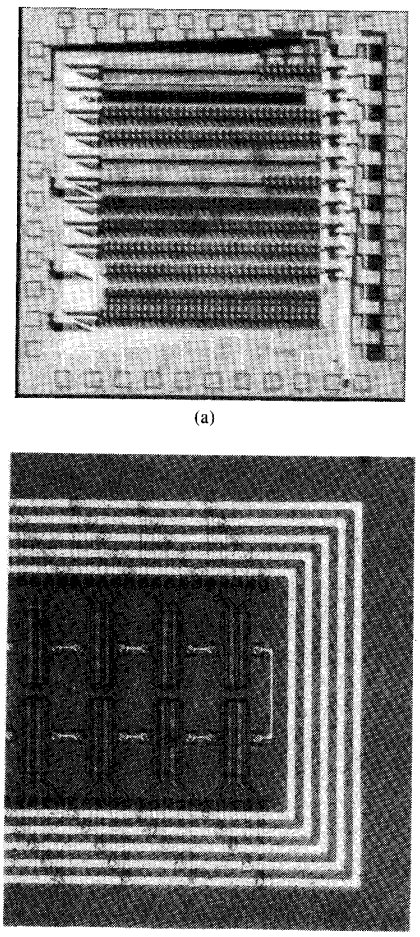
The shift registers were operated as three-phase devices with overlapping waveforms. Each phase had a 50% duty cycle with a total period of six clock cycles on the PI-5800. Thus the wire-transfer portion occupied two clock cycles, or one clock cycle for each of the two steps. In this paper, the single-clock-cycle time (T_c) is reported as the operating speed of the device, whereas the total time to transfer from one stage to the next (one wire transfer and two CCD transfers) takes six clock cycles.

Electrode $B1$ was typically dc biased at 1.0 V using a precision power supply, electrode $B2$ clocked with an adjustable peak voltage typically 1.0 V, higher than $B1$, and electrodes $P1$, $P2$, and $P3$ clocked with a common peak voltage typically 16 V. The substrate was grounded and the low level for all clocked signals was ground. A photograph of the applied clock waveforms is shown in Fig. 5.

Charge transfer efficiency was characterized for worst case operation in which a single full charge packet is loaded into a shift register with 100 empty following charge packets to examine the subthreshold node leakage. The output charge packet is distorted by loss due to subthreshold effects, wire-transfer efficiency, and CCD transfer efficiency. The measured CTE is approximately given in this case by

$$\eta = \left\{Q_1/(Q_1 + Q_2 + Q_3 \cdots)\right\}^{(1/m)} \qquad (14)$$

where Q_1 is the first charge packet, Q_2 is the first trailing charge packet, Q_3 the second trailing charge packet, etc. Fig. 6 is an oscilloscope photograph showing the output of the 8-stage, 32-stage, and 96-stage shift registers for a clock cycle time of 40 ns. The invariance of total output charge between the three different length registers indicates that fixed loss does not dominate device behavior. However, deferred charge clearly depends on register length.



(a) (b)

Fig. 4. (a) Microphotograph of the wire-transfer test vehicle chip. (b) Closeup of shift-register stage.

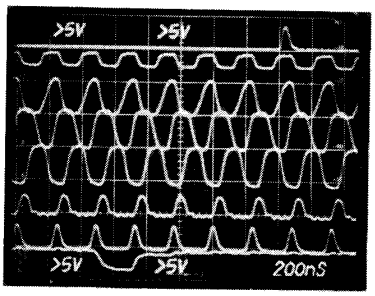


Fig. 5. Oscilloscope photograph showing applied clocking waveforms. Traces, from top to bottom, are voltage pulse for generating charge packet, V_{B2}, V_{P1}, V_{P2}, V_{P3}, amplifier reset, sample-and-hold, and output of 96-stage register ("wrapped" around screen).

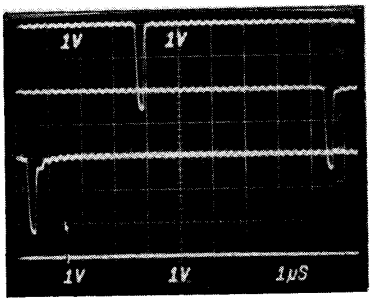


Fig. 6. Oscilloscope photograph showing the delayed output of the shift registers following input of single packet. Top trace, second trace, and third trace show output of 8-, 32-, and 96-stage shift registers, respectively. Lower trace shows voltage pulse for generating charge packet. Note that third trace is "wrapped" around screen. 100 empty packets (no fat zero) follow input packet. Clock cycle time was 40 ns.

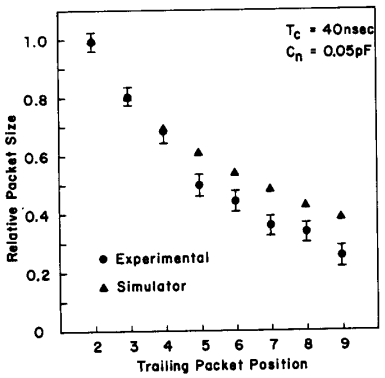


Fig. 7. Relative size of trailing charge packets (normalized to second trailing packet) as a function of packet output position measured experimentally and simulated.

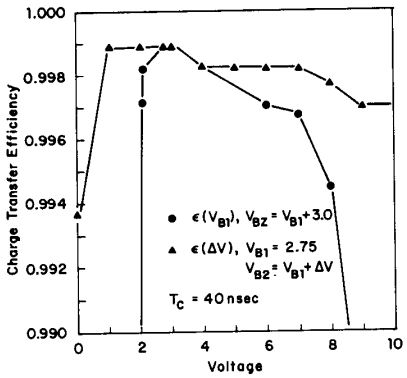


Fig. 8. Charge transfer efficiency as a function of $B1$ and $B2$ bias voltages.

C. Results

The CTE was measured for each shift register for several clock cycle times. The CTE was found to be nearly independent of cycle time for the cycle times tested, which ranged from 40 ns to 0.3 ms, provided the voltage on $B1$ was adjusted to be higher for the shorter cycle times (to insure sufficient conductance under $B1$ to accommodate the higher value of I_{cs}). Over these times, the CTE for the nominal geometry shift registers was approximately 0.9985 with an experimental accuracy of 0.0005. For the altered geometry shift registers, the smaller barrier length had lower CTE than the nominal register, and the longer barrier length had higher CTE. However, the spread was only approximately 0.0005, close to the limits of experimental accuracy and was not consistent leading to inconclusive results with respect to optimal barrier gate sizing. For the registers with additional node capacitance, the CTE was degraded as expected. The shift register with additional wiring capacitance exhibited CTE of approximately 0.9970 and the shift register with the bootstrap capacitance had a CTE of approximately 0.9960. Furthermore, the bootstrap arrangement was more susceptible to low-frequency coupling to the substrate leading to the conclusion that the bootstrap approach is inferior in the case of heavily doped substrates. The CTE for the 96-stage 4-phase CCD was tested and found to exhibit CTE exceeding 0.9999, indicating that the CCD portion of the transfer process does not limit overall device behavior.

Closer examination of the deferred charge observed in Fig. 6 reveals that it appears to have two components. The first is represented by the first trailing packet, which scales with signal size. This proportional behavior, which dominates the measured CTE, is termed η_w, the wire transfer efficiency, and includes all trapping effects at the junction diode surface discussed later. The second component of the deferred charge is a much smaller series of trailing charge packets commencing with the second trailing packet and which slowly decay in amplitude. The amplitude of this series, 1% to 2%, of the full-well packet size, is nearly independent of the size of the primary and first trailing packets. This deferred charge is attributed to the subthreshold effect.

Using η_w as an adjustable parameter in the shift register simulator, and including the subthreshold effect, reasonable fitting of the observed trailing packets in the nominal geometry shift registers was obtained using η_w approximately equal to 0.9988 as shown in Fig. 7. Without including the subthreshold effect, a proportional loss model cannot be sensibly fitted to the experimental data. Note that the trailing packets are normalized to the second trailing packet. With subthreshold effect charge loss, the net CTE agrees with the experimental CTE of 0.9985.

The nominal geometry 96-stage wire-transfer shift register was also tested for other combinations of duty cycle, where duty cycle is defined as the ratio of number of full charge packets to number of empty packets. For duty cycles ranging from 0.01 to 100, the CTE of the register appeared to remain constant, confirming that fixed-loss effects do not dominate device behavior. Fixed losses, expected from (7), may be ameliorated by dark current in the junction diodes which refill charge lost to subthreshold leakage providing the thin zero described above.

For a fixed cycle time, the effect of electrode $B1$ and $B2$ bias voltages was investigated. The measured CTE as a function of these voltages is shown in Fig. 8. The dc voltage on electrode $B1$ is not overly critical provided it is greater than the MOS threshold voltage. The voltage range for $B2$ was more robust provided it was biased greater than $B1$.

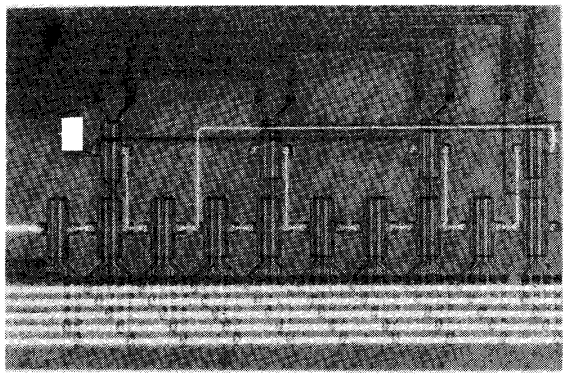
A wafer with a buried-channel implant was also tested. The major difference between the buried-channel and surface-channel devices (from the perspective of the wire-transfer model) is that the node is n^+/n and there is no depletion region edge in the heavily doped region. Thus the effect of carrier trapping in the vicinity of the junction should be reduced. The node capacitance is also lower implying lower loss due to subthreshold effects. Indeed, the buried-channel devices were found to have CTE as high as 0.9999 which is attributed to these factors (rather

than increased speed) since the CTE in the surface-channel devices was not a function of operating frequency.

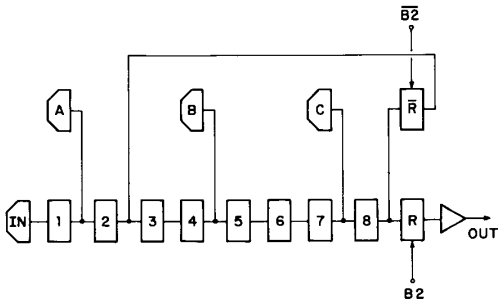
The CTE of the surface-channel devices varied from lot to lot and poor CTE correlated with poor junction diodes. The conclusion is drawn that charge trapping in the vicinity of the junction diodes is presently limiting the performance of the wire-transfer process. However, CTE did not appear to vary significantly from wafer to wafer or device to device in the final lot tested, and is attributed to deliberate fabrication of higher quality junctions.

The ability of the screen electrode ($B2$) to prevent barrier height modulation under electrode $B1$ was tested using a single shift register stage with an external connection to both junctions. Using a pulsed charge domain measurement, similar to that employed by Scott and Chamberlain [13], a relative measurement of the potential ψ_{B1} under $B1$ could be made. The transfer function $d\psi_{B1}/dV_{B2}$ was measured for each of three gate geometries. It was found that the transfer function was approximately 20, 30, and 50 mV/V for the 3.5/3.0, 3.0/2.5, and 2.5/2.5 $B1/B2$ geometries, respectively. The screened transfer function for $P1$ ($d\psi_{B1}/dV_{P1}$) was then measured and found to be approximately 0.7 mV/V, indicating excellent screening by the 2.5-μm $B2$ electrode.

The noise floor in the measurements was dominated by residual 60-Hz and RF noise in the test station, with a value on the order of 2 mV. Thus the measured dynamic range (defined as 20 log SNR) was 62 dB independent of shift register length. However, using the expression in (12) with a full bucket equal to 4×10^6 carriers and Q_{mtp} equal to 4.4×10^4 carriers, one obtains a noise level of 210 carriers per transfer, or a theoretical dynamic range of 65 dB after 96 transfers.



(a)



(b)

Fig. 9. (a) Photograph of router/parallel-load experiment. (b) Block diagram of router/parallel-load experiment.

IV. Routing and Parallel Load

A. Router

As discussed in the Introduction, the primary function envisioned for wire transfer is the topological crossing of signals in charge-domain signal processing circuits. However, wire transfer allows other functions such as summation and routing to be performed as well. An experimental test site was included on the wire-transfer test vehicle chip for exploring this concept. As shown in Fig. 9, the test site consists of eight shift register stages. The ninth stage is a router structure consisting of two parallel stages with the input diode junctions connected together. The stages' electrodes are tied in parallel with the exception of the $B2$ electrodes. These electrodes are used for steering the charge packet (current source) to one stage or the other in manner similar to that proposed by Heller [19].

To test the router, a single charge packet is loaded into the shift register input and shifted to the router. The router is clocked to cause the charge packet to be steered into the upper register. The output of the upper register is tied back to the node following the second stage register. Thus the routed charge packet is summed with the output of the second stage and loaded into the third stage. However, in the experiment, only empty packets followed the initial packet. The charge packet is again clocked toward the end of the shift register. In one timing pattern, the charge packet is allowed to pass on to the output amplifier. In a second timing pattern, the charge packet was diverted a second time and looped back to the output of the second stage before being allowed to pass to the output amplifier. A double-exposure oscilloscope photograph illustrating this programmed delay function is shown in Fig. 10.

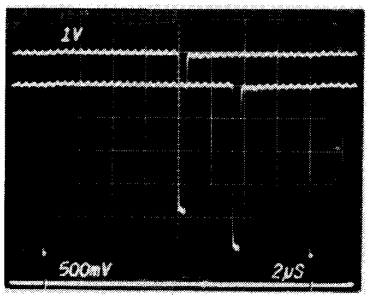


Fig. 10. Double-exposure photograph showing output of shift register for one programmed loop (top trace) and two loops (second trace). Lower trace shows voltage pulse for generating charge packet.

The ability of the router to effectively steer charge packets can be measured by examining the residual charge leaking through the nonselected stage. The ratio of the magnitude of the routed packet to the leakage is a measure of the router rejection ratio. This ratio was found to be approximately 600:1.

If both $B2$ electrodes in the router stage are selected, the input charge packet is split between the two receiving wells. One charge packet is transferred to the output amplifier while the other is recirculated and split a second time. This process is repeated yielding output packets split in powers of two. This splitter mode worked unexpectedly well with split accuracy of better than 1%. Splitting and programmable routing make the implementation of a charge-domain multiplying digital-to-analog converter (MDAC) straightforward [7].

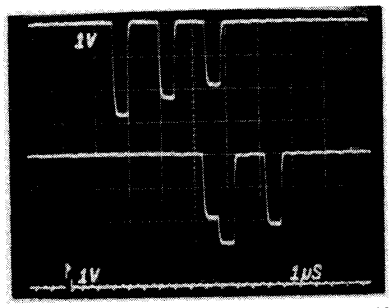


Fig. 11. Double-exposure photograph showing output of shift register following parallel load of 3 charge packets (top trace) and following load and recirculation of first packet (second trace). Lower trace shows voltage pulse for generating charge packet.

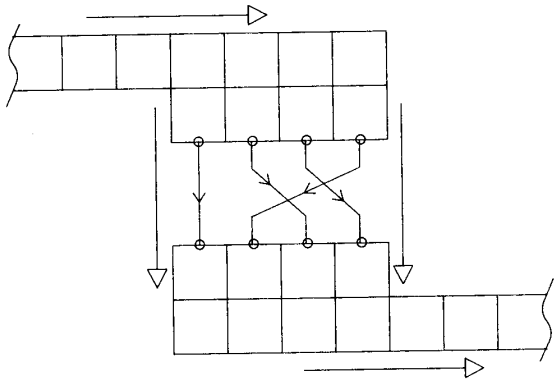


Fig. 12. Block diagram of serial/parallel-parallel/serial circuit for arbitrary reordering of serial charge packet data stream using wire transfer.

B. Parallel Load

In addition to the router loop-back on this test site, a parallel-load structure was also included. Three charge packets, Q_a, Q_b, and Q_c can be simultaneously generated and summed using wire transfer with the outputs of stages 1, 4, and 7, respectively, thus effecting a parallel-to-serial multiplexing operation. The top trace of Fig. 11 demonstrates this function. The charge packet router was programmed to recirculate packets Q_c and Q_b thereby changing the sequential order of output packets from Q_c–Q_b–Q_a to Q_a–Q_c–Q_b, as illustrated in the lower trace of Fig. 11.

Changing the serial order of charge packets in a data stream is an important function for focal-plane image processing, particularly in the case of pyramid compression schemes [20]. The use of a router is a programmable means for performing this function. However, a simple CCD serial–parallel conversion, followed by wire-transfer reordering and finally CCD parallel–serial conversion can be used more effectively for hard-wired applications, as illustrated in Fig. 12.

V. Summary

A structure for the virtual transfer of charge packets across metal wires has been analyzed theoretically and simulated by computer. An experimental test vehicle was fabricated and demonstrated good performance over a wide frequency range. The observed CTE of the structure ranged between 0.998 and 0.999 for surface-channel devices, and was as high as 0.9999 for buried-channel devices. The devices were found to be robust with respect to bias voltages and clock waveforms.

In the experimental devices described in this paper, the test station was the limiting consideration for both speed and dynamic range performance. The minimum clock cycle time used was 40 ns and the maximum dynamic range was approximately 62 dB, limited by residual 60-Hz and RF noise in the test station.

The wire-transfer process allows for the topological crossing of signal charges in charge domain signal processing circuitry. The wire-transfer structure also facilitates corner turning, changing channel width, and the programmable steering of charge packets. The wire-transfer structure also makes charge summation and charge packet splitting readily achievable. The structure provides a degree of design flexibility and methodology previously denied CCD circuit designers.

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