A Novel Trench-Defined MISIM CCD Structure for X-ray Imaging and Other Applications

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Abstract—**A new charge-coupled device (CCD) utilizing a trench-defined metal-insulator-semiconductor-insulator-metal (MISIM) sandwich structure is proposed and analyzed. The CCD features high charge capacity and a deep photogenerated carrier collection depth. The trench CCD structure has potential application in X-ray imaging as well as in high-density visible and infrared imaging.**

I. Introduction

A SOLID-STATE imaging device useful for the X-ray portion of the spectrum has been elusive due to the low absorption coefficient of X-rays in silicon [1] and to the fabricational difficulties associated with GaAs and other materials with higher absorption coefficients. Typically, conventional imagers with deposited phosphorescent layers are used to indirectly obtain X-ray images [2], but these devices have low overall quantum efficiency. Direct-detection silicon charge-coupled device (CCD) structures fabricated on high-resistivity silicon (e.g., 1–10 kΩ·cm) have very deep depletion regions extending hundreds of micrometers into the substrate thus allowing efficient collection of deeply generated carriers [3]. Although some progress has been recently reported [4], the resistivity of the silicon usually suffers from contamination introduced during processing. Furthermore, large voltages (e.g., 100 V) are often required to sweep out the required depletion region. Other novel techniques for realizing a silicon X-ray imager on high-resistivity material are also under investigation [5].

A new trench metal–insulator–semiconductor–insulator–metal (MISIM) CCD structure is proposed for X-ray imaging applications. This structure does not require high-resistivity material nor high voltages and retains the high quantum efficiency of very deep depletion devices. It may be useful for high-density high-capacity signal processing applications as well. The trench CCD structure is shown in Fig. 1(a) and (b). Majority-carrier signal charge is confined in the semiconductor sandwich located between the trenches. Note that the trenches, which can be formed in a number of ways, including the use of reactive-ion etching, might be better described as fence-post holes, thus facilitating subsequent overlapping polysilicon electrode definition. The capacity of the structure is increased over conventional buried-channel CCD's since the charge packet has significant vertical extent in addition to the planar directions. The depth of the trench, which in principle can extend through the entire wafer, determines the additional charge capacity and carrier collection region. Since collection of generated carriers in the vertical direction is facilitated by the trench structure, the need for high voltages and high-resistivity material is eliminated. Fabrication complexity is not increased beyond that which is necessary for dynamic random access memory (DRAM) structures except in the case of very deep (e.g., 20 μm or more) trenches. The fill factor of the structure for direct visible imaging is reduced due to the trench real estate. An amorphous-silicon overlayer might be employed for detection to increase the fill factor and to improve the blue response, with the trench CCD used for high-capacity readout.

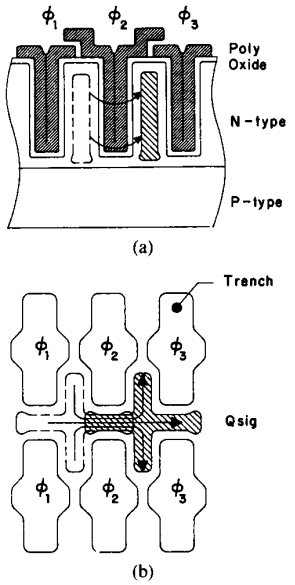

Fig. 1. Proposed trench CCD structure: (a) cross section, and (b) top view (polysilicon electrodes not shown). Three of four phase electrodes illustrated.

II. Trench CCD Analysis

To understand the operation of the trench CCD, a one-dimensional analysis of an MISIM structure is performed. The semiconductor portion of the sandwich has width w, and each oxide has thickness d_{ox}. The sandwich is depleted from both sides, and the neutral region toward the center has width equal to $w - Q_{sig}/qN_d$, which implicitly defines Q_{sig}. The maximum charge capacity of the structure scales linearly with doping concentration N_d and trench depth. The electrostatic

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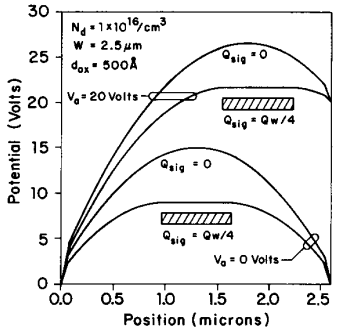

Fig. 2. Electrostatic potential across full sandwich structure for various conditions.

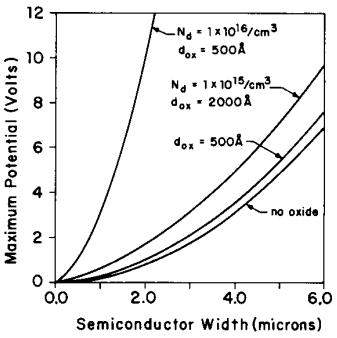

Fig. 3. Maximum channel potential as a function of semiconductor width.

potentials of each side of the sandwich (the left and right electrodes) are defined as ψ_l and ψ_r. The applied potential difference $\psi_r - \psi_l$ is defined as V_a. The electrostatic potential in the structure is plotted as a function of position in Fig. 2.

With V_a and Q_{sig} both zero, analysis reveals the maximum electrostatic potential in the semiconductor to be

$$\psi^0_{m0} = (\psi_l + \psi_r)/2 + Q_w/C_e \tag{1}$$

where Q_w is defined as $qN_d w$, and the effective capacitance C_e is defined as $(1/2C_{ox} + 1/8C_w)^{-1}$. The terms C_{ox} and C_w are defined as $e_0 e_{ox}/d_{ox}$ and $e_0 e_s/w$, respectively, where e_s and e_{ox} are the relative dielectric constants of the semiconductor and insulator, respectively, and e_0 is the permittivity of free space. The zero-applied-bias, zero-signal-charge maximum potential ψ^0_{m0} scales linearly with doping concentration and as the square of the width w and is plotted in Fig. 3. Note that a reduced width can be used to decrease the potential and define the edge of the channel, as illustrated in Fig. 1(b). Note also that the dependence on oxide thickness is relatively weak. In fact, the oxide can be eliminated from the structure yielding a Schottky-barrier electrode, thus making the CCD suitable for GaAs implementation as well as improving its radiation hardness.

With V_a zero but Q_{sig} nonzero, the potential is reduced to

$$\psi_{m0} = \psi^0_{m0} - Q_{sig}/C_e - (1 - Q_{sig}/Q_w)(Q_{sig}/8C_w). \tag{2}$$

Finally, if a bias is applied across the sandwich of magnitude V_a, the center of the signal charge shifts position by the amount

$$\Delta X = w[V_a/\{2Q_w/C_{ox} + (Q_w - Q_{sig})/C_w\}]. \tag{3}$$

Note that the shift is linear with applied bias. Defining ΔQ as $qN_d \Delta X$, the maximum potential becomes

$$\psi_m = \psi_{m0} + \Delta Q^2/2C_w Q_w . \tag{4}$$

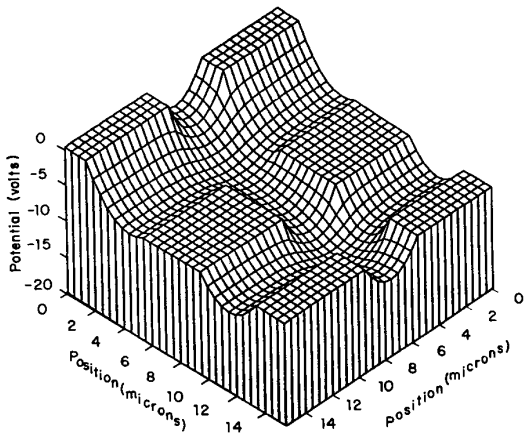

Fig. 4. Results of 2-D modeling with $N_d = 1 \times 10^{15}/cm^3$, $w = 4$ μm, and no oxide. Electron potential for $V_a = 6$ V is shown.

In the trench CCD, four adjacent trenches are needed to form one potential well (see Fig. 1(b)), and the charge is largely confined between them in the central semiconductor region. Although in principle this region must be treated by a two-dimensional analysis, its deeper potential can be estimated using an effective width w_{eff} in the 1-D analysis where w_{eff}/w is found to be 1.3 and 1.4 using 2-D modeling.

Charge is transferred in the trench CCD from one central region to the next by applying appropriate bias voltages in a four-phase clocking scheme. The deeper potential in the central region appears as a barrier to charge transfer, which can be overcome by applying a transfer voltage V^x_a approximately given by

$$V^x_a = 2[(w_{eff}/w)^2 - 1]\psi^0_{m0}. \tag{5}$$

In Fig. 4, the electrostatic potential of an empty trench CCD in a slice parallel to the surface is represented. The flat regions correspond to the trench electrodes, and a bias voltage sufficient for complete transfer is applied between adjacent phases.

The charge transfer efficiency in the trench CCD can be expected to be excellent, provided the signal charge does not come into contact with traps at the semiconductor–insulator interface. This contact is referred to as a crash condition. In a Schottky-gate implementation, a crash would result in the spilling of the signal charge with substantial leakage current occuring just prior to this. The minimum applied bias resulting in a crash condition can be determined in a 1-D analysis by setting $(Q_w - Q_{sig})/2 = \Delta Q$ yielding the crash voltage V^{cr}_a:

$$V^{cr}_a = (1 - Q_{sig}/Q_w)(Q_w/2)\{2/C_{ox} + (1 - Q_{sig}/Q_w)/C_w\}. \tag{6}$$

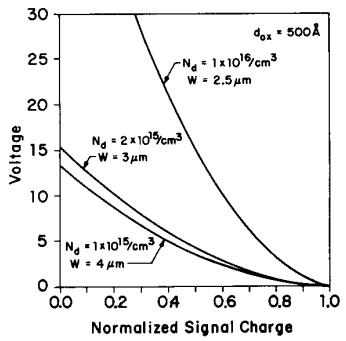

Fig. 5. Crash voltage as a function of signal charge.

The crash voltage as a function of signal charge is shown in Fig. 5. Note that large signals are more susceptible to crashing than are small signals. In the trench CCD, the clock signals should be ramped to prevent the accidental crash of large charge packets prior to transfer.

III. Conclusions

Although conceived for improving X-ray imager performance, the trench CCD yields high charge capacity for small surface area and can serve as a high-density readout multiplexer for visible and infrared imager applications. Recent consideration indicates that two-phase operation can be implemented by changing the shape of the trench in Fig. 1(b) in order to break symmetry [6]. In this case, a trench CCD with an 8-μm pixel size and a trench aspect ratio of 10 has an estimated full well capacity of approximately one million electrons. This is approximately a factor of 5 larger than one might expect from a conventional buried-channel CCD with the same pixel size. Other applications for the trench CCD in digital signal routing and processing are currently under investigation and appear promising.

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