Transport properties and applications of unstrained $In_{0.75}Ga_{0.25}As/Al_{0.6}Ga_{0.4}As$ heterojunctions

D. V. Rossi and E. R. Fossum
Department of Electrical Engineering, Columbia University, New York, New York 10027
P. D. Kirchner and J. M. Woodall
IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

(Received 30 January 1990; accepted 10 April 1990)

The electrical and structural properties of a severely mismatched MBE-grown InGaAs/AlGaAs heterojunction were investigated. The heterojunction shows rectification and the InGaAs's mobility is measured to be 142 cm^2/V s. This low mobility InGaAs contact can be used as the resistive, rectifying contact of a heterojunction-resistive-gate charge-coupled device.

I. INTRODUCTION

While emphasis has been placed on coherent heterojunctions for high speed device structures, the use of mismatched layers unstrained via misfit dislocations has been limited. Yet, in certain cases, the misfit dislocated layer can be advantageous. For example, in the growth of GaAs on $In_{0.53}Ga_{0.47}As$ it has been shown that the misfit dislocations can be isolated to the GaAs interface region suggesting the integration of optoelectronic and high speed logic devices.[1] Alternatively, $In_{0.4}Ga_{0.6}As$ has been grown on GaAs substrates yielding high performance 1.3 μm metal–semiconductor–metal (MSM) detectors which can be integrated with high speed GaAs devices.[2] In fact, the incorporation of a misfit dislocated layer in the active portion of heterojunction bipolar transistors has resulted in higher gain devices compared to those in which a pseudomorphic layer was used.[3]

In this work, a misfit dislocated $In_{0.75}Ga_{0.25}As/Al_{0.6}Ga_{0.4}As$ heterojunction was investigated, since its properties are efficacious for the implementation of a semiconductor, resistive gate GaAs channel charge-coupled device. As depicted in Fig. 1, a resistive gate charge-coupled device (RGCCD) employs a resistive layer which acts as a continuous potential divider between spaced phase electrodes, ensuring that the charge moves under the constant influence of an electric field.[4] Conventional RGCCDs utilize a ceramic metallic (cermet) compound whose composition must be carefully controlled to ensure proper optical and electrical properties.[5] The use of a semiconductor resistive gate, however, exploits the compositional control and uniformity inherent in molecular beam epitaxy (MBE). In addition, novel device structures, such as an internal photoemission CCD imager, can be implemented since the band offset between the resistive and channel layer can be controlled through proper selection of materials. The InGaAs/AlGaAs heterojunction was chosen since the small band gap, high electron affinity InGaAs suggests a large band offset to AlGaAs,[6] yielding a low leakage structure. Furthermore, nonalloyed ohmic contact formation to air-exposed InGaAs containing a large In mole fraction is facilitated by the Fermi level being pinned near the conduction band,[7] which simplifies the RGCCD fabrication process. This paper reports the basic electrical properties of this severely mismatched heterojunction. The heterojunction shows rectification and in one sample exhibited a 1.0 eV barrier height. The low mobility observed in the InGaAs layer is attributed to defects, and is advantageous for the RGCCD application.

II. EXPERIMENT

Figure 2 illustrates the basic layer structure used for the experiments. The material was grown by MBE on ⟨100⟩ oriented semi-insulating GaAs substrates. After a 1 μm undoped buffer layer, a 0.2 μm, 10^{17} cm^{-3} n-type GaAs active layer grown and monotonically graded over 20 nm to $Al_{0.6}Ga_{0.4}As$ (which was undoped) in order to enhance the band offset between the active and resistive layers. Prior work[8] has shown that the measured barrier height between GaAs and $In_{0.75}Ga_{0.25}As$ can also be enhanced by incorporating a thin layer of As at the interface; however, this method was not applied to these structures. At this point, two different growth sequences occurred: 45 nm of $In_{0.75}Ga_{0.25}As$ was grown on sample 1, while on sample 2 5 nm of $In_{0.9}Ga_{0.1}As$ was grown followed by 40 nm of $In_{0.75}Ga_{0.25}As$. Previous investigation[10] of three-dimensionally nucleated $In_{0.9}Ga_{0.1}As$ showed a regular array of edge-type misfit dis-

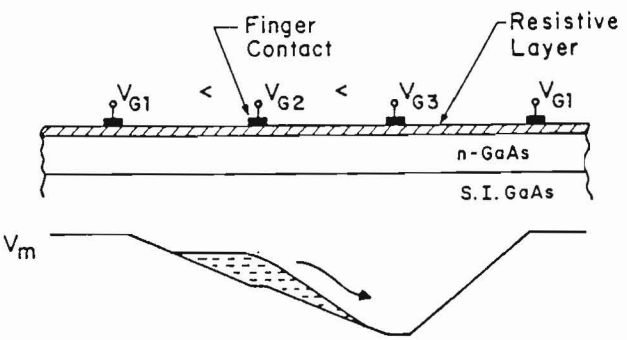

FIG. 1. Schematic cross section of a resistive gate charge-coupled device and the channel potential.

 0734-211X/90/040779-04$01.00

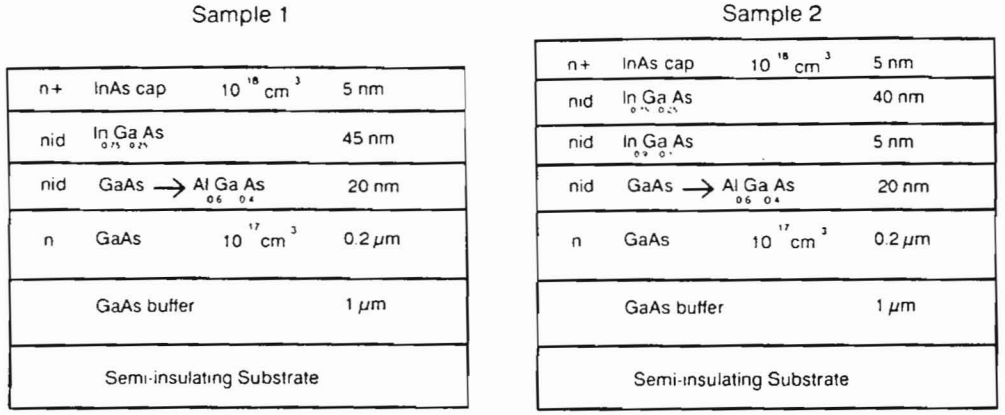

FIG. 2. Schematic cross section of the experimental structures. The InGaAs layer of sample 2 was three-dimensionally nucleated with 5 nm of $In_{0.9}Ga_{0.1}As$ to induce strain relief.

locations formed at the interface during an early stage of growth which accommodates approximately 80% of the mismatch to GaAs. This allows the thin $In_{0.75}Ga_{0.25}As$ layer to be grown on the $In_{0.9}Ga_{0.1}As$ under reduced strain conditions, in contrast to the first sample where plastic deformation would be expected to continue throughout growth. Both samples were capped with 10^{18} cm^{-3} Si doped InAs to assist ohmic contact formation. The entire resistive gate was grown at a 450 °C substrate temperature.

These samples were then processed to form the RGCCDs as well as conventional capacitive gate CCDs and numerous test structures for characterizing the heterojunction and material properties. Processing begins with device isolation by first etching the InGaAs layer with H_2SO_4:H_2O_2:H_2O (1:1:90) followed by etching the active layer down to the undoped buffer layer using NH_4OH:H_2O_2:H_2O (1:1:200). The former etchant removes the InGaAs at a rate of approximately 1.4 nm/s and is not selective, while the latter etchant removes about 120 nm/min of the active layer. Having calibrated the InGaAs etch rate during the mesa level, the same etchant is used to define the resistive gate regions by a timed etch down to the active layer. AuGe ohmic contacts are formed by lift-off and rapid thermal annealing at 425 °C for 40 s in a forming gas ambient. Cr/Au is then patterned, simultaneously forming Schottky barriers to the active layer and nonalloyed ohmic contacts to the InGaAs resistive layer. At this point, all the test structures are complete and the remaining processing is for the CCDs alone. This involves electron-beam evaporated SiO which is used as an intermetal dielectric separating the gate level metallization from the subsequently deposited Cr/Au interconnect metal.

III. RESULTS AND DISCUSSION

The barrier height associated with transport across the heterojunction barrier was calculated using the results of a room temperature current–voltage (I–V) measurement, assuming a simple thermionic emission process obeying the basic Schottky barrier expression. Figure 3 depicts typical I–V curves for samples 1 and 2. Despite the fact that sample 2 was nucleated with $In_{0.9}Ga_{0.1}As$, whose band gap is approximately 120 meV smaller than that for $In_{0.75}Ga_{0.25}As$, the barrier heights for both samples are comparable and are 0.81 and 0.79 eV, respectively. This result would imply that the Fermi level is pinned by electrically active misfit dislocations at the interface.[10] It must be reported, however, that the barrier height measured for the heterojunction formed on a wafer grown several months earlier yielded a barrier height of 1.0 eV (Fig. 4). Such a large barrier height may be applicable to MESFETs incorporating the InGaAs gate structure, translating into a larger noise margin. This wafer was grown similarly to sample 1, except the GaAs epitaxial layer was 0.5 μm and doped at 5×10^{18} cm^{-3} and the graded AlGaAs layer was also doped at this level. These differences, however, cannot account for the 0.2 eV discrepancy in observed barrier height and until a controlled experiment is performed this interesting result can be attributed to possible differences in the AlGaAs compositional grade, since the samples were grown at different times.

A resistive gate FET from sample 2 is depicted in Fig. 5, confirming the resistive gate's ability to modulate the channel potential. These RGFETs were comparable to convential MESFETs present on the same sample with respect to transconductance and threshold voltage. Hall effect measurements performed on both layers indicate a mobility of 142 cm^2/V s, which is considered to be defect limited, and an n-type sheet carrier concentration of 2.7×10^{12} cm^{-2}. Such a

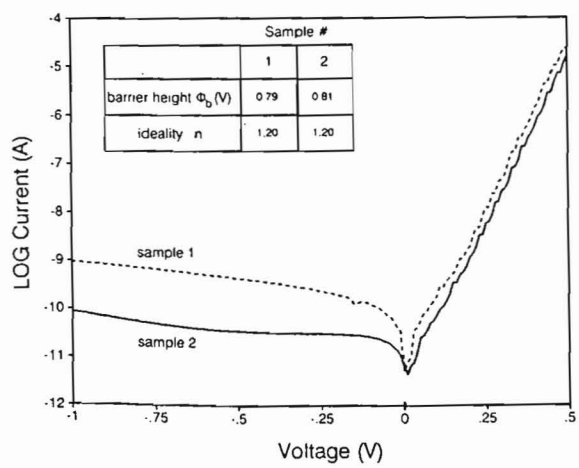

FIG. 3. Typical current–voltage curves for heterojunction Schottky diodes formed on samples 1 and 2.

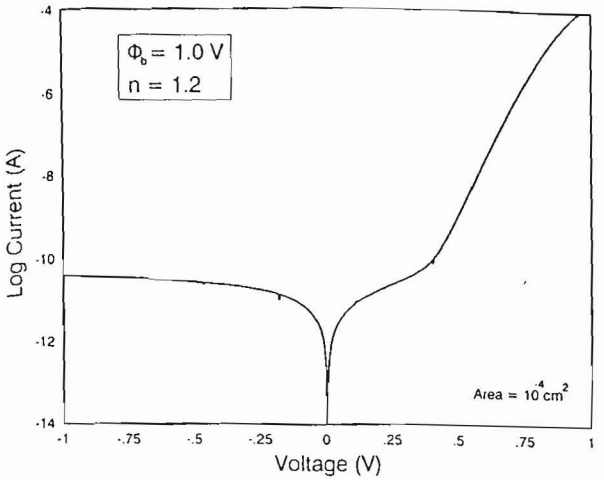

FIG. 4. Typical current–voltage curve for heterojunction Schottky diodes formed on a wafer similar to sample 1 but grown many months earlier. This high 1.0 eV barrier height has not yet been reproduced.

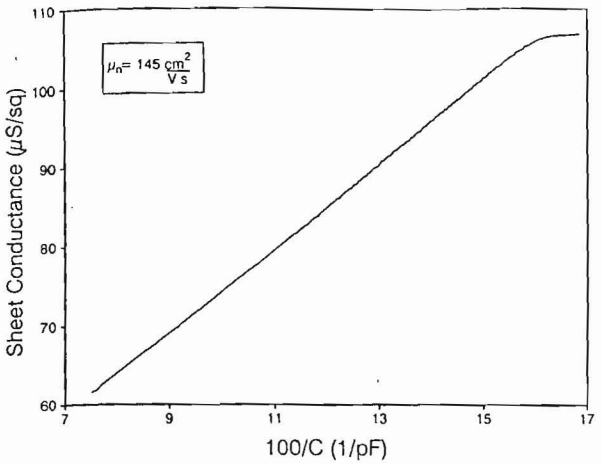

FIG. 6. Sheet conductance of resistive gate layer vs reciprocal gate capacitance.

low mobility is expected, considering the rapid mobility degradation with decreasing film thickness observed for InAs layers grown on GaAs.[11-13]

The InGaAs resistive layer's mobility can also be determined by measuring either its dc conductance or its small signal ac conductance while ramping the bias of the GaAs channel region.[14] The structure used for this measurement is essentially a 100 μm gate length RGFET possessing two gate finger contacts, one at each end of the resistive gate. It can be shown that the resistive gate's dc sheet conductance G_{sh} is given by the expression $G_{sh} = G_b + (\mu_n q \epsilon N_d A)/C$, where G_b is the bulk conductance of the resistive layer, corresponding to a flatband condition, μ_n is the InGaAs mobility, q is the electric charge, ϵ is the GaAs dielectric constant, N_d is the GaAs doping concentration, A is the resistive gate area, and C is the capacitance of the resistive gate structure and is the same expression as for conventional Schottky barriers. It follows directly that the small signal conductance g_{ac} is related to the mobility by the expression $g_{ac} = \mu_n V_d C/A$, where V_d is the dc bias between the two contacts to the resistive gate. Figure 6 depicts the result for the dc measurement while the ac measurement, which was performed at 10 kHz using a Stanford Research Systems SR530 lockin amplifier, is shown in Fig 7. While the mobility extracted from the dc measurement corresponds to the Hall effect measurement, the mobility determined from the ac technique is somewhat low, yet reasonable. Thus, this technique is useful for mobility characterization of such structures.

IV. SUMMARY

The basic electrical properties of a severely mismatched InGaAs/AlGaAs heterojunction have been presented. A barrier height of approximately 0.8 eV is measured for this heterojunction, regardless of the 0.15 InAs mole fraction

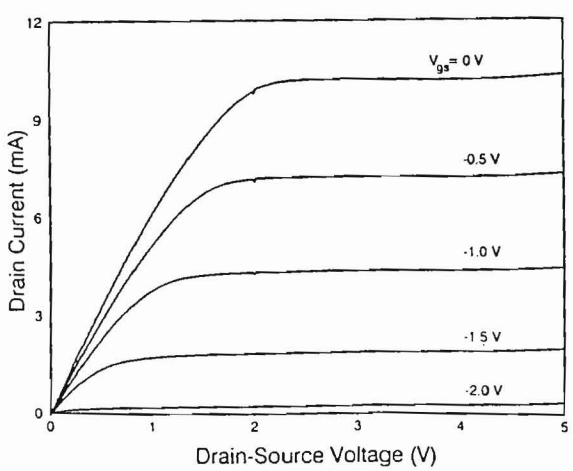

FIG. 5. dc drain characteristic of a resistive gate FET formed on sample 2.

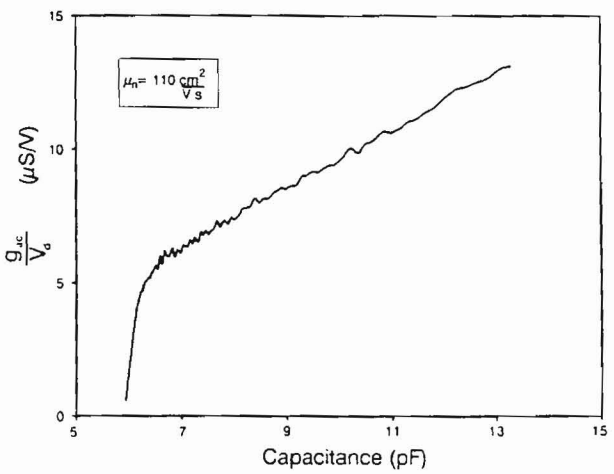

FIG. 7. Small signal sheet conductance divided by resistive gate dc bias vs gate capacitance.

difference of the interfacial InGaAs, suggesting that the Fermi level is pinned by the misfit dislocations. The low mobility InGaAs layer and good rectifying nature of this heterojunction, has been exploited in the implementation of a heterojunction-resistive-gate CCD whose performance will be reported elsewhere. In addition, a 1.0 eV barrier height has been measured for a similar heterojunction which, though not yet reproduced, could have MESFET applications.

ACKNOWLEDGMENTS

The authors thank Ronald F. Marks of IBM Research for help with the MBE growth. This work is supported by an IBM Graduate Fellowship (D.V.R) as well as by the ONR URI Program.

[1]C. Y. Chen, S. N. G. Chu, and A. Y. Cho, Appl. Phys. Lett. **46**, 1145 (1985).
[2]D. L. Rogers, J. M. Woodall, G. D. Pettit, and D. McInturff, IEEE Electron Device Lett. **9**, 515 (1988).
[3]L. P. Ramberg, P. M. Enquist, Y. K. Chen, F. E. Najjar, L. F. Eastman, E. A. Fitzgerald, and K. L. Kavanagh, J. Appl. Phys. **61**, 1234 (1987).
[4]J. A. Higgins, R. A. Milano, E. A. Sovero, and R. Sahai, Proc. IEEE GaAs IC Symp. (1982), p. 49.
[5]J. -I. Song and E. R. Fossum, IEEE Trans. Electron Devices, **36**, 1555 (1989).
[6]S. P. Kowalczyk, W. J. Schaffer, E. A. Kraut, and R. W. Grant, J. Vac. Sci. Technol. B **20**, 705 (1982).
[7]L. J. Brillson, M. L. Slade, R. E. Viturro, M. K. Kelly, N. Tache, G. Margaritondo, J. M. Woodall, P. D. Kirchner, G. D. Pettit, and S. L. Wright, J. Vac. Sci. Technol. B **4**, 919 (1986).
[8]D. V. Rossi, E. R. Fossum, G. D. Pettit, P. D. Kirchner and J. M. Woodall, J. Vac. Sci. Technol. B **5**, 982 (1987).
[9]M. F. Chisholm; P. D. Kirchner, A. C. Warren, G. D. Pettit, and J. M. Woodall (unpublished).
[10]J. M. Woodall, G. D. Pettit, T. N. Jackson, and C. Lanza, Phys. Rev. Lett. **51**, 1783 (1983).
[11]C.-A. Chang, C. M. Serrano, L. L. Chang, and L. Esaki, J. Vac. Sci. Technol. **17**, 603 (1980).
[12]R. A. A. Kubiak, E. H. C. Parker, and S. Newstead, Appl. Phys. A **35**, 61 (1984).
[13]M. Yano, M. Nogami, Y. Matsushima, and M. Kimata, Jpn. J. Appl. Phys. **16**, 2131 (1977).
[14]L. Esaki, W. E. Howard, and J. Heer, Appl. Phys. Lett. **4**, 3 (1964).