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Reduced leakage current in Al-GaAs Schottky diodes containing an interfacial arsenic layer

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Understanding Fermi-level pinning at metal semiconductor interfaces remains a formidable problem. Models which attempt to describe this behavior include metal induced gap states (MIGS)[1], extrinsic defect generation during adatom deposition[2], and effective work functions of mixed interface phases resulting from chemical reactions between metal and semiconductor.[3] The Effective Work Function (EWF) model asserts that these reactions primarily result in excess anion precipitates (e.g. arsenic) which dominate the interface behavior and thus dictate the effective work function. However, ohmic behavior has been reported from a low work function phase of Au-Ga that forms at the periphery of an annealed Au-GaAs contact.[4] If smaller areas of low work function phases exist at the unannealed interface, their weight in the effective work function and the observed barrier height could be low, but they could noticeably increase the reverse bias leakage current. Elimination of the low work function phases at the GaAs interface would reduce the reverse bias leakage current. We have attempted to reduce the reverse bias leakage current by creating a homogeneous "metal"-GaAs interface through deposition of an arsenic layer prior to metallization.

In this experiment, a Molecular Beam Epitaxy (MBE) system was used to grow an n-GaAs/As/Al 'test' structure and an n-GaAs/Al 'control' structure. The GaAs growth and the arsenic and aluminum evaporations were performed sequentially without intermediate removal from the MBE growth chamber. Mesas were defined by photolithography and wet chemical etching. Current-voltage (I-V) and capacitance-voltage characteristics were measured. Initial I-V measurements show a twenty-five fold reduction of reverse bias leakage current in the sample with the arsenic interlayer. A typical 50mV increase in measured barrier height accompanies, but does not fully explain, the large decrease in leakage current. This would be expected from a mixed-phase interface in the control structure.

In addition, we will report some preliminary results on GaInAs/GaAs interfaces in which we find the measured barrier height extracted from I-V data depends on the condition of the GaAs surface prior to deposition of the GaInAs layer.

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