into the 12-stage SP^3 register and the nine pixel neighborhood is transferred in parallel to a conventional parallel-to-serial 9-stage CCD register for serial output. While the nine pixels are being transferred out of the conventional register, the subsequent nine-pixel neighborhood is reordered such that a continuous output stream is generated.
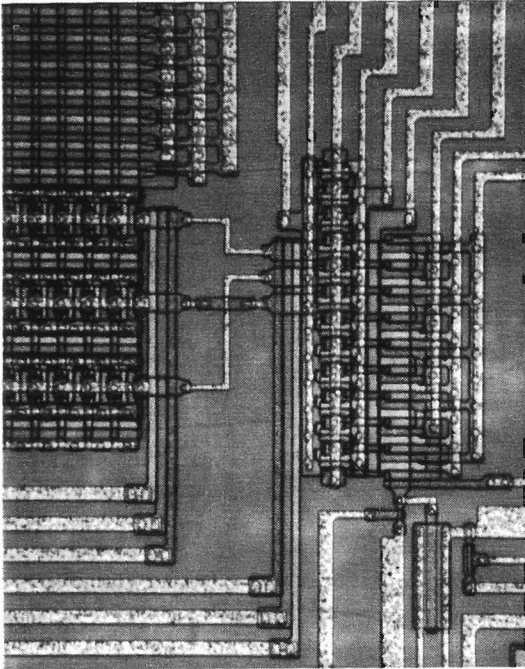

Fig. 5   Photograph of the image reorganization circuitry.
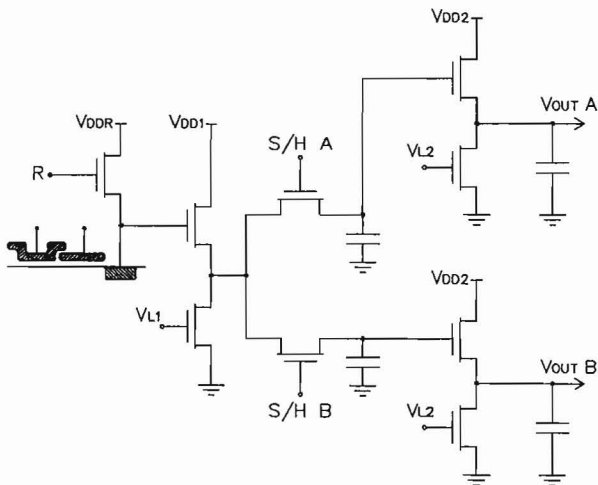

Fig. 6   Circuit diagram of output sampling stage.

The serial pixel stream is loaded into the output sampling block. This block consists of a first stage source-follower output amplifier (which can be seen in Fig. 5) followed by dual (parallel) sample-and-hold circuits (Fig. 6). The first pixel data is sampled by the upper S/H circuit. The subsequent eight pixels from the neighborhood are sampled by the lower S/H circuit. The S/H circuits are buffered by a matched pair of source-followers with active load transistors, which in turn drive the output pads. Thus the difference in output voltage between the matched circuits is proportional to the difference between the center pixel intensity and each of its surrounding neighbors.

EXPERIMENTAL RESULTS

The chip was tested both electrically and optically. The imaging and processing circuitry was operated with 5 volt three-phase clocks, yielding a total estimated dissipated power of $150\mu W$ at a 30 Hz frame rate, not including the off-chip drive amplifiers. These add an estimated 7 mW of power since they were designed to drive an oscilloscope directly (1 MΩ 22 pF load), but in principle need only drive an A/D converter.

Electrical

The circuit was tested electrically at the wafer-probe and chip level at a 277 kpixel and at a 2 Mpixel/sec output rate respectively. An additional serial-to-parallel charge electrical input structure was added above the imaging section to facilitate quantitative testing. Charge transfer efficiency in the frame transfer imager section was measured to exceed 0.99996/stage, and CTE in the horizontal SP^3 registers was measured to be 0.99991/stage at 1 Mpixel/sec and 0.9996/stage at 2 Mpixel/sec. Overall output amplifier sensitivity was measured to be $3.2\mu V/e^-$. Intrinsic read noise levels could not be assessed due to test station noise limitations. Matching of the output amplifier pair was measured to be better than 0.05%, with some chip to chip variation observed. (Mismatch can be corrected using an off-chip preamplifier prior to A/D conversion, if needed.)

Optical

Optical testing was performed at a 2 Mpixel/sec output rate (26-28 frames/sec). A 28-85 mm Nikon lens was used to focus an image onto the chip. Raw output from the chip was first buffered by a pre-amplifier, which through gain and offset correction, provided a 0-1.5 volt signal which was then inverted and sent to a raster scan converter for display. To demonstrate functionality, a photograph taken from the screen of the scan converter is shown in Fig. 7. The larger image is a portion of the complete 256 x 256 image captured (at a

26 Hz frame rate) by multiplexing the imager output through the upper SP^3 register and bypassing the pixel resequencing circuitry. The inset image is composed of one of the eight difference-encoded elements (center pixel minus neighboring diagonal pixel) of each 3 x 3 block yielding an 80 x 80 subsampled "edge" image also generated at a 26 Hz frame rate.
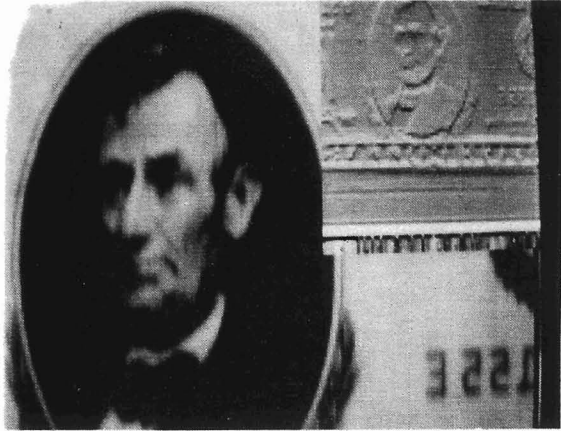

Fig. 7   Demonstration of IC functionality. Photograph taken from video monitor showing portion of image sensor output when reformatting circuitry is bypassed. Inset real-time "edge" image using on-chip reformatting circuitry is described in text. (Note - actual hierarchical code of Fig. 1 not amenable to display.)

CONCLUSION

In summary, a CCD image sensor has been integrated with additional charge-domain circuitry to enable pyramidal, differential output of the image data, thus simplifying downstream electronics and reducing system size, power and weight of lossless hierarchical compression hardware. The additional circuitry occupies an additional 2% of chip area and inconsequentially increases IC power dissipation. Signal integrity is not compromised by the structure since charge transfer efficiency is high and the number of transfers is not increased. A summary of IC characteristics is given in Table 1 and a chip photograph in Fig. 8.

ACKNOWLEDGMENTS

TABLE 1

IC CHARACTERISTICS AND PERFORMANCE SUMMARY

|	
Imager architecture	3-phase frame transfer
Number of pixels	256 x 256
Pixel size	$15\mu m \times 15\mu m$
Charge capacity	100,000 electrons
Chip area	5.4 mm x 9.4 mm
Imager area	3.9 mm x 3.9 mm
Processor area	$0.61\ mm^2$
CTE vertical register	0.99996
CTE SP^3 register	0.99991
Power dissipation (excluding drive circuitry)	$150\mu W$
Output amplifier sensitivity	$3.2\mu V/electron$
Package	68 pin leadless
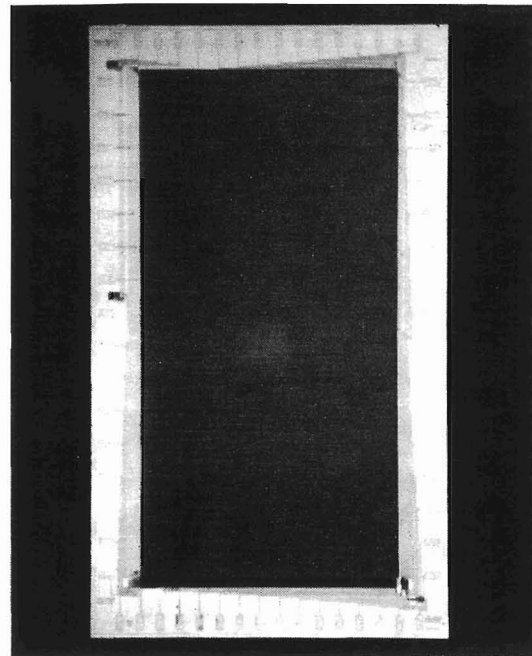
Fig. 8   Chip photograph.

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2. E.R. Fossum, "Wire transfer of Charge Packets Using a CCD-BBD Structure for Charge-Domain Signal Processing," to appear in IEEE Trans. Electron Devices, Feb. 1991.