Programmable multiresolution CMOS active pixel sensor

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ABSTRACT

CMOS active pixel sensors (APS) allow the flexibility of placing signal processing circuitry on the imaging focal plane. The multiresolution CMOS APS can perform block averaging on-chip to eliminate the off-chip software intensive image processing. This 128 x 128 APS array can be read out at any user-defined resolution by configuring a set of digital shift registers. The full resolution frame rate is 30 Hz with higher rates for all other image resolutions.

1. INTRODUCTION

For a variety of image processing tasks, such as biological vision modeling, stereo range finding, pattern recognition, target tracking, and progressive transmission of compressed images, it is desirable to have image data available at varying resolutions to increase processing speed and efficiency. The user can then obtain a frame of data at the lowest resolution necessary for the task at hand and eliminate unnecessary processing steps. The multiresolution image data is usually generated through an image pyramid approach, and has been used extensively in recent years [1-4]. Typically each image level is a low-pass filtered and down sampled version of the prior level, although block averaging and down sampling can also be used to generate the pyramid [5]. With the exception of a single non-programmable digital chip developed by Sarnoff [6], there is no existing or proposed hardware for the image pyramiding task. In software, construction of the multiresolution pyramid is often the most computationally intensive and time consuming portion of the image processing task. For applications where power consumption is of concern, the power consumed by the processor while performing this task can be critical. These problems become especially severe for image processing tasks performed on large format imagers (e.g. 1024 x 1024) that are read out at video rates (30 frames/second).

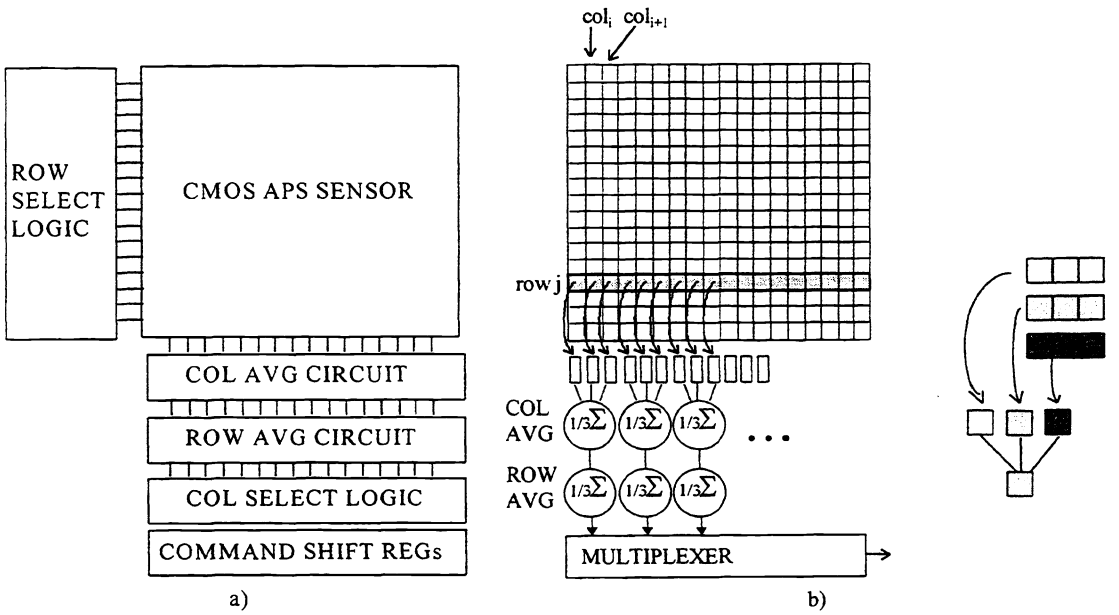

Figure 1. (a) Programmable multiresolution CMOS active pixel sensor architecture (b) example of column's functional configuration for 3x3 block averaging.

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CMOS active pixel sensor architectures (figure 1a) allow x-y addressability of the array for windows of interest and sparse sampling readout of the array[8]. Sparse sampling the array, for example, by reading out every fourth pixel of every fourth row reduces the amount of image data by a factor of 1/16 but introduces aliasing into the image. By block averaging regions of the array and reading out this average (figure 1b), data reduction is achieved without aliasing effects.

The multiresolution CMOS APS is a 128 x 128 photogate array that is programmable to readout any size n by n block of pixels or kernel. Each kernel value represents the average of all the pixel values in its region. Averaging is done in the column readout circuitry so that the average value is based on a full resolution image. Using the sensor's x-y addressability and programmable resolution, the user can readout a window of interest at various resolutions (figure 2). Details of the sensor operation are discussed in section 2. Section 3 presents the test results from the fabricated chip.

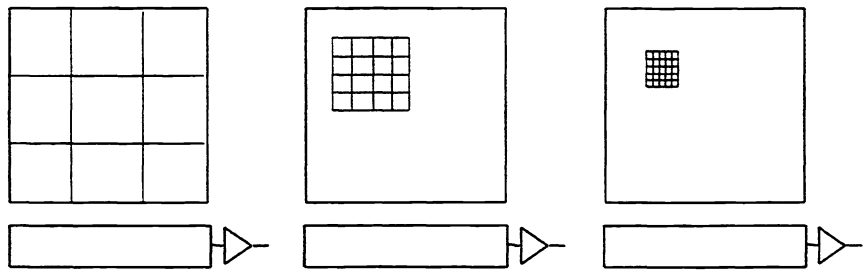


Figure 2. Sensor x-y addressability and multiresolution readout allows the user to zoom into an area of interest with increased resolution.

2. DESIGN AND OPERATION

2.1 Design Overview

The sensor contains a 128 x 128 photo-gate pixel array similar to [8]. At the bottom of each column in the array is a network of capacitors to store pixel reset and signal levels. The column circuitry also contains an additional capacitor and a set of switches to the adjacent column to perform averaging on any size square array of pixels called a kernel (rectangular kernels are also possible). Resolution of the sensor is set by the size of the kernel. Large kernels sizes are set for low resolution imaging requirements. The X-Y addressability of the sensor allows the user to zoom into areas of interest.

Figure 3 shows a block diagram of the sensor. A decoder at the side of the array selects a row of pixels for readout. Each pixel is controlled by a photo-gate signal enabling readout of integrated charge, a reset signal, and select signal to enable the buffered pixel data to drive the column output line. Column parallel circuitry at the bottom of the array samples the addressed row of pixel data simultaneously. The kernel size determines how a set of shift registers in the column circuits are configured. These shift registers control how the columns containing stored readout data are averaged and where the averaged row data is stored for subsequent processing. A second decoder at the bottom of the array controls which columns containing the processed data are readout. The sensor's differential output circuitry performs correlated double sampling(CDS) and double-delta sampling (DDS) to suppress pixel kTC noise, 1/f noise, and fixed pattern noise[9].

Row pixel data is read onto a column averaging capacitor with switches to its neighboring columns that are subsequently enabled resulting in averaged column data for that row (figure3). Averaged column data for that row is stored on a second bank of capacitors in one of the columns of the kernel. Data from successively readout rows is stored in each of the remaining columns in the kernel. Shift registers in the readout circuitry are configured according to kernel size to determine which switches are enabled to perform averaging and where the averaged column data is stored.

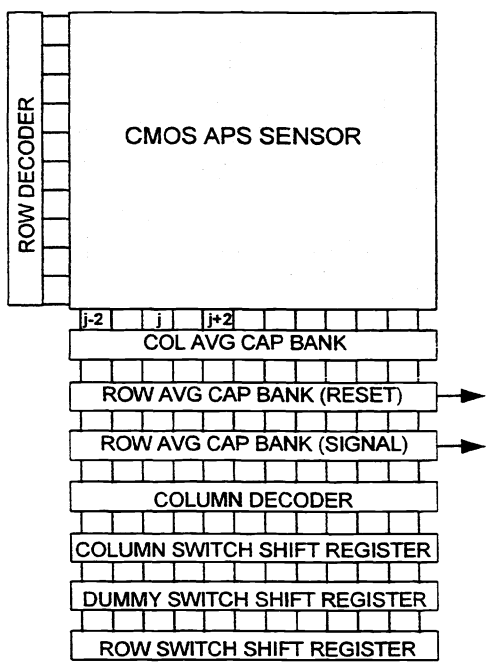


Figure 3. Multiresolution image sensor block diagram.

Once all n rows of the kernel are read, they are averaged by connecting the second bank of capacitors together and mixing the charge. A shift register configured to enable dummy switches to correct for switch feedthrough effects is also included. Both reset and signal levels are processed for a kernel so that correlated double sampling and double-delta sampling operations can be performed.

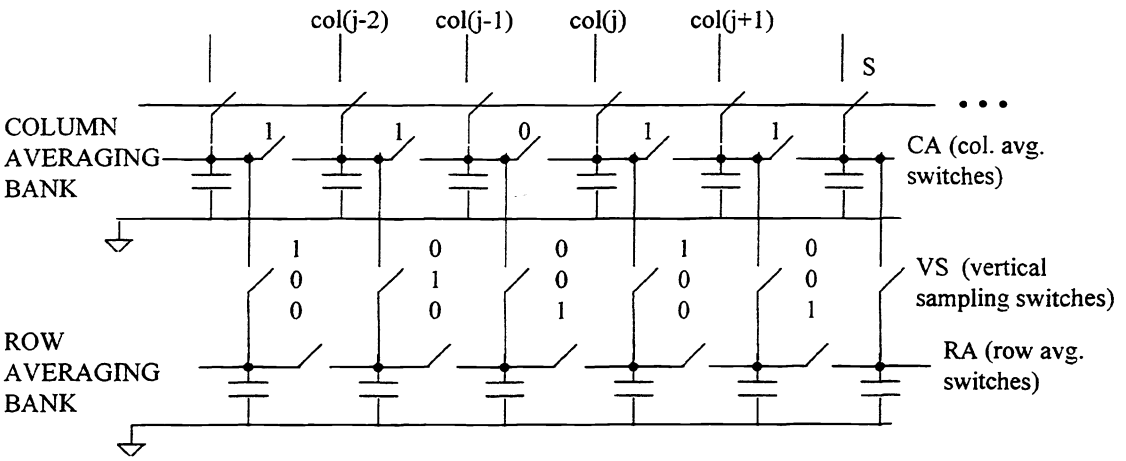


Figure 4. Ideal switch and capacitor model for 6 columns configured for 3x3 block averaging.

Operation will be illustrated by stepping through the sequence for 3 x 3 block (kernel) averaging (figure 4). In this case, every third column average (CA) switch is open (i.e. deselected, denoted by bit 0 over the switch), while the other switches are closed (i.e. selected, denoted by bit 1 over the switch). Pixel signals are sampled onto the column averaging capacitors by globally pulsing (closing) the signal select switches (S). Charge redistributes such that the voltage on each capacitor in each block of three capacitors is the same:

$$V_{i\_ker} = 1/n \sum_{k=1}^{n} V_{j-k}$$

where n is the horizontal size (number of columns) of the block average (kernel), V_{j-k} the pixel voltage value of the (j-k)th column, and V_{i_ker} is the average value for the ith row in the kernel. These kernel row averages are then sampled onto the first capacitor in the n-capacitor block of the row averaging bank of capacitors. Column averaging is repeated with the next pixel row (i+1) and these new $V_{(i+1)\_ker}$ kernel averages are sampled onto the second capacitor in the n-capacitor blocks of the row averaging bank of capacitors. The process is repeated until all n rows have been processed and n samples have been collected in n adjacent capacitors in the row averaging bank. The temporal switching sequence(digital pattern) is shown for the 3x3 kernel case (figure 4). After the n-samples (V_i, V_{i+1},...$V_{i+(n-1)}$) have been collected, charge is redistributed by pulsing the row averaging (RA) switches with the same pattern used for the column averaging switches, resulting in the final block average:

$$V_{ker} = \frac{1}{2} \sum_{i=1}^{m} V_{i\_ker}$$

where m is the vertical size (number of rows) in the kernel. The constant factor of 1/2 arises from charge sharing between the column and row averaging capacitors when the column average is sampled onto the row averaging capacitor. Thus for the first 3x3 kernel:

$$V_{ker0} = 1/2\{1/3[1/3(V_{0,0} + V_{0,1} + V_{0,2}) + 1/3(V_{1,0} + V_{1,1} + V_{1,2}) + 1/3(V_{2,0} + V_{2,1} + V_{2,2})]\}$$

These kernel values are then scanned out of the array by reading out every nth capacitor in the row average bank. The row averaging capacitors are then reset (circuitry not shown) and the process is repeated to generate the next row of kernels.

Note that in the configuration described above, kernels must be either square or rectangular, where the number of rows must be less than or equal to the number of columns.

2.2 Column processing circuitry

Shown in figure 5 is the column parallel circuitry for 3 columns. It shows the sample and hold capacitors for both pixel reset and signal values. The second bank of capacitors is for storing the reset level after its been averaged on the first bank of capacitors. The third bank is for storing the averaged signal level. The kernel reset switch to ground is shown as well as the column buffer amplifier for generating VoutR and VoutS. The buffer amplifier is only enabled when the column is selected for readout.

The digital patterns shown are an example of the timing for a 3 x 3 kernel. They are generated by gating the output of the configuration shift registers and the timing signals shown in figure 5. The global timing signals are CA (enable column averaging), RA (enable row averaging), VS (sample signal onto row averaging capacitor), and VR (sample reset onto row averaging capacitor). Each of these global signals is gated with the output of one of the two configuration shift registers. The CA and RA signal are gated with the output of the same shift register (CARA shift register). The VS and VR signals are gated with the output of the second shift register (VSVR shift register).

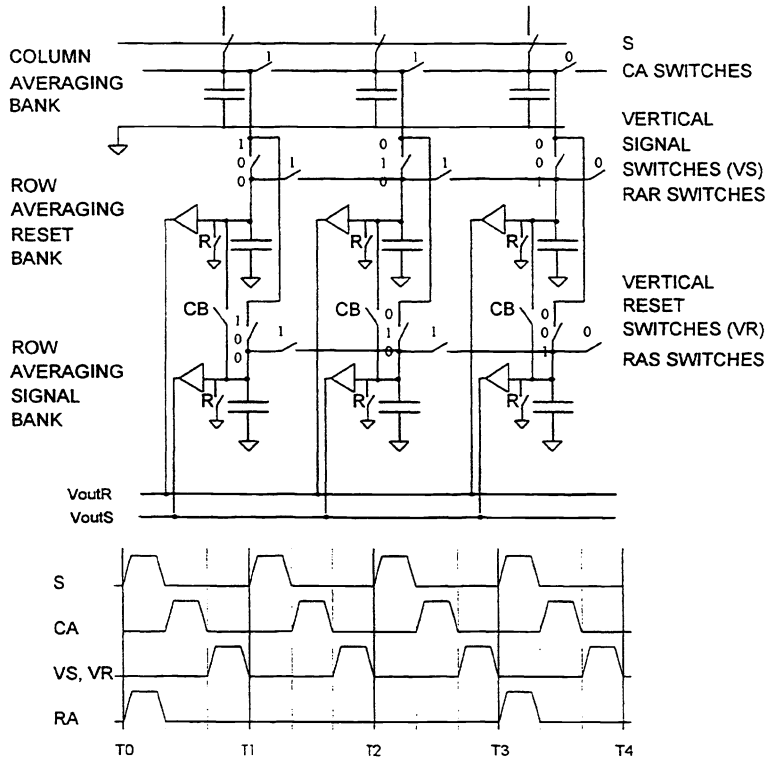


Figure 5. Multiresolution column processing circuitry for 3 columns.

The transistor level schematic of the column circuit is shown in figure 6. The signals CA_i, RA_i, VS_i, and VR_i are the outputs from the corresponding global signals gated with the shift register output bit for that column. The buffer amplifier is a p channel source follower. The CB signal is part of the double delta sampling readout scheme as reported in [9] used to reduce column fixed pattern noise.

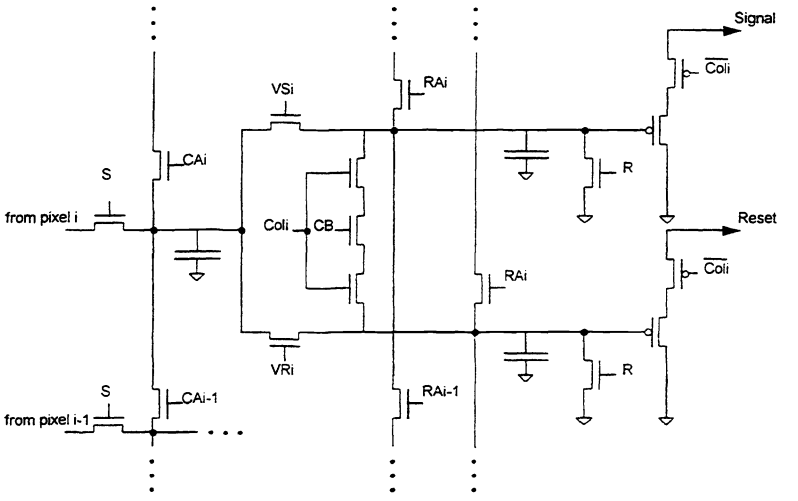


Figure 6. Transistor level schematic of column circuit. Capacitors are poly-diffusion linear capacitors.

3. EXPERIMENTAL RESULTS

The sensor was fabricated through MOSIS in the HP 1.2 μm n-well CMOS process. The 128 x 128 photogate sensor has a pixel pitch of 24 μm. The total chip size is 4.8 mm x 6.6 mm (figure 10). Table 1 lists some of the sensor characteristics for full resolution operation.

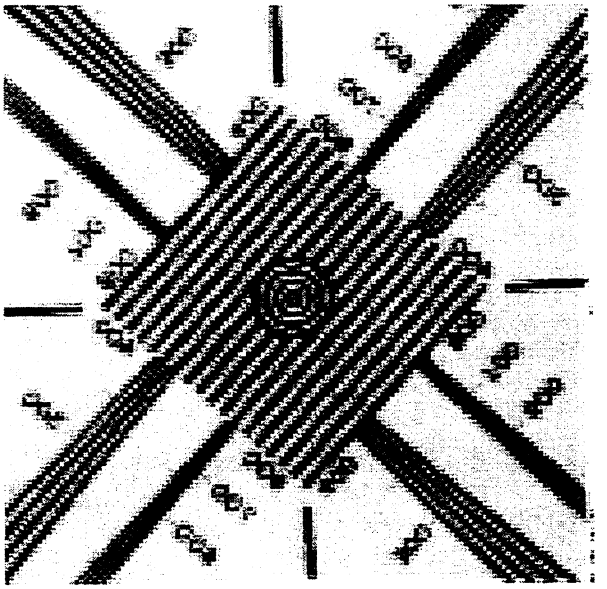


Figure 7. Sensor's full resolution image (128x128)

Figure 7 shows a full resolution image of a test pattern used to demonstrate the sensor's block averaging. Figure 8b shows the same image for the sensor operating in a sub-sampling mode where every fourth column of every fourth row is read with no averaging. Because the test target contains relatively high spatial frequency patterns, the sub-sampled image produces

dramatic aliasing. Comparing this 32x32 image with the full resolution 128x128 image shows the appearance of both fewer stripes and diagonal stripes rather than parallel stripes relative to the edge of the square. The 32x32 image with 4x4 kernel averaging (figure 8a) reduces this effect because the pixel array is read at full resolution and subsequently averaged.

To measure how well the multiresolution sensor performs averaging, a test pattern containing a black and white stripe was imaged. The black white edge (defocussed) was positioned so that half the pixels in the kernels on the edge are black. Thus, the sensor output of the kernels aligned on top of the edge ideally should equal one-half of the difference between the totally white and black pixels. To measure the individual pixels in the kernel, subsampled data was first measured. Based on this subsampled raw image data, block averages were calculated for the pattern. This data was compared to the multiresolution sensor's output at different kernel sizes.

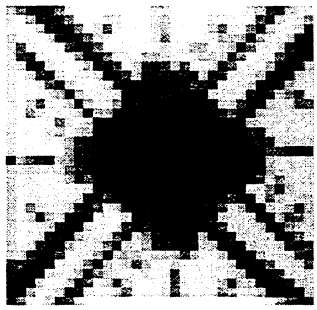


Figure 8a. 4x4 block averaged image

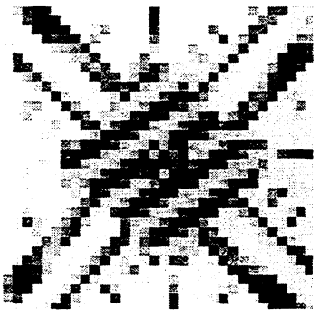


Figure 8b. 1/4 subsampled image (no averaging)

An example of the sensor's output for one of the rows is shown in figure 9 where the sensor's full resolution row data and 4x4 kernel output data are shown. The row shown (figure 9a) is 1 of 4 rows used to calculate the average from the full resolution image for comparison with the on-chip 4x4 kernel average. Figure 9b illustrates the 4x4 kernel producing an output voltage at the average value of the four pixels at the black-white stripe edge (pixels in columns 65-68).

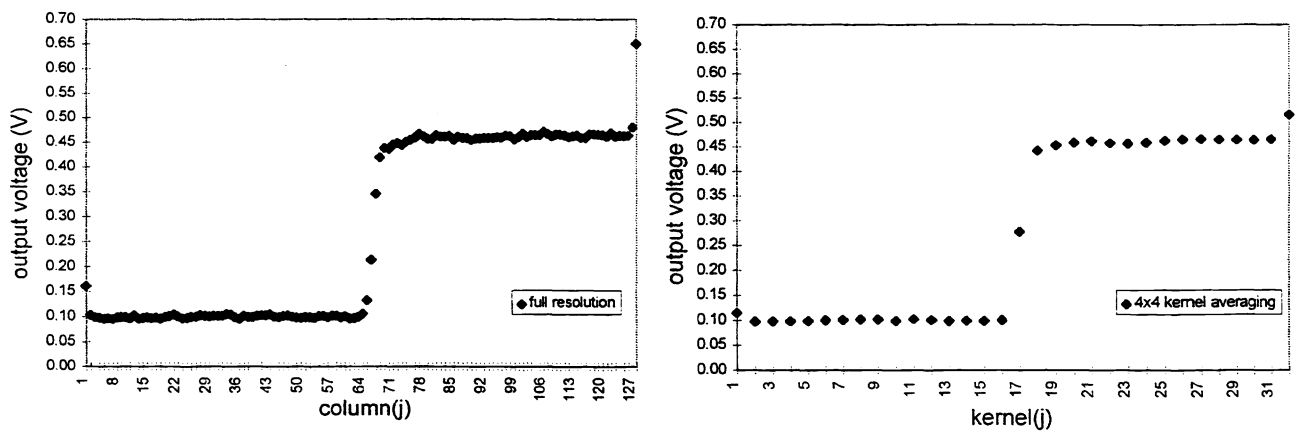


Figure 9. a) Full resolution sensor output for one row pixels b) 4x4 kernel output from same image.

Image data for 2x2, 4x4, and 8x8 kernel sizes were acquired for this test pattern. Analysis of kernel data for the entire frame versus the off-chip block average data based on full resolution data shows that the sensor is accurate to within 2% of the ideal average value. The use of dummy switches for switch feedthrough compensation did not have a significant effect of the averaging accuracy.

Table 1 lists the results from sensor characterization tests similar to those described in [9]. The sensor exhibited very low fixed pattern noise and dissipated very little power. Overhead for performing on-chip block averaging is a small percentage of the sensor readout time and total power consumption. For lower resolutions the frame rate increase above 30 Hz is approximately proportional to the number of pixels, n x n, in the kernel.

Array Size	128x128
Pixel Size	24 μm
Technology	1.2 μm n-well CMOS (HP)
Saturation level Vsat	1200 mV
Conversion gain	8 μV/e^-
Read Noise (full resolution)	116 μV rms (15 e^- rms)
Dynamic Range	80 dB
Power@30Hz frame rate Vdd=5V, Vsat = 1200mV	5 mW
Vdd=4V, Vsat = 500mV	1.25 mW
Fixed Pattern Noise	3 mV p-p (0.25% of saturation)
Kernel averaging error	≤ 2 %

Table 1. Sensor Characteristics

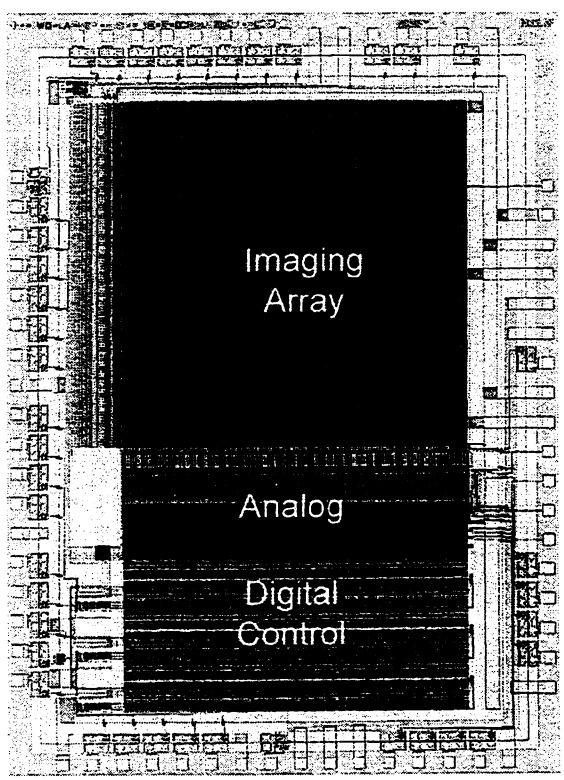
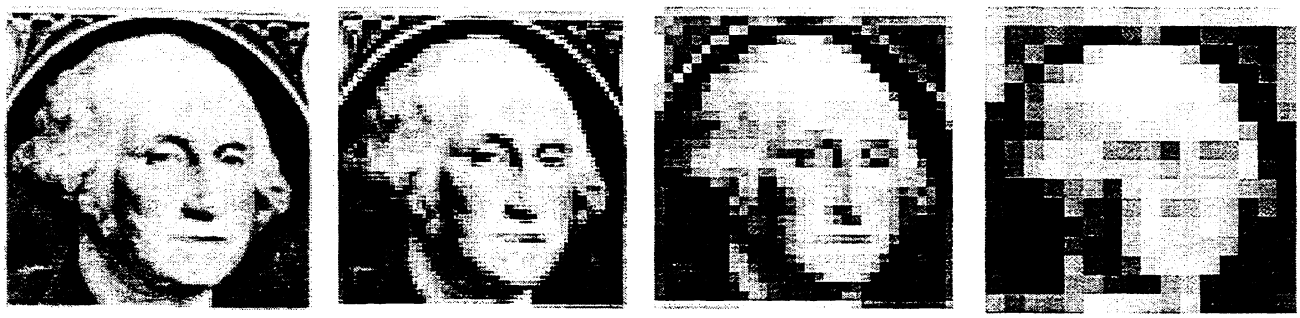


Figure 10. Photograph of completed Programmable Multiresolution APS (128x128 array)

4. SUMMARY

The multiresolution sensor demonstrates the versatility of CMOS active pixel image sensors. On-chip column circuitry performs block averaging using programmable kernel sizes. The images of George Washington in figure 11 from a dollar bill

illustrate the sensor's multiresolution ability. Shown are images at full resolution, 2x2, 4x4, and 8x8 kernel configurations. The accuracy of averaging is within 2% of the average calculated from full resolution image data. With power consumption as low as 5 mW and 30 Hz minimum frame rate operation for any resolution, this programmable multiresolution sensor can significantly reduce camera system complexity and power where multiresolution image processing is required.



a) b) c) d)

Figure 11. Programmable multiresolution sensor output for a) full resolution, b) 2x2, c) 4x4, and d) 8x8 kernel configurations.

5. ACKNOWLEDGMENTS

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