# Noise and electrical characteristics below 10 K of small CHFET circuits and discrete devices

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## ABSTRACT

This paper discusses the latest results of a continuing study of the properties of the complementary heterojunction field-effect transistor (CHFET) at 4 K. The electrical characteristics, including the gate leakage current and the subthreshold transconductance, and the input-referred noise voltage for a new lot of discrete CHFETs is presented and discussed. It is shown that the inclusion of a sidewall spacer on the gate substantially reduced the gate leakage current, as compared to a previous lot without the sidewall spacer. The input-referred noise is approximately the same order of magnitude as previous devices, on the order of 1 $\mu V/\sqrt{Hz}$ at 10 Hz for subthreshold operation. The noise is relatively unaffected by changes in the bias current and drain voltage, but decreases with increasing device size, and is increased by the inclusion of dopants in the channel region. Several simple multiplexer circuits using CHFETs are presented, and the open-loop transfer curve of a multiplexed single gain stage operational amplifier at 4 K is shown.

## 1. INTRODUCTION

The design of systems that include detector focal plane arrays operating at temperatures below 10 K would be greatly simplified by the availability of readout electronics that can operate at the detector temperature. Otherwise, the designer is forced to isolate the electronics in a warmer compartment and run a wire for each sensor in the array from the focal plane cold head to the warmer electronics compartment. These wires carry heat from the electronics compartment to the cold head, increasing the load on the cold head refrigerator or cryogen supply. The wires are also susceptible to cross-talk and to the pickup of noise through electromagnetic induction or microphonics. As the array size increases, these problems become more acute, making this "brute force" method increasingly less attractive. By contrast, if the electronics are placed directly on the cold head with the sensor array, these problems are reduced or eliminated. The sensor array can be bump bonded directly to the associated array of electronics, which reduces the electrical connection between the sensor and electronics to micron lengths, making electromagnetic and microphonic noise pickup negligible. Also, since the electronics and sensor are at the same temperature, these connections do not contribute to the heat load. The electronics will amplify and multiplex the signals from the sensor array. This results in fewer leads coming off of the cold head for reduced heat conduction, and the amplified signals are less susceptible to noise.

The major technical challenge involved in building very low temperature electronics is due to the phenomenon of carrier "freeze-out." For semiconductor material that is not heavily doped, it requires a small but finite energy to liberate carriers from the dopant atoms so that they can travel freely through the semiconductor and contribute to conduction. At sufficiently low temperatures, the carriers lack the required energy and are recaptured by the dopant atoms or other traps. This causes the conductivity of the semiconductor to fall sharply as the temperature is lowered, which results in degraded performance, or complete device failure, of any transistor that is made of that semiconductor. In addition, the random trapping and de-trapping of carriers causes the conductivity to randomly vary with time, which is the major source of noise.

By far the most popular material system for low power electronics has been silicon complementary metal-oxide-semiconductor (CMOS) technology. However, silicon is poorly suited to very low temperature applications. The ionization energies for free carriers in silicon is relatively high. As a result, silicon freezes-out at a relatively high temperature, and it requires very high doping levels to make silicon degenerate. Conventional silicon bipolar transistors cease to function below


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about 50 K. CMOS transistors can operate to somewhat lower temperatures, but conventional CMOS still exhibits excessive noise and current-voltage anomalies such as kinks and hysteresis below about 20 K. The state-of-the-art CMOS optimized for low temperatures has demonstrated anomaly-free performance and moderate noise levels down to and slightly below 10 K.[1] Despite this advance, there is still no silicon technology suitable for operation at and below 4 K.

By contrast, GaAs-based transistors exhibit superior performance at low temperatures. The ionization energy for electrons is much smaller that for silicon, so it freezes-out at a much lower temperature, and becomes degenerate at much lower doping concentrations. In addition, epitaxial growth technology is highly advanced for GaAs-based structures which allows the growth of very pure semiconductor with few background impurities that can act as traps. It also allows the growth of heterojunctions that can separate the carrier charge from traps and dopants. Several groups have begun to explore GaAs-based transistors for low temperature readout electronics applications.[2-6] For example, R. Kirschman et. al., have studied commercial and foundry GaAs junction field-effect transistors (JFETs) and metal-Schottky field-effect transistors (MESFETs) at 4 K.[2] Also, Kozlowski et. al., have designed GaAs-based circuits for low temperature readouts.[3]

## 2. PREVIOUS STUDY OF THE CHFET

As part of the NASA Sensor Electronics Program, JPL has been studying GaAs-based electronics for readout electronics applications in the 2-4 K temperature range. This has included an investigation of the low-temperature properties of a type of CMOS-like GaAs-based transistor called the complementary heterojunction field-effect transistor (CHFET). The CHFET was developed by Honeywell for high-speed, room-temperature digital applications.[7] It has several features, however, that indicate that it might be suitable for very-low temperature operation.

A cross-section of the CHFET is shown in Fig. 1. Starting on a semi-insulating GaAs substrate, molecular beam epitaxy (MBE) is used to grow a GaAs buffer layer, an InGaAs channel, a high aluminum mole-fraction AlGaAs layer, and a thin GaAs cap layer for surface passivation. A WSi gate is deposited and serves to make the source and drain self-aligned. The entire structure can be undoped except for the implanted source and drain which are degenerately doped. These implants can be either n-type or p-type allowing complementary transistor circuits. The device operates in enhancement mode in a manner analogous to that of silicon CMOS, with the AlGaAs layer playing the role of the oxide. A gate voltage draws electrons or holes into the channel where they are confined vertically by the AlGaAs dielectric. The carriers move laterally, and are collected by the drain. The gate voltage modulates the channel charge density above threshold, and the channel potential below threshold.

The availability of complementary devices is extremely useful in the design of low power electronics. The fact that the structure can be made so that each region of the device is either degenerately doped or undoped makes the device immune to freeze-out. Because the carriers are confined by the heterojunction barrier to a channel that can be undoped, the carriers can have very high mobility, and will see few impurities, traps, or surface states to scatter or trap them. Together these facts indicate that the CHFET offers a good deal of promise as a low-power, low-noise device functional at very low temperatures.

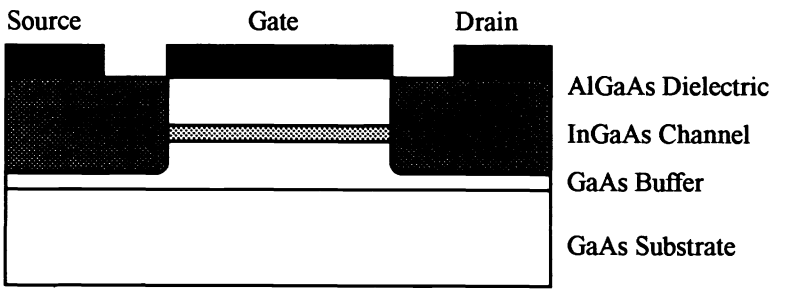



Fig. 1: A cross-section of the complementary heterojunction field effect transistor (CHFET). The entire structure can be undoped except for the source and drain implants, which are degenerately doped.

A previous study has shown the CHFET to be fully functional at 4 K, exhibiting normal subthreshold and above-threshold characteristics, including the proper voltage, length, and width dependencies.[8] However, there are still issues that need to be addressed before the CHFET is ready for application in very low temperature readout electronics. Because the AlGaAs

dielectric presents a much lower barrier to carrier leakage than the oxide in silicon CMOS, the gate leakage current of the CHFET is a major concern. The device noise is also of great importance, since readout electronics for scientific imagers typically work with very small signals. A study of the voltage and temperature dependence of the gate leakage current showed that the gate current was due to a combination of several different phenomena, including field-emission, thermionic emission, and ohmic conduction, each of which was dominant in a particular range of voltage and temperature.[9] The results from these previous studies are summarized in Fig. 2 which shows the above threshold transistor curves for an n-channel and p-channel device, and in Fig. 3 which shows the subthreshold drain current and gate current as a function of gate voltage.

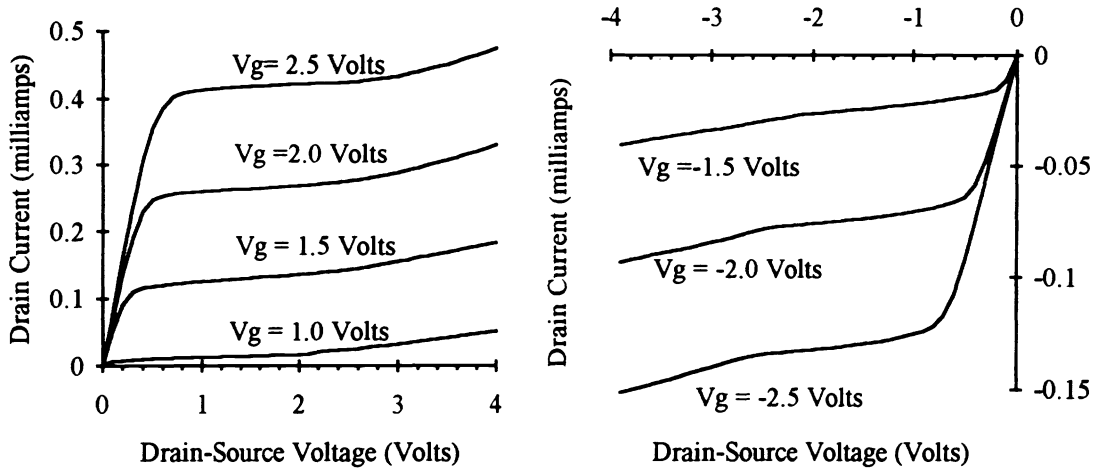



Fig. 2: The transistor curves for n-channel and p-channel CHFETs

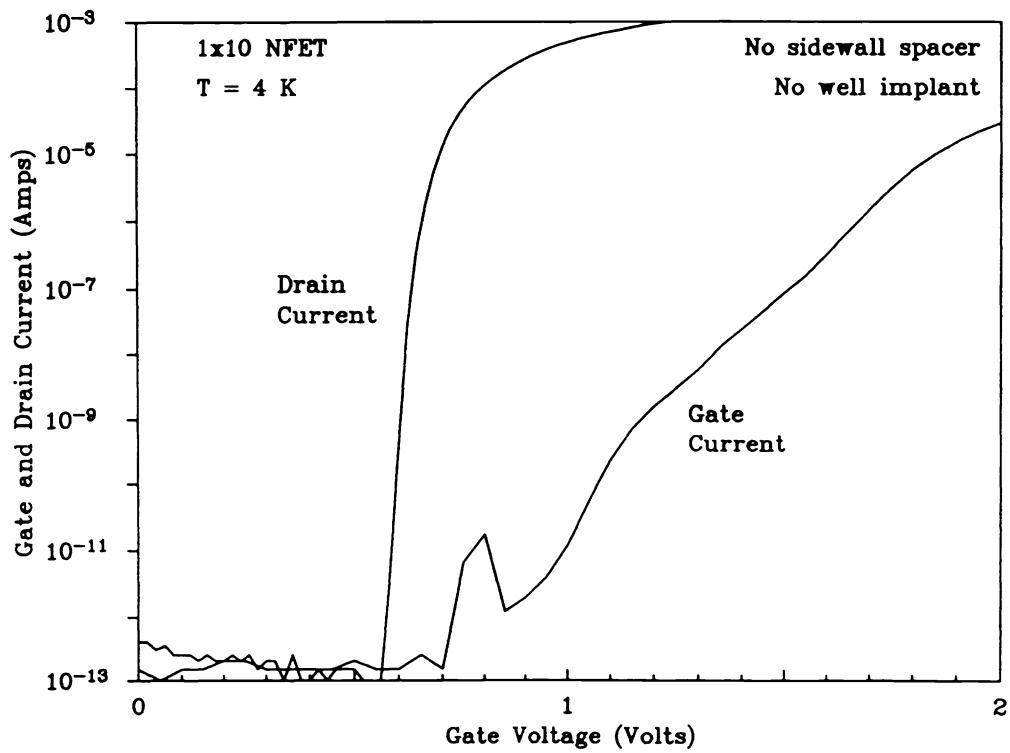



Fig. 3: The subthreshold drain current and gate current for a CHFET with low gate leakage. The data was measured with an HP4145B semiconductor parameter analyzer; the sensitivity of the HP4145B is $10^{-12}$ amps.

## 3. DATA FOR THE NEW CHFET TRANSISTORS AND CIRCUITS

A second lot of devices was fabricated by Honeywell to facilitate a systematic study of the gate leakage current and noise voltage. Eleven n-channel and eleven p-channel discrete transistors were laid out on each chip, with sizes ranging from 1 μm x 3 μm (length x width) to 50 μm x 50 μm. Other parameter variations included the AlGaAs thickness and aluminum mole fraction, the GaAs buffer layer thickness, the inclusion of a gate sidewall spacer, and variations of the sidewall implant. In addition to discrete transistors, several CHFET multiplexer circuits were also fabricated.

In the fabrication of devices that included a gate sidewall spacer, an implant was done in the region adjacent to the gate using the bare gate as a mask. Sidewall spacers were then added to the edges of the gate and the usual source and drain implants were done, so the doping is controllable in the sidewall region between the source or drain and the gate edge, independent of the source-drain doping. The gate leakage was examined for devices with heavy, moderate, and light sidewall region doping. Some of the devices also received a very light well implant. This was a p-type implant for n-channel devices, and was n-type for p-channel devices. All of the tested devices used channel doping included during the epitaxial growth to make the turn-on voltages of the n-channel and p-channel transistors more symmetric.

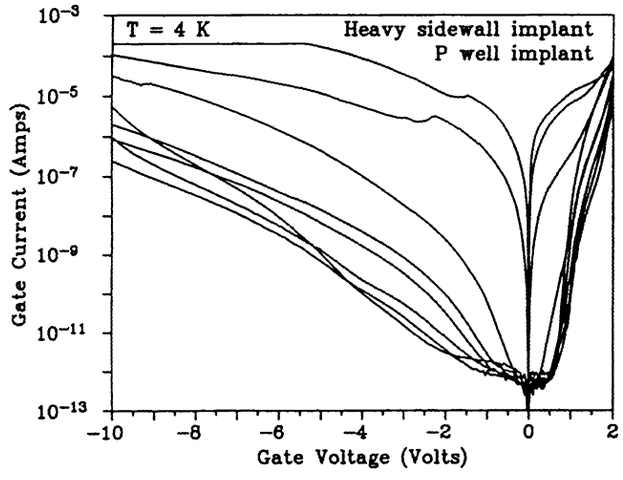
## 4. GATE LEAKAGE FOR THE NEW DEVICES

The gate leakage current with the source and drain grounded was measured using an HP4145B semiconductor parameter analyzer for n-channel CHFETs with p-well implant and with heavy, moderate, and light sidewall region implants. The current was also measured for a device with a moderate sidewall region implant and no well implant. These devices were all fabricated on the same wafer: the wafer was divided into quadrants, each of which received a different implant. The AlGaAs dielectric layer thickness was 250 Å for these devices, and the aluminum mole fraction was 0.75. The absolute value of the gate current for both forward and reverse gate voltages is shown in Fig. 4. The data for the same devices but for forward gate voltage only on a more sensitive scale in shown in Fig. 5. The different curves on each plot are for different size devices fabricated together in each quadrant. In Fig. 6 the gate current is compared for a typical CHFET from the old lot that did not include a sidewall spacer, and for a new device that included a sidewall spacer and used light sidewall region doping.

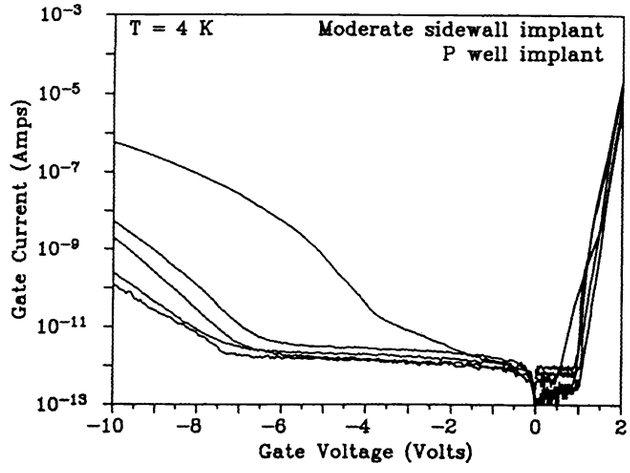
As can be seen in Figs. 4, 5, and 6, the gate current is strongly affected by the doping in the sidewall region. Several of the devices with the heavy sidewall region doping have currents in excess of a microamp at voltages of less than a quarter of a volt applied in either polarity. By contrast, the gate current of the devices with the light sidewall region doping does not reach 1 pA (which is the sensitivity limit of the HP4145B semiconductor parameter analyzer with which the current was measured) until a forward voltage of about 1 V or a reverse voltage of -6.5 V. The samples with a moderately doped sidewall region showed gate leakage comparable to, but slightly worse than the lightly doped device. The gate current reaches 1 pA at about a forward voltage of 0.95 V and a reverse voltage of -5.5 V. The addition of the p-well implant for devices with moderate sidewall region doping decreases the reverse leakage current slightly, but has no noticeable effect on the forward leakage current. The p-well implant increases the turn-on voltage by about 0.1 V.

The gate leakage current for any particular doping conditions does not show any reasonable dependence on the device size, an effect that was also seen on the old lot of devices. The leakage for various device tends to cluster, with about 80% of the devices on any chip showing approximately the same behavior, and with 20% of the devices as outliers, with much higher current levels. This may be due to the fact that the current is dominated by the details of the gate edge shape, or by defects near the gate edge. In any case, the current does not show a regular width or area dependence.

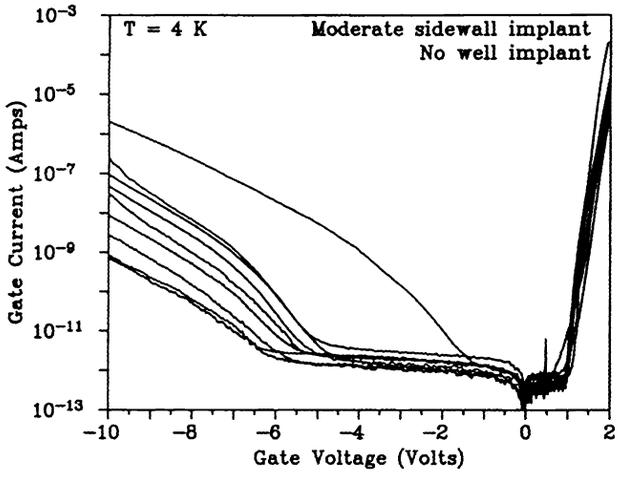
While the details of the gate leakage current mechanism are still not fully understood, it is clear that the inclusion of a sidewall spacer helped enormously. As seen in Fig. 6, when the old device without a sidewall spacer is bias to a subthreshold current of around 10 nA, which is a reasonable design value for bias currents in low-power analog readout circuits, the gate current is on the order of $10^{-12}$ amps. For the same drain current in the device with the sidewall spacer and with light sidewall region doping, the current is below the sensitivity of the HP4145B and the electrometer. If an extrapolation from the measured data is accurate, the gate current is less than $10^{-14}$ amps, which is an improvement of two orders of magnitude.



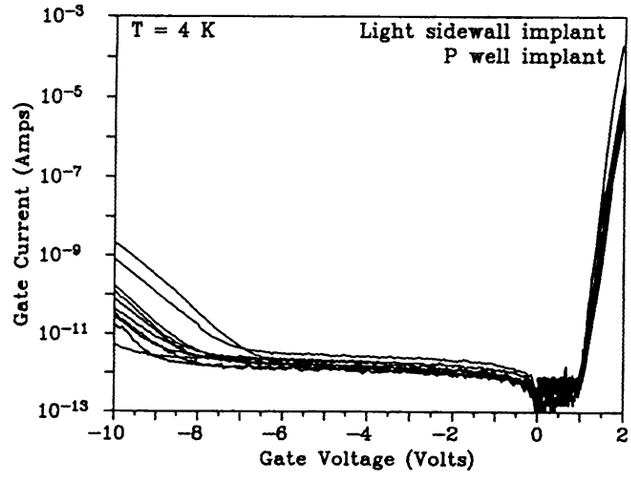

a) Heavy sidewall region doping with p-well implant




b) Moderate sidewall region doping with p-well implant

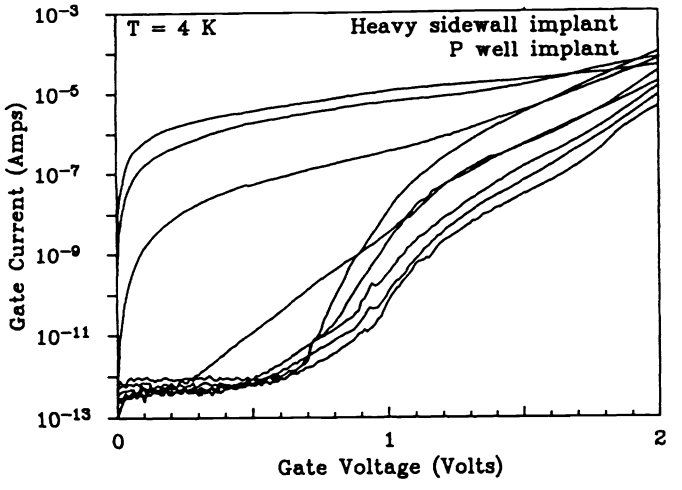



c) Moderate sidewall region doping with no well implant

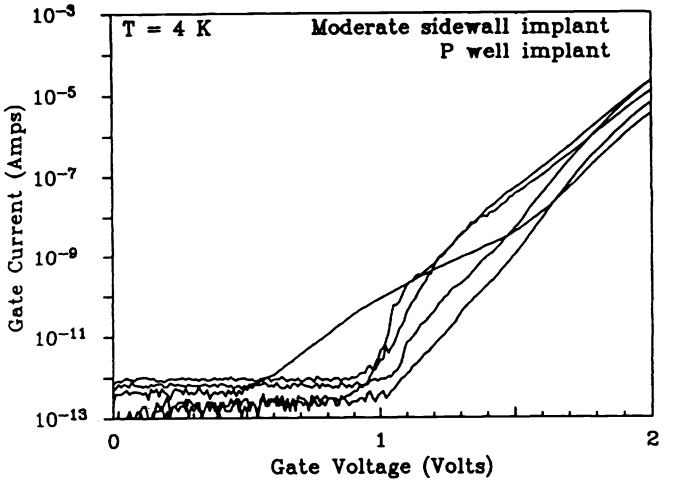



d) Light sidewall region doping with p-well implant

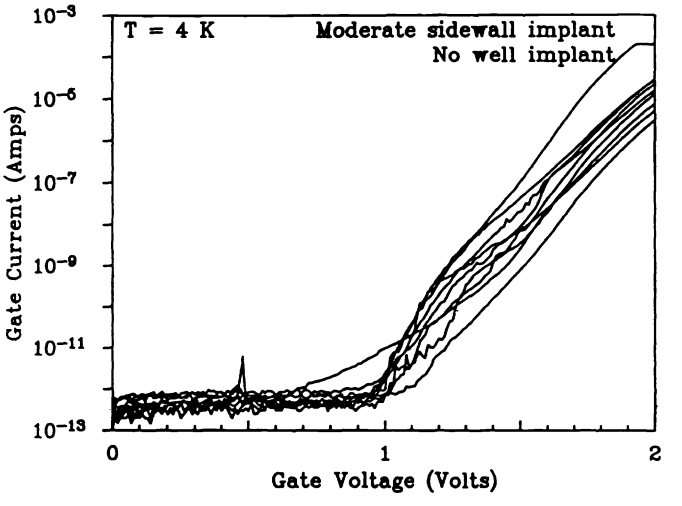
Fig. 4: The forward and reverse gate leakage currents for devices with heavy, moderate, and light sidewall region doping and with and without a p-well implant. The gate current was measured with the source and drain grounded, using an HP4145B semiconductor parameter analyzer. The sensitivity of the HP4145B is 1 pA.



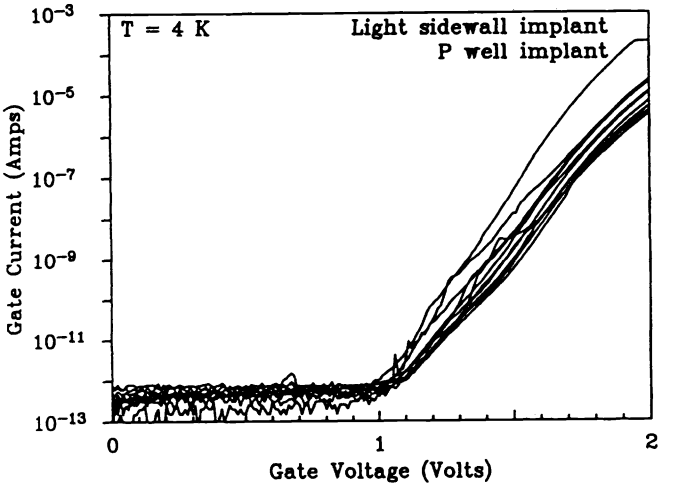

a) Heavy sidewall region doping with p-well implant




b) Moderate sidewall region doping with p-well implant

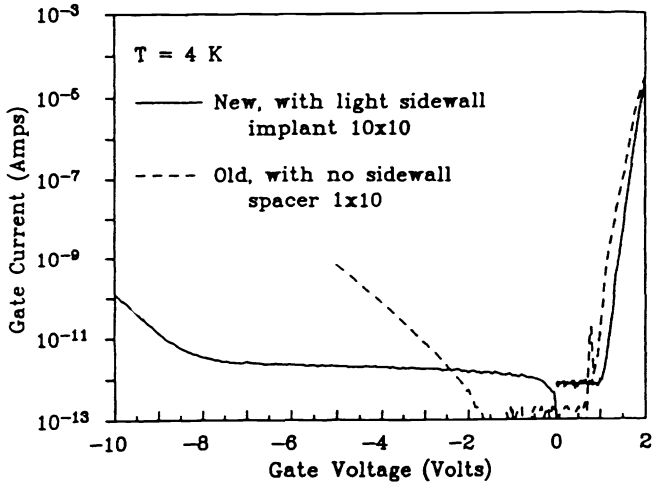



c) Moderate sidewall region doping with no well implant

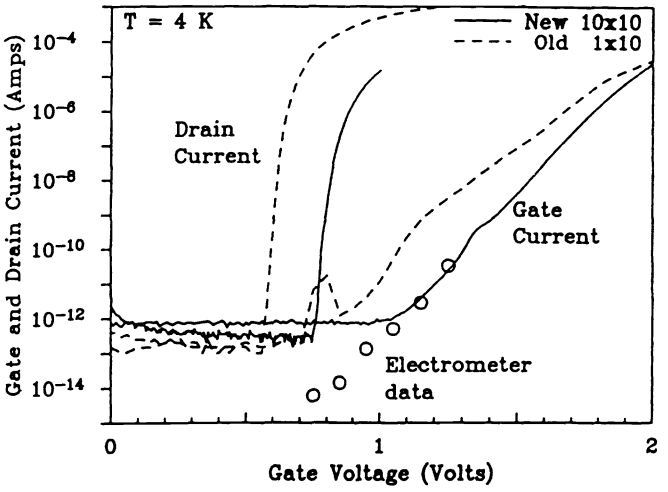



d) Light sidewall region doping with p-well implant

Fig. 5: The forward gate leakage currents for devices with heavy, moderate, and light sidewall region doping and with and without a p-well implant. The gate current was measured with the source and drain grounded, using an HP4145B semiconductor parameter analyzer. The sensitivity of the HP4145B is 1 pA.




a) Forward and reverse gate leakage.




b) Forward gate leakage current, subthreshold current and electrometer data.

Fig. 6: A comparison of the gate leakage of a typical device of the old lot of CHFETs which did not use a gate sidewall spacer (plotted using a dotted line) and a device from the new lot that includes a gate sidewall spacer with the lightest sidewall region doping (plotted using a solid line). The data was measured with an HP4145B semiconductor parameter analyzer, which has a sensitivity of 1 pA. Included in b) is the subthreshold drain current for the old and new device, and data taken with an electrometer, extending below the sensitivity of the HP4145B. The gate current for a old device biased at subthreshold operation is on the order of $10^{-12}$ amps. Extrapolating on the basis of the electrometer data, the gate current for the new device with the sidewall spacer biased at subthreshold operation is on the order of $10^{-15}$ amps.

## 5. THE NOISE VOLTAGE FOR THE NEW DEVICES

The input-referred noise for the new devices was measured at various temperatures, drain currents, and drain voltages, and for devices of different sizes and with different doping conditions. Previously, the output current noise was measured using a differential amplifier across a drain resistor. The transconductance was measured by injecting a small, known signal onto the gate and measuring the change in current. The input-referred voltage noise was then calculated by dividing the output current noise by the transconductance. In the new measurements, a feedback circuit was used that directly puts out an amplified version of the input-referred noise. The old and new circuits are shown in Fig. 7.

In Fig. 8, a comparison is made of the noise in a typical old device to that of a comparably sized new device. Neither device used a p-well implant. The noise in both devices is similar, on the order of 1 $\mu V/\sqrt{Hz}$ at 100 Hz. The effect of including a p-well implant is also shown in Fig. 8. As expected, the presence of additional dopants increases the noise.

The effect of the device size, temperature, drain bias current, and source-drain voltage on the noise is shown in Fig. 9. For this lot of devices, the device size had a strong effect. The device noise decreases with increasing device size, as is normally the case. The effect of the temperature, drain bias current, and drain-source voltage appears to be negligible. Some of the devices show a peak at 50 Hz in the noise spectrum, the cause of this is under investigation.

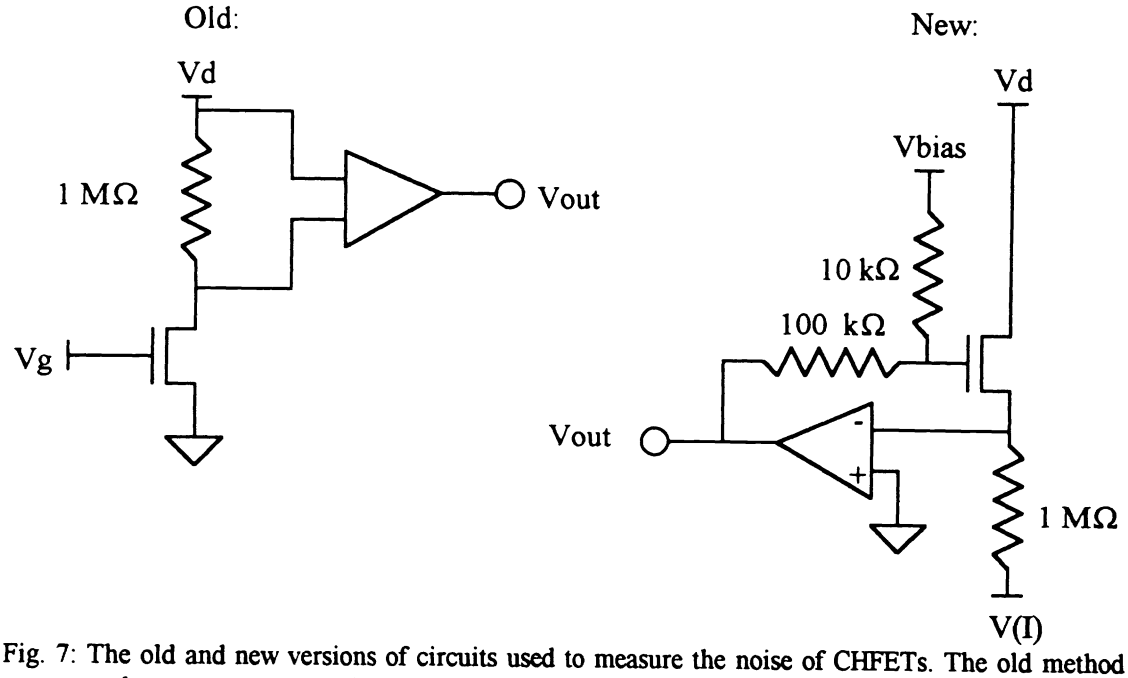
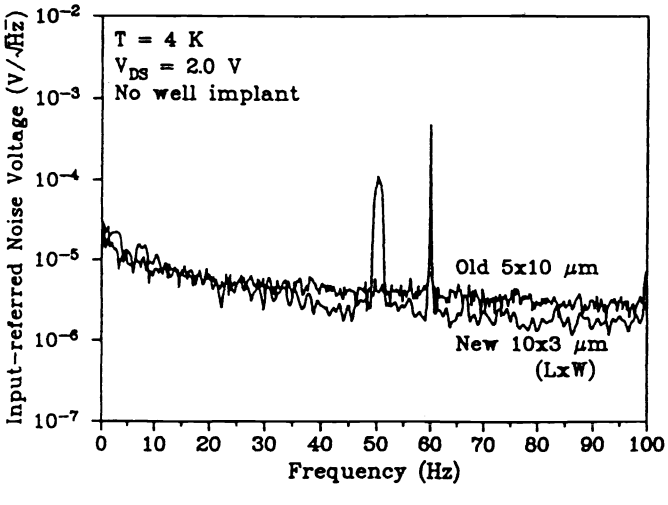
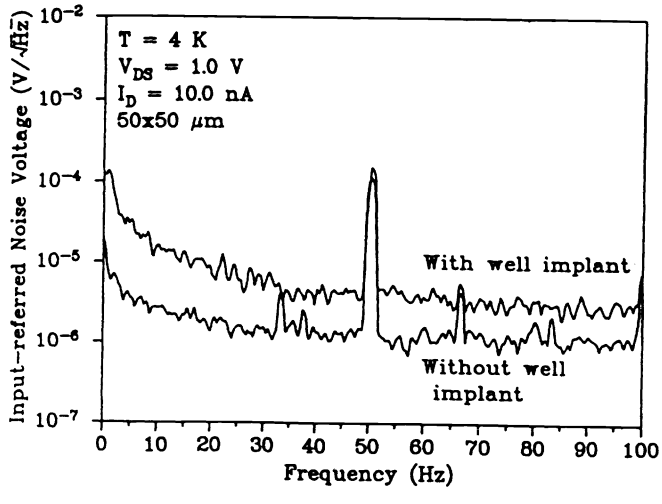



Fig. 7: The old and new versions of circuits used to measure the noise of CHFETs. The old method measures the output current noise, and the input-referred voltage noise must be calculated, using the transconductance. The new circuit directly provides an amplified version of the input-referred voltage noise.

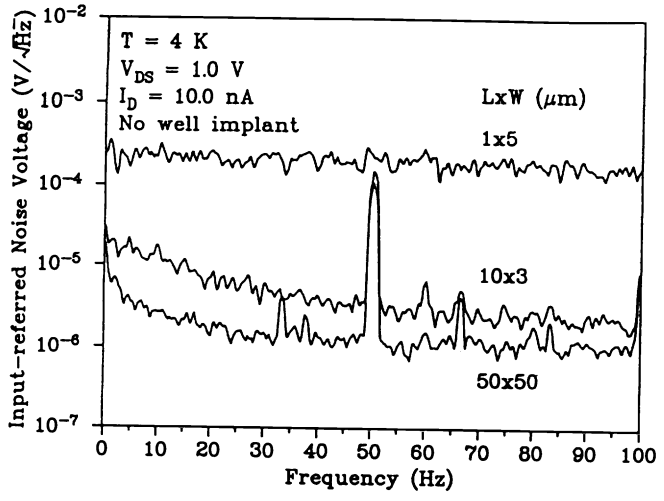



a) Noise for old and new devices.

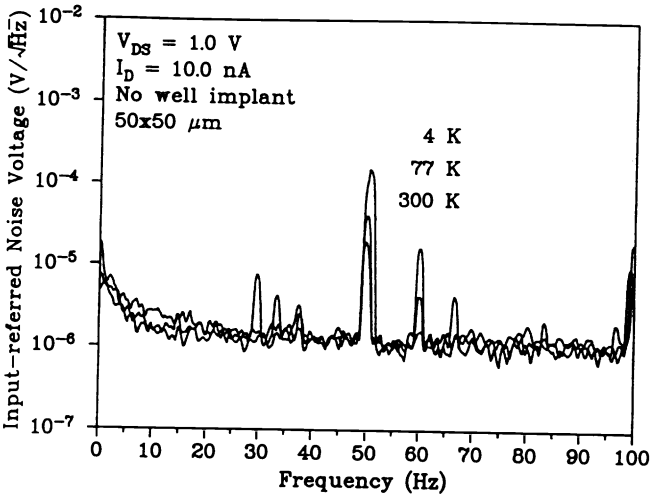



b) Noise for devices with and without a p-well implant.

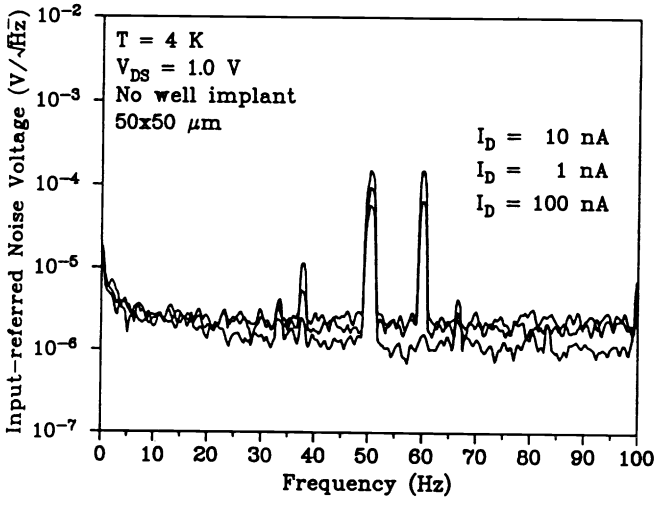
Fig. 8: A comparison of the input-referred noise voltage for different CHFETs. In a) the noise of a typical device from the old lot is compared with that in a device from the new lot. Neither device includes a p-well implant. In b) the noise for a device with a well implant is compared to that without a p-well implant. Both devices are from the new lot.



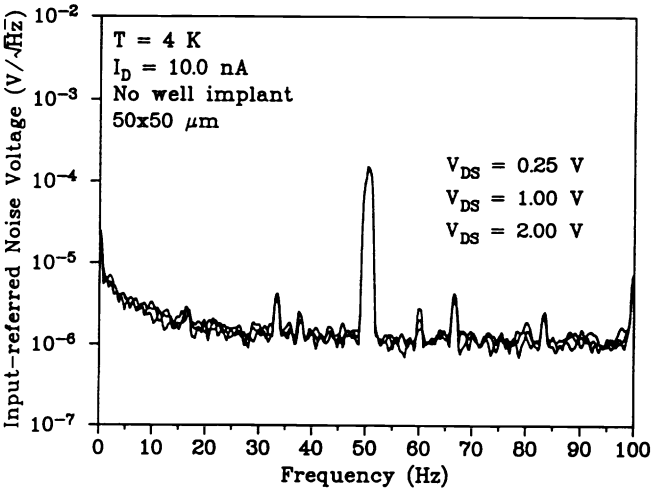

a) Noise for a 1x5, 10x3, and 50x50 size device (Dimensions are length x width in microns).




b) Noise for a device at 300 K, 77 K, and 4 K.




c) Noise for a device with drain currents of 1, 10 and 100 nA.




d) Noise for a device with drain-source voltages of 0.25, 1.0, and 2.0 V.

Fig. 9: The dependence of the input-referred noise voltage on the device size, temperature, drain current, and drain-source voltage. All devices are n-channel. Unless stated otherwise in the particular figure, the device tested was a 50 μm x 50 μm CHFET with no well implant; the temperature was 4 K; the drain current was 10 nA; the drain voltage was 1 V.

## 6. CHFET MULTIPLEXERS

Several different simple 8x1 multiplexer circuits were also fabricated and tested at 4 K. In each of these a voltage could be stored on eight capacitors that simulated a small linear array of detectors. Addressable readout electronics were connected to each capacitor and to common output circuitry which included a source follower output driver. Most of these circuits did not operate properly at 4 K. The p-channel CHFETs used to reset the capacitor voltage appeared to exhibit high leakage current from the drain to the gate and source. As a result, the output was influenced by the reset voltage and reset gate enable. P-channel CHFETs were also used in the cell select of most of the circuits, and the leakage of the p-channel devices made it impossible to disable the devices completely. It was not possible to demonstrate the multiplexing action in these devices.

One circuit did function, although with limited performance. This circuit consisted of a multiplexed array of operational amplifiers which were enabled by sending a bias voltage signal to the n-channel current source of the differential pair in the selected cell. Although the failure of the p-channel CHFETs still made it impossible to turn off the capacitor reset voltage completely, and probably reduced the impedance of the inverter load, it was possible to see both inverting and non-inverting action in the device.

This circuit, called the switched op-amp multiplexer, consists of eight differential pairs, each connected to an addressable pair source. The drain of the inverting transistor of each pair is connected to a common p-channel active load. The output voltage is buffered through an n-channel source follower connected to an n-channel current source transistor. A circuit schematic for the switched op-amp multiplexer along with the inverting transfer characteristics for each cell measured at 4 K are shown in Fig. 10. The voltage gain at 4 K is approximately 250.

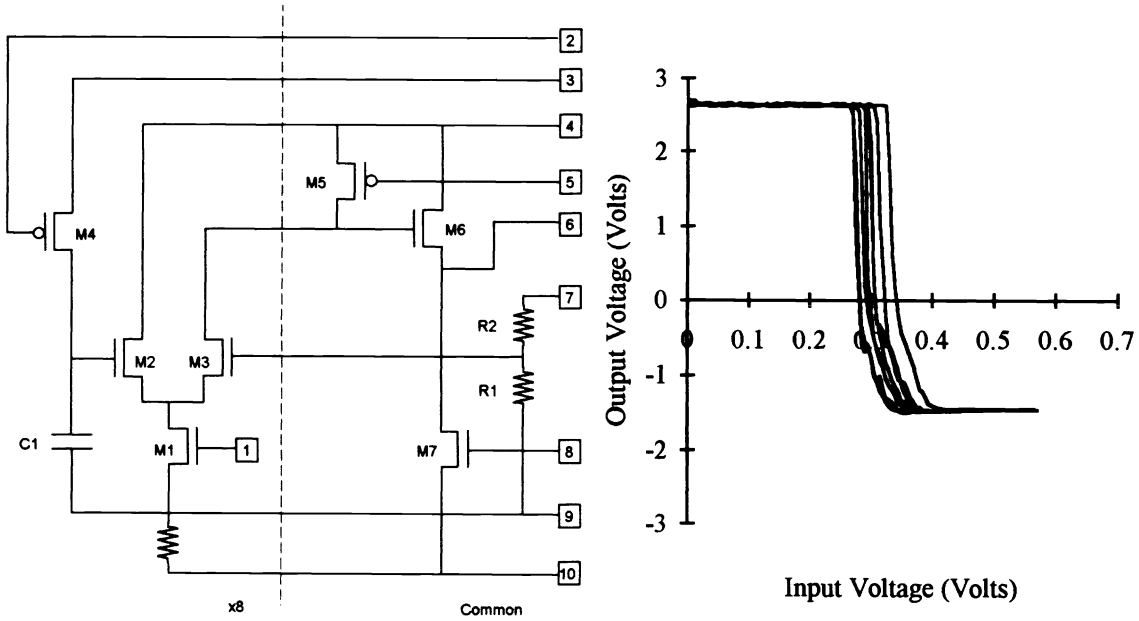



Fig. 10: A multiplexed op-amp circuit designed for operation at 4 K and a transfer curve at 4 K.

## 7. SUMMARY

The study of the new lot of CHFETs has shown that the gate leakage current can be reduced by orders of magnitude by using a gate sidewall spacer with light doping in the sidewall region. The device to device variation in the leakage current is large enough to overshadow any dependence on device area or width. This may indicate that the current is dominated by defects or point emitters on the gate edge. The noise in the new devices is of the same order of magnitude as those in the old lot. The noise is reduced by increasing the device size. It also is smaller in devices that did not include a well implant, which indicates that the existence of dopants in or near the channel region tend to increase the noise. The noise in these devices was relatively insensitive to temperature, drain current, or source-drain voltage.

## 8. ACKNOWLEDGMENT

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## 9. REFERENCES

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