Noise and current-voltage characterization of complementary heterojunction field-effect transistor (CHFET) structures below 8 K

Thomas J. Cunningham and Eric R. Fossum

Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California 91109

Steven M. Baier

Honeywell Systems and Research Center
Bloomington, Minnesota 55420

ABSTRACT

Noise and current-voltage characterization of complementary heterojunction field-effect transistor (CHFET) structures below 8 K are presented. It is shown that the CHFET exhibits normal transistor operation down to 5 K. Some of the details of the transistor operation, such as the gate-voltage dependence of the channel potential, are analyzed. The gate current is examined and is shown to be due to several mechanisms acting in parallel. These include field-emission and thermionic-field-emission, conduction through a temperature-activated resistance, and thermionic emission. The input referred noise for n-channel CHFETs is presented and discussed. The noise has the spectral dependence of 1/f noise, but does not exhibit the usual area dependence.

1. INTRODUCTION

The design of systems that include detector focal plane arrays operating at temperatures below 10 K would be greatly simplified by the availability of readout electronics that can operate with low noise at the detector temperature. One transistor that is a candidate for such applications in the complementary heterojunction field-effect transistor (CHFET). Although this device was originally developed by Honeywell Inc. for high speed digital applications,[1] several features of the device make it attractive for possible applications at temperatures below 10 K. These features include the fact that complementary p- and n-channel devices are possible (which enables low power circuitry), a structure that is expected to be immune to carrier freeze-out (providing low noise operation at very low temperatures), and heterojunction carrier confinement for radiation hardness (which is important for space applications). This paper presents the properties of these digital CHFETs at temperatures down to 5 K. It is shown that the devices exhibit normal transistor operation down to 5 K, with no kinks or other anomalies in the operating characteristics. The gate current is also analyzed and the various mechanisms that contribute to it are described. The input-referred noise is presented, and briefly discussed.

2. CHFET STRUCTURE

The structure of the CHFET and the corresponding band diagram are shown in Fig. 1. The structure is grown by MBE on a semi-insulating GaAs substrate. On this substrate an undoped GaAs buffer layer is grown, followed by a GaAs or InGaAs channel, followed by an undoped AlGaAs dielectric, and ending in a thin undoped GaAs cap layer. A WSi gate is then deposited, and serves as a self-aligned mask for the subsequent source and drain implants. After implant activation, suitable ohmic contacts are made to the source and drain. The details of the fabrication have been previously published.[1-3] The device may be either n-channel or p-channel depending solely on the source and drain implants. The channel may also be delta-doped in order to make the threshold voltages in n- and p-channel devices more symmetrical. The remainder of the structure is entirely undoped.

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The structure of the CHFET is analogous to the structure of a MOSFET, with the undoped AlGaAs layer playing the role of the oxide. One important difference, however, is that the region below the channel is undoped. In an ordinary MOSFET, a lightly doped but depleted region exists below the channel. Electric field lines from the gate terminate at the end of this depletion region. It is largely the freeze-out of this lightly doped region that causes anomalous behavior in MOSFETs as they are cooled below 20K. In contrast, the buffer layer below the channel in the CHFET is undoped, and the semi-insulating substrate is non-conducting. Electric field lines from the gate that do not terminate on the channel charge pass through the undoped buffer and terminate on the source or drain. Because the semiconductor in the CHFET is either undoped, or degenerately doped in the case of the source and drain, the device is immune to carrier freeze-out. In principle, the CHFET should operate even at temperatures approaching absolute zero. In addition, the AlGaAs dielectric is a lattice-matched epitaxial layer and can be expected to contain fewer bulk and interface traps than in the Si/SiO_2 system.

3. TRANSISTOR CHARACTERISTICS

The experimental results confirm that the CHFET operates normally down to 5 K. The transistor curves for n- and p-channel CHFETs are shown in Fig. 2a and Fig. 2b, respectively. Both devices show normal transistor operation free from kinks or other anomalies, although there is indication of a soft breakdown as the source-drain voltage is increased beyond approximately 3 V. The sub-threshold drain current I_D also behaves as expected, varying exponentially with the sub-threshold gate-source voltage V_{GS} as shown in Fig. 3. The various curves are for different size devices. Above threshold, the current should vary as $(V_{GS}-V_T)^2$. This is confirmed by a plot of $\sqrt{I_D}$ vs. V_{GS} shown in Fig. 4. Although the curves are not perfectly straight, they demonstrate reasonably linear behavior and the curves for the different size devices converge to a common V_T. A comparison of the drain currents in the different size devices at a given gate voltage also verifies that the drain current scales linearly with the width and inversely with the length as expected. For the 1x3 μm n-channel CHFET shown in Fig. 2a, the normalized transconductance at 5 K and 0.5 mA drain current is approximately 260 mS/mm. The channel mobility derived from this is approximately 4000 cm^2/V-sec.

A plot of drain current vs. gate voltage that highlights the subthreshold behavior is shown in Fig. 5 for various temperatures between 290 K and 10 K. From this data, the behavior of the channel potential as a function of gate voltage can be derived. The subthreshold current is due to thermionic emission over the barrier formed by the difference of the channel and source potentials. Once in the channel, carriers diffuse toward the drain, where they are collected. Because the current varies exponentially with the barrier, the drain current can be expressed as $I_D = I_0 \exp(V_{GS}/V_\alpha)$, where V_α is a empirically determined fit value. For any given temperature, V_α can be found from the slope of the $\mathrm{Log}(I_D)$ vs. V_{GS} in the sub-threshold region. V_α can also be expressed in terms on an ideality factor, n, times kT. Fig. 6 shows a plot of V_α vs. kT. The ideality factor n is approximately unity. There is, however, an offset, the reason for which is unknown. It is also possible to determine the barrier height at a given gate voltage from the slope of an Arrhenius plot constructed from the drain current. By examining a series of Arrhenius plots for different gate voltages, one can determine the barrier height as a function of gate voltage. A set of such Arrhenius plots is shown in Fig. 7. The resulting barrier height as a function of gate voltage is shown in Fig. 8. The barrier height varies linearly with the gate voltage with a ratio that is very nearly 1:1. This is an expected consequence of the buffer beneath the channel being undoped. The threshold voltage can also be derived, and is approximately 0.62 V for this device.

The results of these experiments can be summarized by stating that the CHFETs show normal transistor operation, as expected, with no anomalies down to the tested temperatures of 5 K.

4. GATE CURRENT

In a silicon MOSFET the charge carriers are confined to the channel by the oxide. The CHFET, on the other hand, relies on the band discontinuity between the GaAs or InGaAs channel and the AlGaAs dielectric to confine the charge

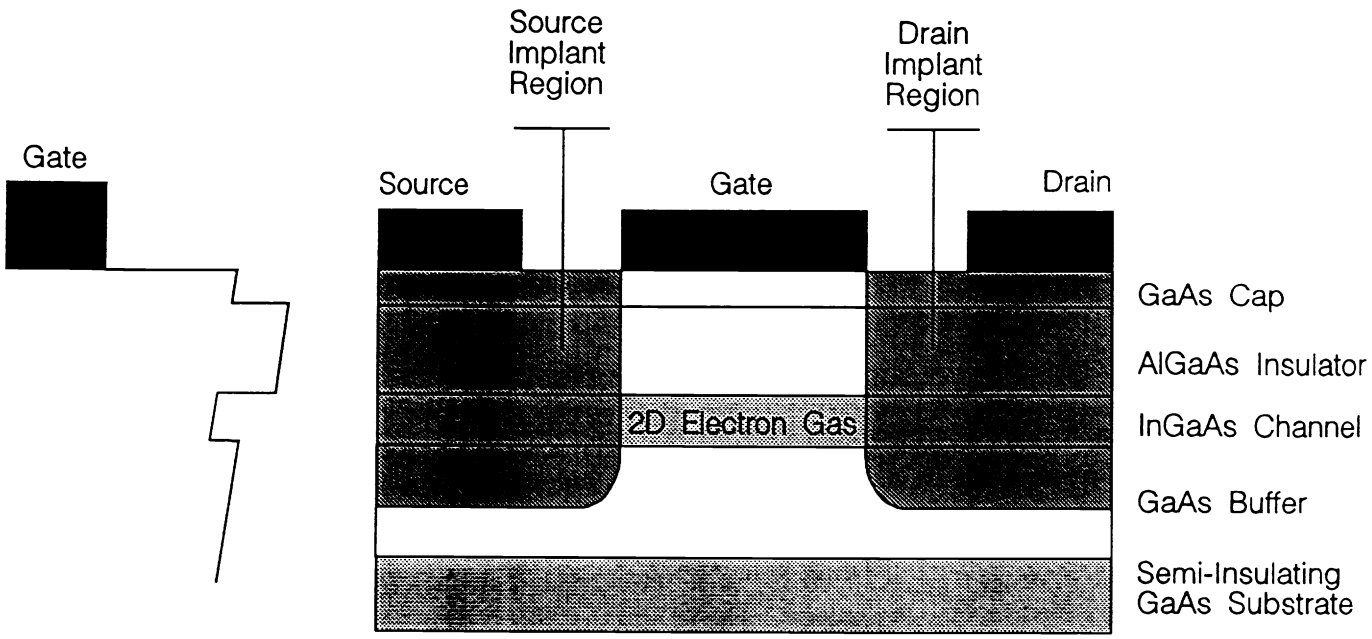

Fig. 1. The structure of the complementary heterojunction field-effect transistor (CHFET) and the corresponding band diagram. (After Honeywell Inc. Systems and Research Center)

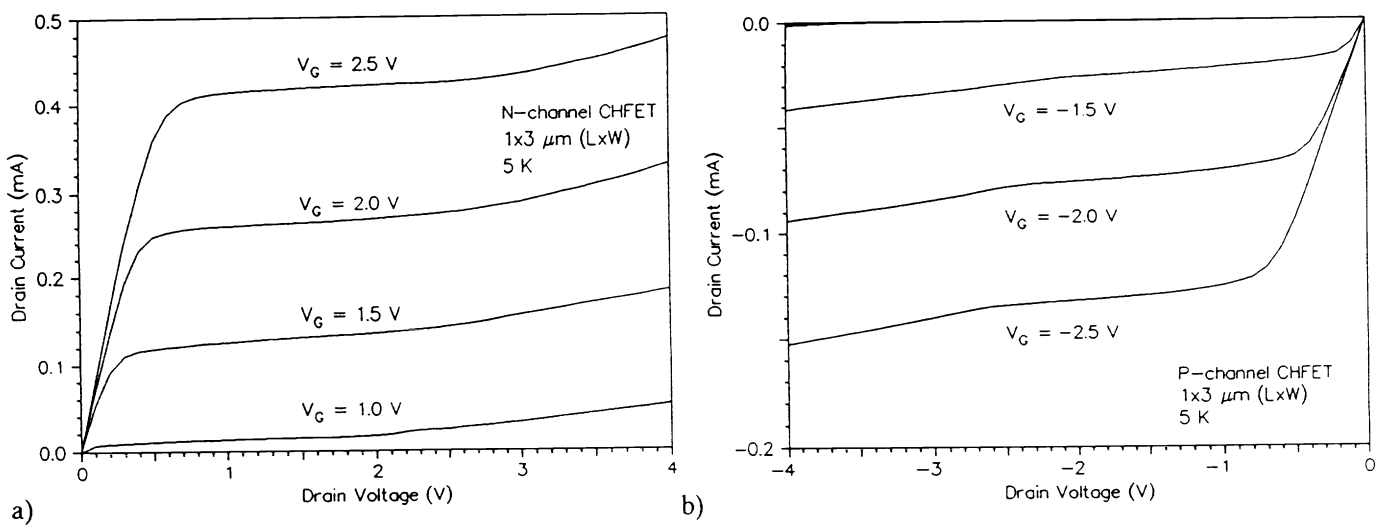

Fig. 2. The transistor curves of CHFETs at 5K. a) A 1x3 μm n-channel CHFET b) A 1x3 μm p-channel CHFET

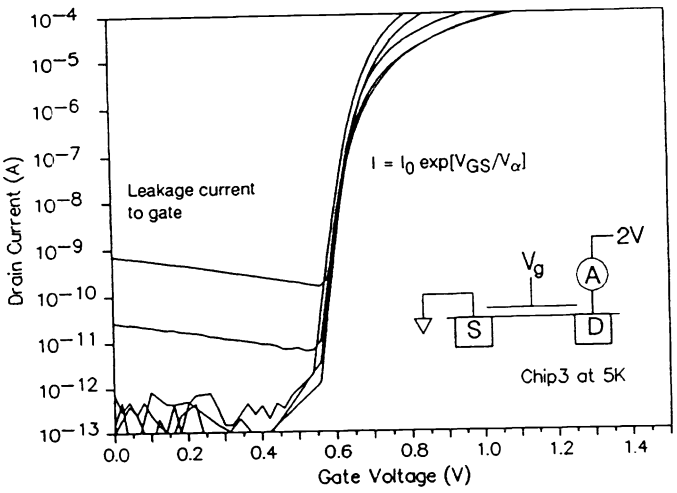

Fig. 3. The drain current as a function of gate voltage for various size n-channel devices, showing the sub-threshold behavior. The drain voltage is 2 V.

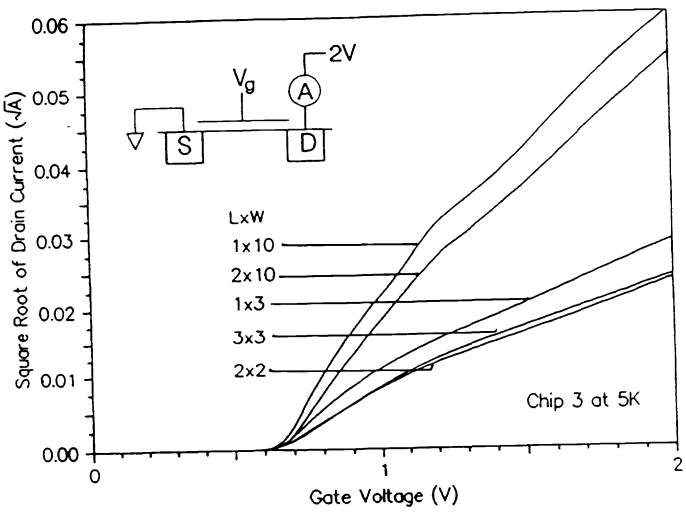

Fig. 4. The square root of the drain current as a function of gate voltage for various size n-channel devices. The drain voltage is 2 V.

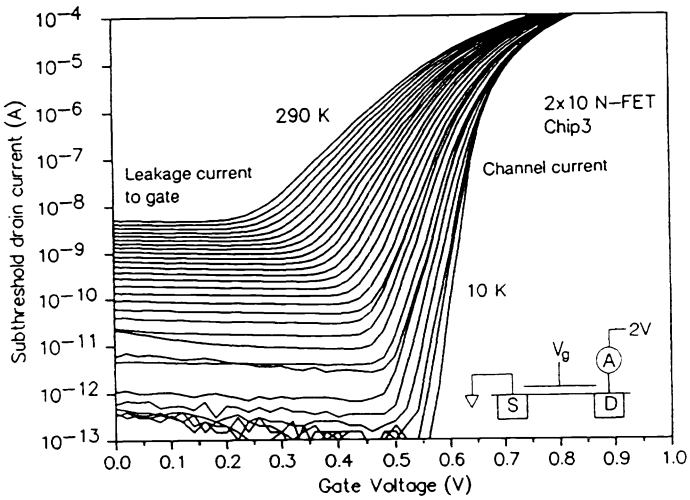

Fig. 5. The drain current vs. gate voltage for various temperatures between 10 K and 290 K for a 2x10 μm n-channel CHFET. The drain voltage is 2 V. The flat section of each curve at lower voltages is due to leakage to the gate. The noisy behavior below 10^{-12} A is due to the limit of the resolution of the HP4145 parameter analyzer used to measure the current.

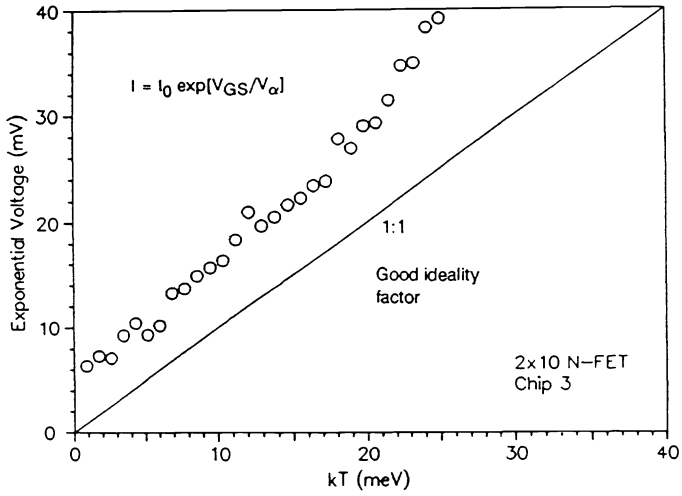

Fig. 6. The voltage V_α vs. kT for a 2x10 μm n-channel CHFET, where V_α is from an empirical fit of the drain current to the expression $I_D = I_0 \exp(V_{GS}/V_\alpha)$.

carriers. Because this band discontinuity is considerably smaller than that in the Si/SiO_2 system, the gate current in a CHFET can be significant, whereas it is negligible for most applications in the silicon MOSFET.

Fig. 9 shows a plot of the gate current in an n-channel CHFET as a function of gate voltage for various temperatures between 10K and 290K. The current was measured with an HP4145 parameter analyzer with both the source and drain grounded. The current can be understood to be due to several different mechanisms all operating in parallel and each dominant in different temperature and voltage ranges. For negative gate voltages at temperatures below 40 K, the current is dominated by field emission of electrons from the gate. The current values converge for temperatures of 10, 20, and 30 K, indicating that the current below 30 K is primarily due to field emission. As the temperature continues to increase, this broadens into thermionic-field emission. The voltage dependence of the current at 10 K is well described by the Fowler-Nordheim equation, which is verified by the fact that the data yields a straight line when graphed on a Fowler-Nordheim plot as shown in Fig. 10. The tunneling barrier height can be determined from the slope of the line. The barrier height derived from Fig. 10 is 0.48 eV, which is reasonable.

For positive gate voltages and at low temperatures, the current is again dominated by field-emission that broadens into thermionic-field-emission as the temperature is increased above 30 K. This current, however, is not well described by a Fowler-Nordheim expression. It is presumed that this current is due to tunneling of electrons in the channel through the AlGaAs dielectric and into the gate. The voltage dependence of this current is expected to be complicated, however, by the change in the amount of channel charge and the channel quasi-Fermi level, as well as the electric field, with changing gate voltage. An accurate description of the current would have to solve self-consistently for the Fermi-level in the channel. This calculation has not yet been performed. Non-uniformity in the channel potential would also have to be considered, and edge effects may be important.

For both polarities of gate voltage near room temperature, the current is dominated by a temperature activated ohmic conductance. This can be verified by plotting the current on a linear scale as shown in Fig. 11. As can be seen, the current is controlled simply by a linear resistance that depends on the temperature. Separate measurement indicate that this conductance exists not only from gate-to-source and gate-to-drain, but also from source-to-drain on a given device as well as from device-to-device on the same chip. In fact, this conductance acts like a spreading resistance in that the magnitude of the conductance is the same between any two points on the chip. A possible explanation is that the AlGaAs dielectric contains some type of trap that makes the AlGaAs layer uniformly conducting across the entire chip.

The temperature dependence of this ohmic conductance can be studied by examining an Arrhenius plot of the current at a fixed gate voltage. An Arrhenius plot of the current at a gate voltage of -1 V is shown in Fig. 12 for devices with an AlGaAs aluminum mole fraction of 75% and 50% .The plots for both mole fractions show linear portions below room temperature down to about 160 K, below which they exhibit some slight curvature. From the slope in these linear regions, activation energies can be derived. The activation energy changes with aluminum mole fraction, being 0.095 eV in the samples with 75% aluminum mole fraction, and 0.102 eV in samples with 50% aluminum mole fraction. The fact that the activation energy depends on the mole fraction gives further support to the hypothesis that the ohmic conduction is due to traps in the AlGaAs. The resulting expression for this temperature-activate ohmic resistance is

$$R = R_0 \exp(E_a/kT) \qquad (1)$$

where E_a is the activation energy. R_0 =6.5 MΩ for the device with 75% AlGaAs aluminum mole fraction, and 15.6 MΩ for the device with 50% AlGaAs aluminum mole fraction. At room temperature the resistance is of the order of 10^9 Ω.

Above room temperature the current-voltage characteristic becomes super-linear and the temperature dependence of the current becomes even more pronounced, as a thermionic emission process begins to dominate conduction. The plots on Fig. 12 also show for each mole fraction a second linear region characteristic of the thermionic emission. The activation energy for this process is about 0.45 eV for both mole fractions.

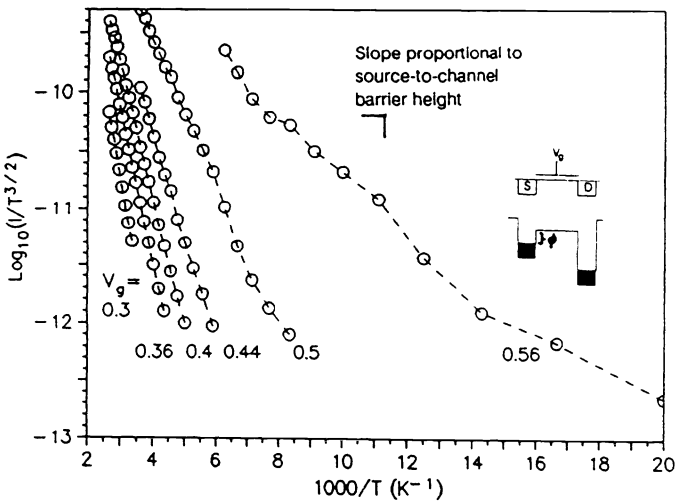

Fig. 7. A set of Arrhenius plots for a 2x10 n-channel CHFET derived from the temperature dependence of the drain current at several fixed gate voltages. The slope of each Arrhenius plot is proportional to the source-to-channel barrier height at the given gate voltage.

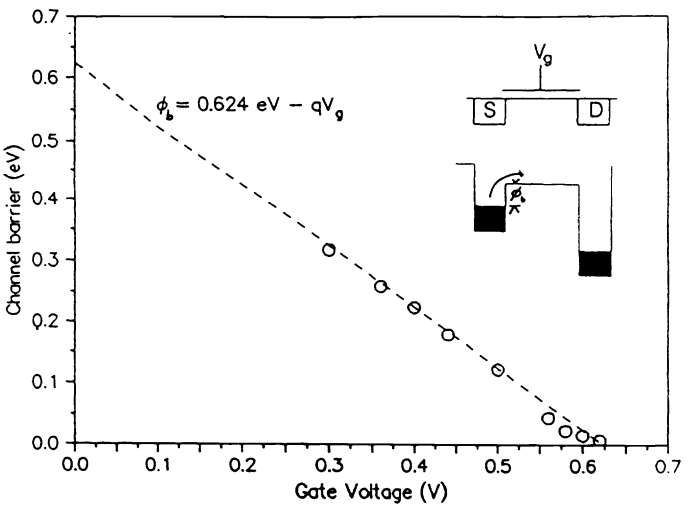

Fig. 8. The source-to-channel barrier height vs. gate-source voltage for a 2x10 n-channel CHFET.

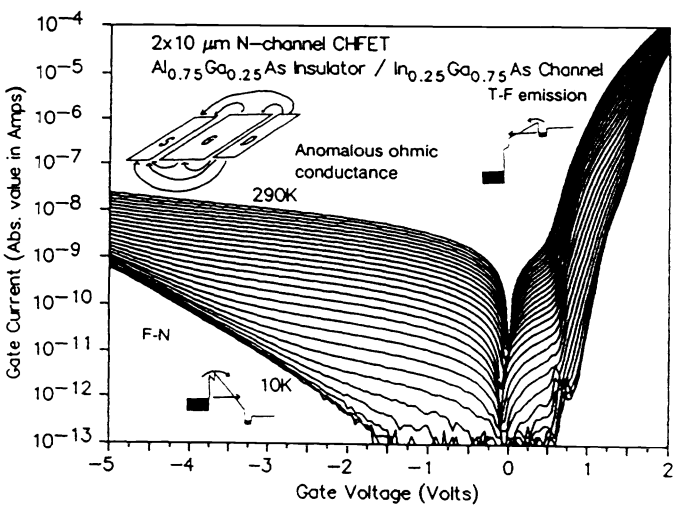

Fig. 9. The gate current vs. gate-source voltage for a 2x10 n-channel CHFET for every 10 K between 10 K and 290 K. Different conductance mechanisms dominate in different temperature-voltage regions.

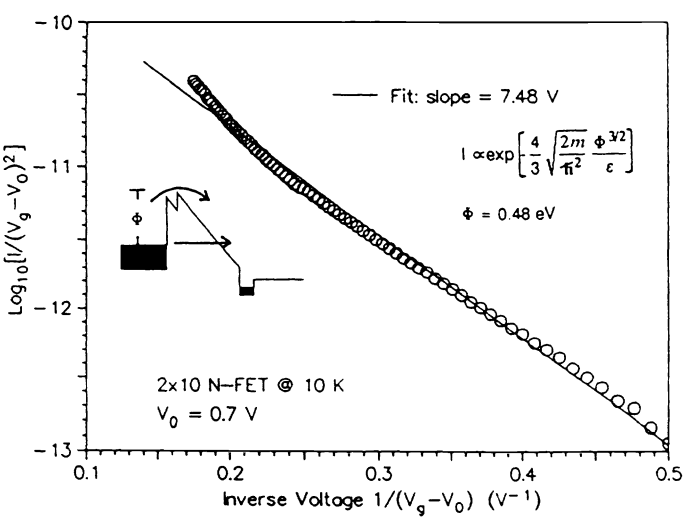

Fig. 10. A Fowler-Nordheim plot of the gate current of a 2x10 n-channel CHFET at 10 K for V<-2.0 V. The slope of the line is proportional to the tunneling barrier to the 3/2 power. The barrier derived from this plot is 0.48 eV.

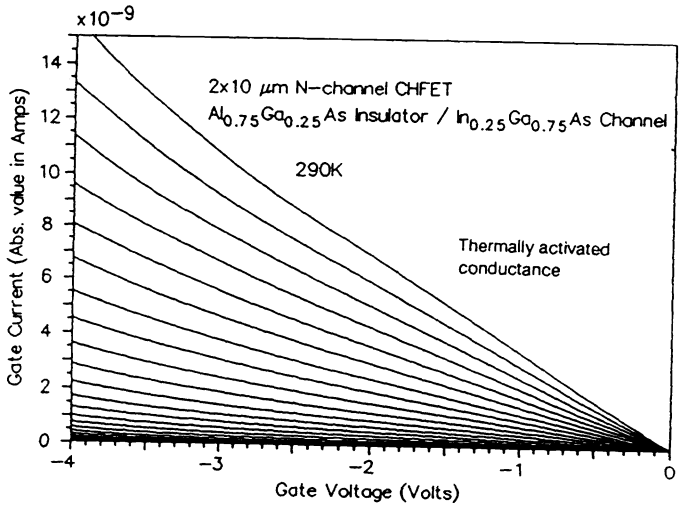

Fig. 11. The gate current vs. gate-source voltage for a 2x10 n-channel CHFET for various temperatures, plotted on a linear scale. For voltages greater than -2V, the I-V curves are linear, indicating that the current is dominated by conduction through a temperature-dependent ohmic resistance.

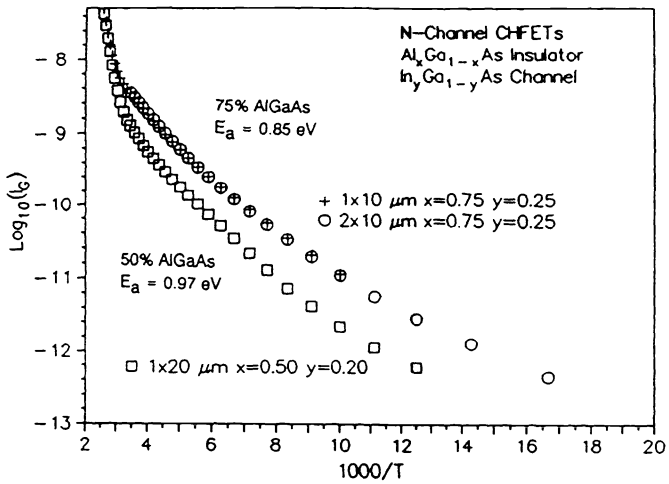

Fig. 12. An Arrhenius plot of the gate current at a fixed gate voltage of -1V, for n-channel devices with different aluminum mole fractions in the AlGaAs dielectric. Plots are shown for devices with aluminum mole fractions of 50% and 75%.

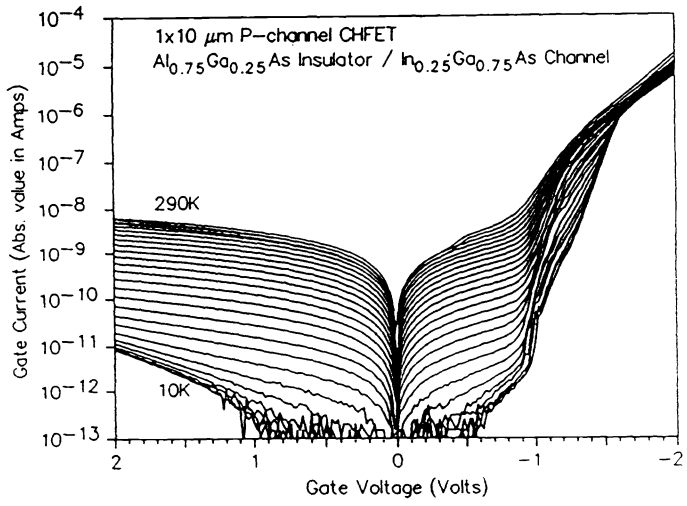

Fig. 13. The gate current vs. gate-source voltage in a 1x10 μm p-channel CHFET for every 10 K between 10 K and 290 K. All of the conduction mechanisms that are present in n-channel devices are also present in the p-channel device.

A plot of the gate current in a p-channel CHFET as a function of gate voltage for various temperatures between 10K and 290K is shown in Fig. 13. All of the qualitative features described for the n-channel device also appear for the p-channel device, and the currents are of the same order of magnitude.

The data involving the gate current can be summarized by stating that the current is the sum of currents due to several different mechanisms that operate in parallel. Fowler-Nordheim tunneling current dominates conduction for reverse gate voltages at low temperatures. For forward gate voltages the current is dominated by field-emission at very low temperatures and by thermionic-field-emission at slightly higher temperatures. Near room temperature, the current is dominated by conduction through a temperature activated resistance, which may be due to traps in the AlGaAs dielectric layer. Finally, at temperatures above room temperature, the conduction is dominated by thermionic emission. Proper manipulation of the various barrier heights and widths, along with the elimination of the trap responsible for the temperature activated ohmic resistance, may be able to significantly reduce the current from each of these mechanisms.

5. NOISE MEASUREMENTS

The drain current noise in the CHFETs was recorded by biasing the transistor in the sub-threshold region, and then measuring the voltage with a differential amplifier across a 1MΩ drain resistor held at 77 K. The noise spectra were recorded on a HP3561 dynamic signal analyzer. The input-referred noise was then calculated by dividing the drain current noise by the transconductance. The input-referred noise spectra taken on n-channel CHFETs with drain currents of 1, 10, and 100 nA are shown in Fig. 14 for a 1x3 μm device and in Fig. 15 for a 1X10 μm device.

The magnitude of the noise is approximately 50 $\mu V/\sqrt{Hz}$ at 10 Hz for I_D = 100 nA on the 1x3 μm device. This is slightly higher than that for large silicon CMOS transistors that have been optimized for cryogenic performance. The spectral dependence of the noise is characteristic of 1/f noise. The other dependencies characteristic of 1/f noise are not present, however. The input referred noise tends to decrease with increasing current, but this is not true of all devices (See Fig. 14), nor does it vary strictly inversely with the square root of the current. In most devices, 1/f noise decreases linearly with increasing area. That relationship is not valid for the tested CHFETs, however, since the noise shows no systematic variation with device size. It was also observed that the noise in p-channel devices was generally higher than in n-channel devices.

Given the small number of devices available for test, little can be inferred about the origin of the noise. It will be necessary to collect systematic data of the dependence of the noise on the temperature, area, and device bias conditions. This data, when it is available, may suggest methods of reducing the noise.

6. SUMMARY

In summary, the characteristics of the CHFET have been measured at cryogenic temperatures. The CHFET exhibits normal transistor operation down to 5 K with no kinks or anomalies in the electrical characteristics. In addition, the details of device performance, such as the variation of the channel potential with gate voltage, are reasonably well understood. The gate current is understood to be the result of several different mechanisms acting in parallel. These mechanisms are known to be field-emission and thermionic-field-emission, together with thermionic emission and a temperature-activated ohmic conductance. The activation energy of the ohmic conductance measurement has been characterized and varies with the aluminum mole fraction in the AlGaAs dielectric, suggesting that traps in the AlGaAs are responsible for this ohmic conductance. Lastly, the noise has been measured for some devices. The input-referred noise tends to decrease with increasing drain current, but does not decrease linearly with increasing area as expected. The noise data is not sufficient to suggest any mechanism responsible for the noise, indicating that more data from systematic measurements are required. New test structures and devices are presently being fabricated.

7. ACKNOWLEDGMENTS

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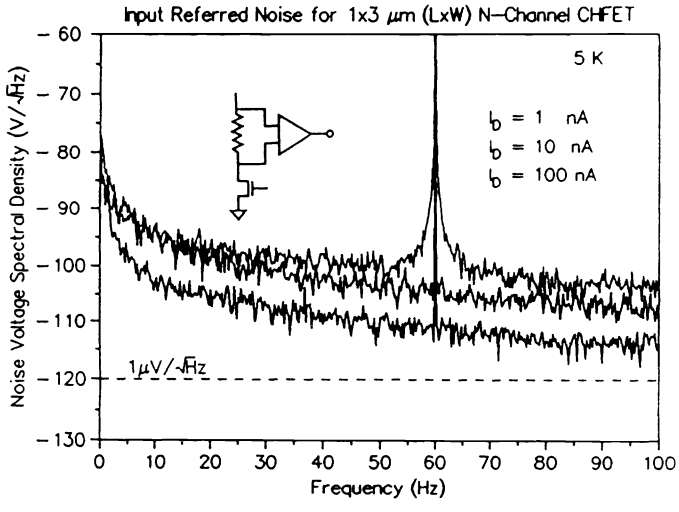

Fig. 14. Input-referred voltage noise for 1x3 μm n-channel CHFET.

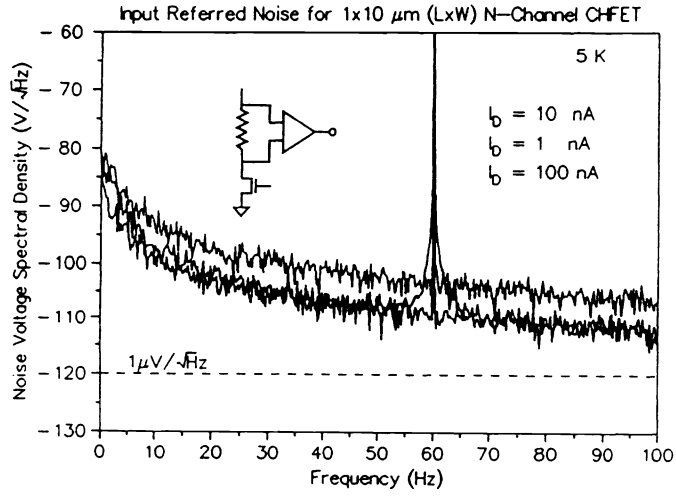

Fig. 15. Input-referred voltage noise for a 1x10 μm n-channel CHFET.