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Measurement of Hole Leakage and Impact Ionization Currents in Bistable Metal–Tunnel-Oxide–Semiconductor Junctions

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Abstract—**The electron tunneling, oxide hole transport, and hot-electron impact ionization currents in bistable metal-tunnel-oxide-semiconductor (MTOS) junctions have been measured using a novel charge-coupled device charge packet insertion transient technique, and by steady-state hole injection. Good agreement was obtained between the two techniques. An electron-to-hole oxide current ratio in the range of 20-40 was observed for a 33-Å tunnel oxide. In addition, the impact ionization hole generation current was found to be 2-5 percent of the electron tunneling current. This excess hole generation appears to be balanced in the stable high current state by back diffusion from a super-inverted semiconductor surface. The impact ionization phenomenon results in a newly discovered voltage controlled n-type negative resistance when the MTOS junction is coupled to an adjacent p-n junction through the use of an intermediate control gate.**

I. Introduction

THE metal-tunnel-oxide-semiconductor (MTOS) junction has been shown to exhibit bistable behavior in its reverse bias current-voltage characteristic for oxide thicknesses in the range 30-45 Å [1]-[3]. In the low current OFF state, a small voltage drop across the oxide allows sufficient hole leakage to balance the thermal hole generation rate in the semiconductor. In the high current ON state, a hot-electron impact ionization process resupplies holes to the interface lost to back diffusion, recombination and leakage. In this state, most of the applied voltage drops across the oxide. In either state, the observed device current is primarily the electron tunneling current from the metal gate to the semiconductor conduction band through the oxide tunneling barrier.

There are several methods to switch the device from the high impedance to the low impedance state. For example, Lai *et al.* demonstrated the use of an Al-SiO_2-Si(n) device as a light intensity sensitive latching threshold detector [1], [2]. Teng [5], [6] has shown that switching can be induced by hole injection from an adjacent forward biased p-n junction or by thermal cycling. In addition, Teng demonstrated that the associated depletion region modulation can be used in a depletion mode MOSFET for bistable signal amplification.

In this paper, the use of a charge-coupled device (CCD) input structure to inject a metered packet of holes into the MTOS junction is reported. In this mode, the MTOS junction can serve as a charge packet threshold detector. In addition, analysis of the MTOS junction current transient as it switches into either of its two stable states allows the measurement of the oxide hole transport current and hot-electron impact ionization generation current. Such measurements are confirmed by operating the input structure in a gate-controlled diode mode, and measuring the lateral hole injection current required to maintain a desired operating point of the MTOS junction.

II. Device Fabrication

For the experiments, the device structure shown in Fig. 1 was fabricated. The input structure consists of a p^+ input

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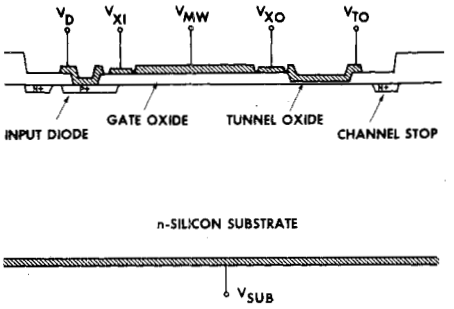

Fig. 1. Experimental device structure cross section.

diode diffusion and three electrodes. The separation between adjacent electrodes is approximately $\frac{3}{4}$ μm, obtained by using a shadowed evaporation technique [7]. The metering well (V_{MW}) size is 254 μm by 254 μm, and the MTOS junction size is 127 μm by 203 μm. The gate oxide for the input structure was grown in dry oxygen at 1000°C and subjected to both an *in situ* N_2 anneal and premetallization forming gas (95 percent N_2, 5 percent H_2) anneal at 400°C. The tunnel oxide was grown in dry oxygen at 800°C for 11 min followed by a 10-min *in situ* N_2 anneal. A post metallization anneal in N_2 at 400°C was also performed. This fabrication process yields high-quality tunnel oxides which are virtually pin-hole free [8], [9].

From small-signal capacitance-voltage measurements, it was found that the gate oxide was 550 Å thick, and had an inversion layer formation threshold voltage of -2.0 V. The nominal surface doping concentration N_D was determined to be $1.0 \times 10^{16}/\text{cm}^3$. The tunnel oxide was measured to be 33.4 Å ± 0.5 Å thick using a modified C-V extrapolation technique, [8], [10] where the thickness uncertainty reflects the measurement technique, not thickness uniformity. The MTOS flatband voltage V_{FB} was determined to be -0.19 V.

The entire experimental structure is surrounded by a phosphorous n^+ diffusion which serves both as a minority carrier channel stop and an impurity getter for minority-carrier lifetime improvement [11], [12]. Each electrode has a bonding pad located outside the channel stop region on a thick field oxide (~5000 Å). The devices were scribed and then bonded ultrasonically on a low power setting. The bonding yield on the ultra-thin oxide devices (as determined by measuring device current before and after packaging) was 100 percent. All measurements were performed with the packaged device inside a light-tight electrically shielded test box.

III. Device Operation and Results

The input structure of the experiment can be used in a number of modes. Because the gaps between adjacent electrodes are submicrometer in size, no significant barrier to lateral charge transfer exists in the semiconductor [11]. In the first mode to be discussed V_{XI}, V_{MW}, and V_{XO} are connected in parallel and the input structure functions as a gate-controlled diode [13]. The diode voltage V_D controls the surface potential ψ_s under the three gates (biased at -4 V) according to the approximate relationship

$$\psi_s = V_D + V_0 \tag{1}$$

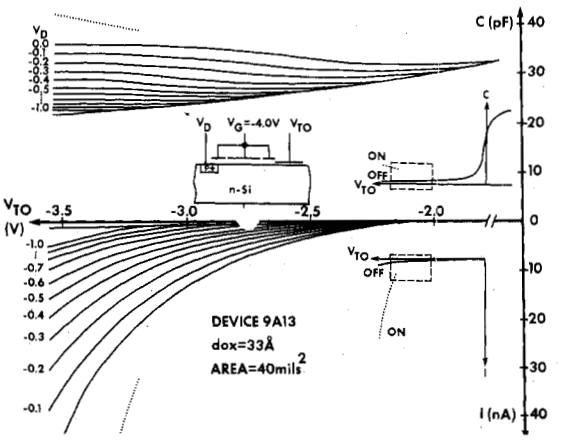

Fig. 2. MTOS junction current and small-signal, high-frequency capacitance as a function of tunnel-oxide electrode voltage, for various values of diode voltage. Inset graphs show MTOS device characteristics with V_G = 0 V. Inset cross section shows electrode biasing.

where V_0 = -0.70 V for $N_D = 1 \times 10^{16}/\text{cm}^3$. This behavior was confirmed by capacitance measurements. When a bias voltage of -3.5 V is applied to the tunnel oxide electrode, its surface potential is similarly controlled by V_D,[1] which in turn determines the tunnel oxide voltage drop. This technique is somewhat similar to that of Hsueh *et al.* [14] except that they used a p^+ region to bridge the inter-electrode gap and confined their attention to thinner oxides. Our structure avoids an overlap of the tunnel oxide and a heavily doped region, which, depending upon the ratio of areas of the overlap region to nonoverlap region, may contribute a significant error due to the increased oxide voltage drop in the vicinity of the overlap region.

The effect of the diode voltage on the MTOS current-voltage and small signal capacitance-voltage characteristics is shown in Fig. 2. Because hole transport through the ultra-thin oxide can occur,[2] the diode must supply a small lateral injection current I_{inj} to resupply lost holes and maintain control of the surface potential under the tunnel oxide. This injection current has been measured as a function of V_D, by calculating the difference between the total measured diode current when V_{TO} = 0 and when V_{TO} = -3.5 V. As shown in Fig. 3, the injection current increases as V_D is varied from -1.0 to -0.3 V. In this range, the injection current is approximately equal to the oxide hole transport current and increases as the oxide voltage is raised. However, when the oxide voltage reaches a critical value, electrons tunneling from the metal gate have sufficient energy in the silicon to generate electron-hole pairs through an impact ionization process. This hole generation current partially resupplies holes lost through the oxide, and reduces the hole injection required from the diode. Hence, the injection current reduces in an n-type negative resistance fashion from $V_D \simeq -0.3$ V to $V_D \simeq +0.1$ V, and

[1] Capacitance measurements indicate that $V_0 \simeq -0.53$ V for the tunnel oxide surface potential.

[2] The transport mechanism for hole leakage through the oxide is not firmly established. Possible mechanisms include elastic and inelastic electron tunneling from the metal into the semiconductor valence band, and hopping conduction via oxide trap states.

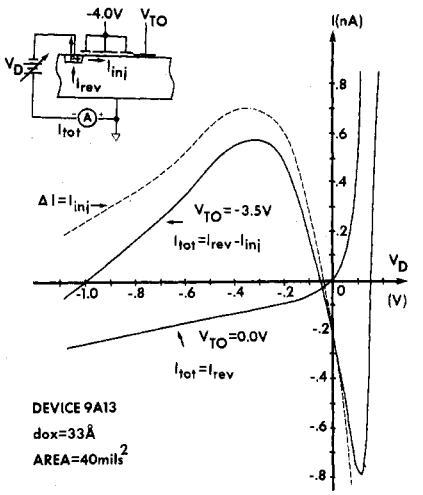

Fig. 3. Diode current-voltage relationship for $V_{T0} = 0$ and $V_{T0} = -3.5$ V. The difference between the two curves is also plotted and may be interpreted as the lateral hole injection/extraction current between the diode and the MTOS junction. Inset shows experimental set up.

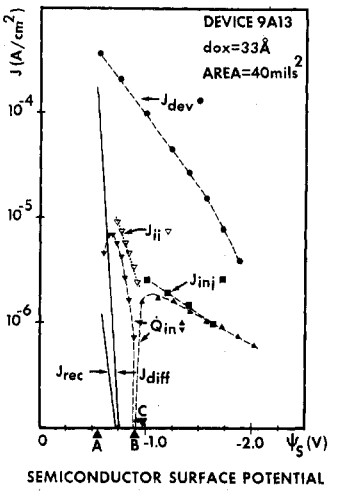

Fig. 4. Current density versus semiconductor surface potential for the MTOS junction biased at -3.5 V. J_{dev} is the experimentally measured device current. J_{inj} is the steady-state hole injection current. Q_{inv} is the rate of charging or draining minority carriers in the inversion layer as measured using the transient current technique. J_{ii} is the inferred impact ionization current obtained by adding the extrapolated oxide hole transport current to Q_{inv}. J_{diff} and J_{rec} are the back hole diffusion and space-charge recombination currents, respectively as obtained using a computer model. Point A marks the steady state ON operating point of the device. Point B marks the metastable operating point of the device. Point C marks the surface potential when $pn = n_i^2$ in the semiconductor space-charge region.

even changes sign as the diode extracts holes from the MTOS junction to maintain the surface potential. Beyond $V_D = +0.1$ V, the normal forward p-n junction diode current obscures the hole extraction current, and the current again changes sign and increases exponentially. A similar n-type negative resistance phenomenon has been observed in recent experiments in our laboratory using a thicker (Fowler-Nordheim) tunnel oxide.

By examining the injection current in the range $-1.0 < V_D < -0.3$ V, a measure of the ratio of the electron current-to-hole current through the oxide can be obtained. These currents are shown in Fig. 4. The ratio of the two current components for this 33 Å oxide is found to be approximately 20 to 40 depending on the oxide voltage drop, and is related to the current multiplication effect of Green and Schewchun [15].

A second mode of operating the input structure is a slight modification of the first, and enables the observation of the transient device current as the MTOS junction switches to one of its two stable states. In this mode, V_{X0} is suddenly clamped off after the input diode has been allowed to preset the tunnel oxide surface potential. The isolated MTOS junction subsequently switches to either its high or low impedance state, depending upon the level of the preset surface potential. The transient device current is shown in Fig. 5 for various values of V_D. The discontinuity of the transient current at $t = 0^+$ is due to the insertion of additional holes into the MTOS junction when the inversion layer under V_{X0} is clamped off. The inserted holes increase the oxide voltage drop and reduce the electron tunneling barrier. The increase in current is in quantitative agreement with the MTOS-current inversion-layer relationship which will be discussed below.

To further investigate the transient response of the device, a third mode of operation is utilized. The first two input structure electrodes and input diode are clocked to create a charge packet of measured size in the metering well. The charge packet is formed using a linear surface potential equilibration method [16] such that the magnitude of the charge

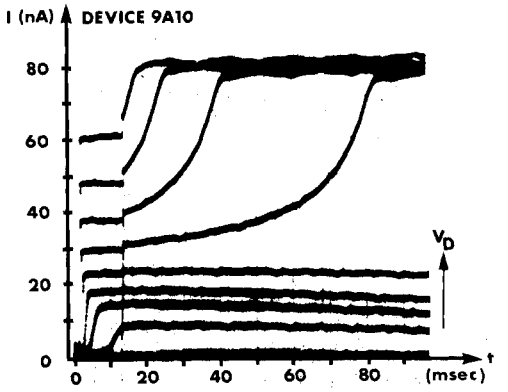

Fig. 5. Multiple exposure photograph showing transient MTOS junction current ($V_{T0} = -3.45$ V) for various values of preset surface potential. V_{T0} is applied at $t = 0$. V_{X0} is clamped off at $t \simeq 12$ ms. V_D is incremented by 100 mV from -0.6 V at the lowest current level to +0.2 V at the highest level. Waveform ripple is due to residual 60-Hz noise in the measuring circuit.

is given by

$$-Q_{in} = A_{MW} \cdot \frac{\epsilon_0 \epsilon_{ox}}{d_{ox}} (V_{MW} - V_{XI}) \qquad (2)$$

where $\epsilon_{ox} = 3.9$ is the relative dielectric constant of SiO_2 and $d_{ox} = 550$ Å is the gate oxide thickness. The relationship between V_{MW} and Q_{in} was confirmed by two methods. The first is the measurement of the net charge injected through the input diode by integrating the diode current. The second is through the use of a parallel charge packet formation channel (isolated from the first by a channel stop diffusion) whose output is routed to a precharged source-follower output ampli-

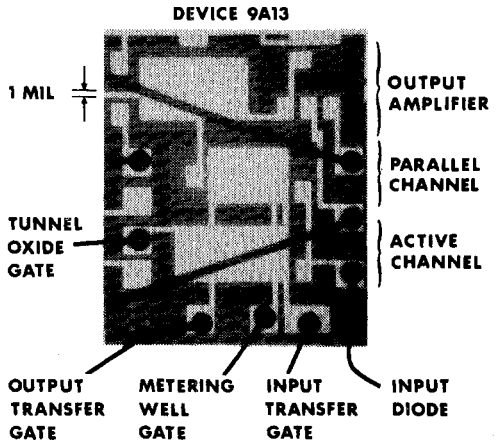

Fig. 6. Photograph of measured device showing aluminum electrodes, parallel charge packet formation channel, and source-follower MOSFET charge packet output amplifier. Interelectrode gaps not visible at this magnification. (1 mil = 25.4 μm)

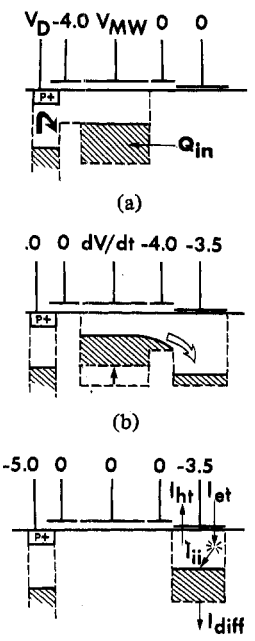

Fig. 7. Depiction of charge packet injection sequence. In Fig. 7(a), the charge packet is formed using a "fill and spill" technique. In Fig. 7(b), the charge packet is injected into the MTOS junction. In Fig. 7(c), the MTOS junction switches into its high-current state.

fier [11], as shown in Fig. 6. For the experimental device, the charge packet was related to V_{MW} by

$$-Q_{in} = 41 \cdot V_{MW} + 164 \quad \text{(in pC)}. \tag{3}$$

Once the charge packet has been formed, $V_{T0} = -3.5$ V is applied to the tunnel oxide, and $V_{X0} = -4.0$ V is applied to the output transfer gate. The metering well voltage V_{MW} is ramped to zero at 0.25 V/μs causing the charge packet to be injected into the deep depleted MTOS potential well. Following injection, V_{X0} is switched off, so that the metered charge packet is equal to the MTOS inversion layer charge and has essentially preset the MTOS surface potential. This sequence is depicted in Fig. 7.

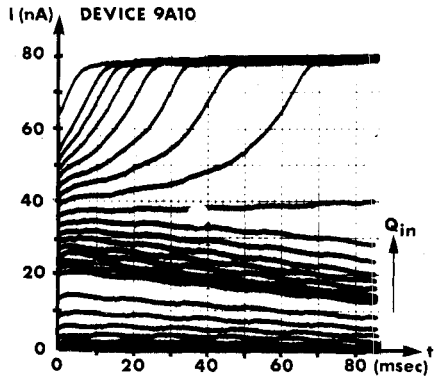

Fig. 8. Multiple exposure photograph showing transient MTOS junction current ($V_{T0} = -3.45$ V) for various sizes in injected charge packets. The packet is injected at $t = 0$. V_{MW} is incremented by -1.0 V in the range -12 to -22 V (highest current level) except between -18 and -21 V where V_{MW} is incremented by -0.2 V. Relationship between V_{MW} and injected charge packet size defined in text. Waveform ripple is due to residual 60-Hz noise in the measuring current.

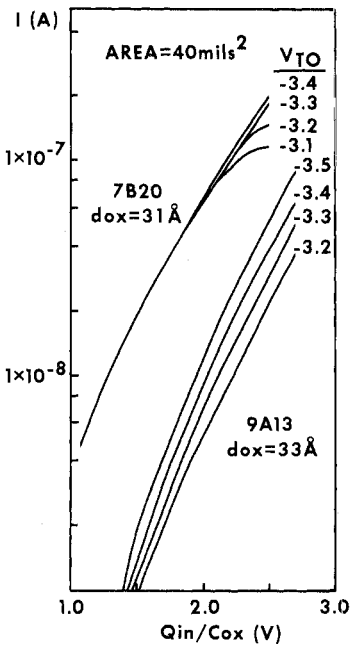

Fig. 9. Semi-log plot of transient current at $t = 0^+$ versus oxide voltage for various values of V_{T0} for two devices.

The transient MTOS current for increasing values of V_{MW} (i.e., Q_{in}) is shown in Fig. 8. It is found that if Q_{in} exceeds a critical value of 630 pC, the MTOS device switches into the high current state. For injected charge packets below this quantity, the transient current decays until the device reaches a low-current steady state. The initial transient current is plotted as a function of injected charge packet for various values of V_{T0} for two different devices in Fig. 9. From electron tunneling theory, the exponential dependence of the current on oxide voltage (proportional to injected charge packet) is expected [8]. Only a marginal effect of the total junction bias V_{T0} on the electron tunneling current is predicted. The apparent dependence of initial transient current on V_{T0} for device 9A13 has been since shown to be an artifact of the measurement circuit, not present during the measurement of other devices such as 7B20.

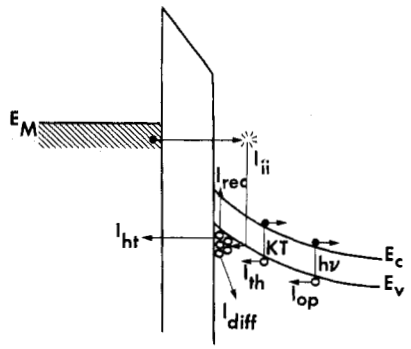

Fig. 10. Schematic energy band diagram of MTOS junction illustrating current components of $\dot{Q}_{inv}$. Subscripts are: *ii*–impact ionization; *th*–thermal generation; *op*–optical generation; *rec*–recombination; *ht*–hole transport; diff–hole diffusion. Not all components are active simultaneously.

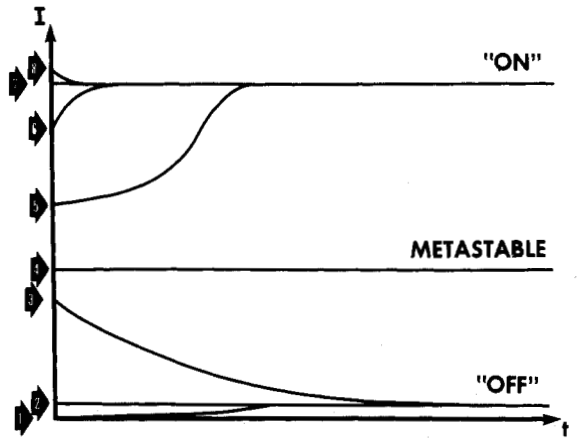

Fig. 11. Illustration of various transient current regimes corresponding to increasing sizes of injected charge packets. Regimes are discussed in the text.

IV. Analysis

The rate of change of transient current is related to the rate of change of inversion layer charge Q_{inv} through

$$\frac{\partial I}{\partial t} = \frac{\partial I}{\partial Q_{in}} \cdot \frac{\partial Q_{inv}}{\partial t}. \tag{4}$$

By measuring $\delta I/\delta t$ at $t = 0^+$, a measure of $\partial Q_{inv}/\partial t = \dot{Q}_{inv}$ can be obtained as shown in Fig. 4.

The rate of change $\dot{Q}_{inv}$ consists of several current components as illustrated in Fig. 10. In general

$$\dot{Q}_{inv} = I_{th} + I_{ii} + I_{op} - I_{ht} - I_{rec} - I_{diff}. \tag{5}$$

However, in any particular transient current regime (see Fig. 11) only one or two terms in (5) dominate. In the discussion below, it is assumed that the optically generated current $I_{op} = 0$.

In the regime labeled 1 in Fig. 11, $\dot{Q}_{inv}$ is dominated by the thermal generation of holes in the deep depletion region and nearby bulk so that $\dot{Q}_{inv} = I_{th}$. The time required to reach the OFF state has been understated in Fig. 11. In regime 2, a small inversion layer of holes has resulted in an increased tunnel oxide voltage drop and reduced hole oxide transport barrier. In this regime, thermal hole generation is balanced by hole leakage so that $\dot{Q}_{inv} = 0$. This is the stable low-current OFF state.

Regime 3 is dominated by net hole leakage from the inversion layer. In this regime, $\dot{Q}_{inv} = -I_{ht}$. Using (4), the hole transport current is calculated and is plotted in Fig. 4. The agreement between the hole leakage current calculated using this transient technique and hole leakage current measured by the gate-controlled diode, steady-state hole injection technique can be seen to be quite good.

In the fourth current regime, the device exists in a metastable state. The hole leakage current is balanced by the impact ionization hole generation current discussed previously, so that $\dot{Q}_{inv} = 0$. This state is unstable with respect to small variations in I_{ii} or I_{ht} (such as introduced by a fluctuation in V_{T0}) and is difficult to observe experimentally for durations exceeding a few hundred milliseconds. This condition represents a critical value of V_{ox}. For higher levels of V_{ox}, the device switches into the low-impedance steady state, and for lower values, the device current decays into the high impedance state. The critical value of V_{ox} for $V_{T0} = -3.5$ V is 2.40 V. Note that the injected charge required to achieve this state (630 pC) exceeds the theoretical charge ($\simeq$600 pC) required to place the device in thermal equilibrium were the device current "turned off."[3] We refer to this condition as super-inversion.

In regime 5, the impact ionization current I_{ii} exceeds the hole leakage current and $\dot{Q}_{inv} = I_{ii} - I_{ht}$. The inversion layer grows, decreasing the oxide barrier. This results in increased electron and hole currents. However, the impact ionization current grows differentially faster than the hole current increasing the gain of the net positive feedback. By calculating $\dot{Q}_{inv}$, an estimate of I_{ii} can be obtained as shown in Fig. 4., by summing $\dot{Q}_{inv}$ with an oxide hole leakage current extrapolated from regime 3. The impact ionization current was found to be 2-5 percent of the total device current. The extrapolated intersection of the impact ionization and hole leakage currents reasonably well predicts the metastable state discussed above.

The measured impact ionization current can be compared to a model of the impact ionization process developed by Drummond and Moll [17]. In their model, the total impact ionization probability for a hot electron of energy E is given by

$$P_{ii} = \sum_{n=0}^{N} P_n \tag{6}$$

where P_n is the probability the carrier will cause ionization after exactly n phonon scatterings, and N is the number of phonon scatterings necessary to reduce the carrier energy below the threshold for impact ionization. The probability P_n is in turn determined according to

$$P_n = (1 - P_0) \cdot (1 - P_1), \cdots, (1 - P_{n-1}) \cdot [1 + r_{ph}/r_{ii}]^{-1} \tag{7}$$

[3] By thermal equilibrium in this case, we mean that $pn = n_i^2$ throughout the space-charge region.

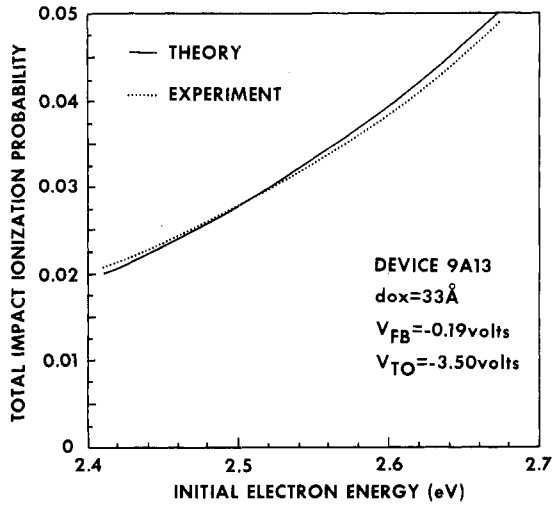

Fig. 12. Total impact ionization probability as a function of initial hot-electron energy, as calculated theoretically [17], and as determined experimentally as described in the text.

where the ratio of optical phonon scattering rate r_{ph} to impact ionization scattering rate r_{ii} is given by

$$r_{ph}/r_{ii} = 648 \cdot [E - nE_{ph} - E_g]^{-4.2} \tag{8}$$

with the optical phonon energy $E_{ph} = 0.063$ eV and the silicon energy gap $E_g = 1.12$ eV.

The total impact ionization rate as a function of hot-electron energy in the energy range probed in this experiment is shown in Fig. 12, along with the experimentally determined ratio of impact ionization current to total device current. The experimental data matches the Drummond-Moll model quite well, though the curvature may be matched more precisely by slight adjustment of the band structure exponent of (8). In this experiment, the hot-electron energy is determined by assuming all the tunneling electrons emerge in the silicon with energy given by the difference between the metal Fermi level and the silicon conduction band edge at the Si-SiO_2 interface. Although such an assumption neglects electrons tunneling from below the metal Fermi level and energy gained by electrons in the silicon due to the electric field, it is expected that these two effects nearly cancel.

In regime 6, the positive feedback mechanism is dampened primarily by hole diffusion from the super-inversion layer back toward the bulk, and partially by electron-hole recombination in the space-charge region. From a simple space-charge model [18], a theoretical back hole diffusion current J_{diff} can be calculated using $\mu_p = 480$ cm^2/V · s and the measured minority-carrier lifetime of 8 μs. This loss current is plotted in Fig. 4. Also shown is the calculated recombination current J_{rec} (which does not include surface recombination). The intersection of the diffusion current loss and the impact ionization generation current gain should yield the stable high current state of the device, since $\dot{Q}_{\text{inv}} = I_{ii} - I_{\text{diff}} - I_{\text{rec}}$, and in regime 7, the stable, high-current ON state, $\dot{Q}_{\text{inv}} = 0$.

It is also possible to have the transient current regime labeled 8. Here, a charge packet exceeding the value of Q_{inv} in regime 7 is inserted into the junction. However, the back diffusion/recombination current is so strong that the state quickly decays to the stable high-current state. We have observed such a transient current for $V_{T0} = -3.4$ V, where the maximum charge packet which can be formed by the input structure is sufficient to cause such a condition.

V. Summary and Conclusions

In summary, an experimental device structure which allows the measurement of both the oxide hole transport current component and electron tunneling current component in an MTOS junction by a steady-state hole injection technique and by an injected hole packet transient technique has been fabricated. Good agreement was obtained between the two methods. For the 33-Å-tunnel oxide device, a current component ratio in the range 20-40 was observed. The impact ionization current component, which is critical to the bistable operation of this device, was also inferred. This current was found to be 2-5 percent of the total device current in the regime examined, and well described by the impact ionization rate model of Drummond and Moll. Finally, by introducing a simple space-charge model, it was shown that the high-current state of the device is limited by a back diffusion loss mechanism, though surface recombination enhanced by a strong electric field may also play an important role.

Because of the good agreement obtained between the two techniques, it is concluded that the transient response analysis technique is viable and accurate, and will be useful for probing other capacitive structures such as metal-nitride-oxide-semiconductor (MNOS) and silicon-rich SiO_2 devices.

The slow switching speed of the Al-SiO_2-Si(n) device (~10-100 ms) due to the low impact ionization probability voids its utility as a charge packet threshold detector in all but the most relaxed system environments. Investigation of thicker (Fowler-Nordheim) tunnel oxides is presently underway to increase switching speed by raising the energy of the hot electrons and increasing their impact ionization probability. Reduction of the gate electrode work function may also increase switching speed in direct tunneling devices by similarly increasing the capacitor charging current.

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A New Tungsten Gate Process for VLSI Applications

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Abstract—**In spite of the growing demand for MOS gates and interconnections of higher conductivity, the refractory metal gate process has not received as much attention as those using silicides because it is incompatible with the Si-gate process. The metal gate cannot withstand oxidizing annealing ambients, and source-drain formation by ion implantation is difficult because of the channeling of doping ions through the gate metal during ion implantation. In a new process developed for use in MOS VLSI fabrication, tungsten (W) is used as a gate metal because degradation of SiO_2 by annealing the metal/SiO_2/Si structure at around 1000°C can be minimized if the metal is W. Metal oxidation is prevented by using a H_2/H_2O ambient for this annealing, which also allows Si to be oxidized in the same ambient. The channeling mentioned above is stopped by forming a thin layer of PSG or WO_x on the W. This gate process is believed to be a step forward toward the desired compatibility.**

I. Introduction

As DEVICE dimensions continue to decrease to achieve higher density and performance, there is a growing demand for a highly conductive material to be used as gates and interconnections in MOS circuits. The poly Si used for this purpose in the conventional process has certain limitations, due mainly to limited conductivity. Recently, various metal silicides [1]-[3] have been considered because they have a conductivity which is higher than that of poly Si by about one order of magnitude and, like poly Si, they can be annealed in oxidizing ambients, if they are used in a metal silicide/poly Si("polycide") structure [2].

Such refractory metals as molybdenum (Mo) [4]-[6] and tungsten (W) [6], [7] have been considered, but they are not widely used, due mostly to the fact that they cannot withstand oxidizing ambients at high temperature. Furthermore, if these metals are to be used as gates, resulting in a departure from the conventional poly Si/SiO_2 structure, very careful evaluation of the metal-SiO_2 interface must be made before they can be used. This should become all the more important as gate oxide (SiO_2) thickness decreases with device dimensions.

However, it is expected that higher conductivity than that of the silicides will be required in the near future for gates and interconnections in VLSI's with very high integration densities ($\gtrsim$Mb). Hence, it is imperative that refractory metals be put to use, in spite of the difficulties just mentioned.

This paper describes a new gate process using W, with special attention to the metal-SiO_2 interface reaction and to the problem of heating in oxidizing ambients. First, selection of the most suitable gate metal is discussed. Next, our solution of the two major problems encountered in making the new process as compatible as possible with the conventional one is presented. These problems are: channeling of the doping ions through the gate metal during the ion implantation used for

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