Low-power low-noise analog circuits for on-focal-plane signal processing of infrared sensors

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ABSTRACT

On-focal-plane signal processing circuits for enhancement of IR imager performance are presented. To enable the detection of high background IR images, an in-pixel current-mode background suppression scheme is presented. The background suppression circuit consists of a current memory placed in the feedback loop of a CTIA and is designed for a thousand-fold suppression of the background flux, thereby easing circuit design constraints, and assuring BLIP operation even with detectors having large response non-uniformities. For improving the performance of low-background IR imagers, an on-chip column-parallel analog-to-digital converter (ADC) is presented. The design of a 10-bit ADC with 50 μm pitch and based on sigma-delta (Σ-Δ) modulation is presented. A novel IR imager readout technique featuring photoelectron counting in the unit cell is presented for ultra-low background applications. The output of the unit cell is a digital word corresponding to the incident flux density and the readout is noise free. The design of low-power (< 5 μW), sub-electron input-referred noise, high-gain (> 100,000), small real-estate (60 μm pitch) self-biased CMOS amplifiers required for photon counting are presented.

1. INTRODUCTION

The operating conditions of IR image sensors vary significantly depending upon applications. While a large background flux is a characteristic feature of terrestrial IR imaging in the 8-14 μm band (LWIR band), IR imagers in astronomical applications operate with an ultra-low background. The presence of a large background flux imposes a prohibitively large dynamic range requirement on the unit cell electronics, and is one of the chief reasons for the scarcity of accurate readout structures for LWIR high background applications [1]. Further, due to the relative immaturity of IR detectors compared to silicon detectors for visible light imaging, the response non-uniformity of an IR detector is inferior compared to its visible wavelength counterpart. Large response non-uniformity (±10%) translates to large spatial noise [2], preventing the background shot noise limited performance (BLIP).

The critical issue in high resolution focal-plane readout design for ultra-low background applications is the system noise. There are several sources of noise in a conventional IR focal-plane array (FPA). Apart from the electronic noise in the readout unit cell, clock pick-up constitutes a major source of noise in the switched CMOS analog multiplexer. The clock pick-up and cross-talk noise can be as high as 400 electrons r.m.s. even for a relatively small array of size 58X62 [3]. Further, electromagnetic interference (EMI) is another important concern in the transmission of analog signals off the focal-plane of high-performance FPAs. While the use of shielded cables and careful attention to details can ameliorate most of the EMI-related effects, it adds an extra heat load to the system, introduces concern for reliability, and tends to be expensive. An additional concern is the power dissipated in driving high resolution analog signals off the focal-plane. The increased power dissipation is a result of the large shielded-cable capacitance, and the large bandwidth requirement associated with the high settling accuracy required in scientific imaging. Thus, conversion of the signal from analog to digital domain can not only provide immunity to signal degradation due to EMI and cross-talk, it also simplifies system interface leading to easy, high reliability, low-power system design, and can help reduce sensor mass, all of which are requirements for several NASA low cost explorer missions [4].

In this paper, low-power focal-plane circuits for enhancing the performance of IR imagers are described. The paper is divided into three main sections, where three different IR focal-plane signal processing circuits are presented. Section 2 deals with an in-pixel background suppression scheme. The critical component of this scheme is a highly accurate current memory operating at ultra-low current levels (1-100 nA). The design and performance of current memory circuits capable of ultra-low current operation are reported in this section. In section 3, the design of a first order Σ-Δ ADC featuring low-

power, 10-bit resolution, and a 50 μm pitch is presented. Section 4 concerns the description of an advanced focal-plane readout technique, featuring photoelectron counting in each pixel. This readout technique is equivalent to incorporation of an ADC in each unit cell, and represents a next-generation sensor for ultra-light-level focal-plane signal detection. The design and performance of low-power, high-gain, sub-electron input-referred noise, self-biased amplifiers are also reported in this section.

2. CURRENT MEMORY-BASED BACKGROUND SUPPRESSION CIRCUIT

2.1 Advantages of background suppression

One of the attractive features of terrestrial IR imaging in the LWIR band is the availability of an increased background flux at typical scene temperatures (300K - 400K). The increased background flux eases the electronic noise requirements on the focal-plane readout due to an increased background shot noise. However, a conventional reset-integrator type readout [5,6] integrates the entire background flux in the unit cell, thereby imposing prohibitively large dynamic range requirements on the readout pixel (required storage capacity ~ 10^9 carriers per pixel). The effective dynamic range requirement can be reduced a factor of N if an N-fold suppression of the background flux is achieved on the focal-plane. This would enable construction of accurate IR focal-plane readouts operating under high background conditions.

The on-focal-plane background suppression also increases the sensitivity of the readout. The sensitivity of a focal-plane readout is determined by the system noise, and is measured by the noise equivalent scene temperature differential (NEΔT) [7]. Including the effect of spatial noise generated by inter-pixel response non-uniformity, NEΔT is given by [8]:

$$NE\Delta T \cong \frac{1}{C}\left[\sqrt{U^2(1-\kappa)^2 + \frac{(1-\kappa)}{N_b}}\right] \tag{1}$$

where U is the average non-uniformity in the detector array, κ is the background suppression fraction (κ=0 indicates no suppression), and N_b is the number of background charges (for a given background flux) integrated on the focal-plane unit cell. The equation 1 indicates that in detector arrays with a large amount of detector response non-uniformity (such as HgCdTe photodetectors), the NEΔT is limited by the spatial noise and not by the background shot noise. However, the spatial noise can be made insignificantly small by incorporating an efficient on-focal-plane background suppression scheme (κ ≈ 1), thereby allowing the readout system to operate at BLIP.

2.2 A background suppression circuit

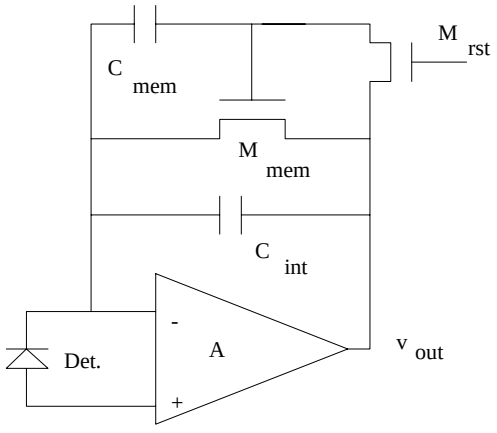

Figure 1: Schematic of a current-mode background suppressing scheme.

An in-pixel current-mode background suppression circuit is shown in figure 1. The circuit is based on the commonly used charge transfer impedance amplifier (CTIA) unit cell design. The background suppression is achieved by the addition of a current memory consisting of a transistor (M_{mem}), a memorizing capacitor (C_{mem}) and the reset switch (M_{rst}). The circuit operates in two modes, the reset mode and the readout mode. The reset phase of the CTIA (i.e. the switch M_{rst} closed) is also used as a calibration cycle during which the array is made to stare at an equivalent background scene. The transistor M_{mem} is biased with its gate-and-drain short-circuited and the background current flowing from the detector is coupled to it. The gate-to-source voltage of the transistor charges to the level required to maintain the current flow and is stored on the capacitor C_{mem}. During the readout phase, the

switch M_{rst} is open, and the voltage stored on the capacitor C_{mem} drives a current through M_{mem} equal to the background current sampled during the calibration cycle. Thus, the share of the detector current that is due to the background flux is bypassed through the transistor M_{mem}, thereby completing the in-pixel background subtraction.

2.3 Current memory design and performance

The critical component of the current-mode background suppression circuit is the current memory. The main sources of error in the current memory [9] is due to the charge feedthrough that takes place following the opening of the switch M_{rst}, and the finite output resistance of the memorizing transistor M_{mem}. The effect of the finite output resistance is to introduce a discrepancy between the channel current flowing in the calibration mode and the readout mode, due to the presence of different drain voltages on the two occasions. The error caused by the output resistance can be made negligible by using cascode circuits [9]. The charge feedthrough-related error is proportional to g_{mm}/I, where g_{mm} is the transconductance of the memorizing transistor and I is the background current. Typical values of the background current to be memorized are between 1 nA and 100 nA. For such low values of current, M_{mem} operates in weak-inversion, thereby maximizing charge feedthrough-related error, since g_{mm}/I is maximized in weak inversion. Further, accurate switch feedthrough reduction circuits are designed for operation at relatively large memorizing currents, require high power dissipation and real-estate [10,11], and are therefore unsuited for focal-plane use.

A novel switch feedthrough reducing, output resistance enhancing current memory circuit, capable of operation at ultra-low current levels (1-500 nA) and compatible with focal-plane design requirements, has been designed, fabricated and tested. The circuit is shown in figure 2. The output resistance of the current memory is increased by using a self-cascoding FET (M_{mem}) [8]. The self-cascoding FET (SCFET) consists of two common-gate transistors connected in series. The transistor with the shorter channel length is the cascode transistor. When the SCFET is biased in weak- or moderate-inversion, the cascode transistor remains in saturation and acts as a screen gate in a manner similar to the operation of the cascode transistor in a conventional cascode circuit. However, unlike a conventional cascode circuit, the SCFET does not require additional bias supply lines or extra real-estate, and is perfectly suited for low-power operation.

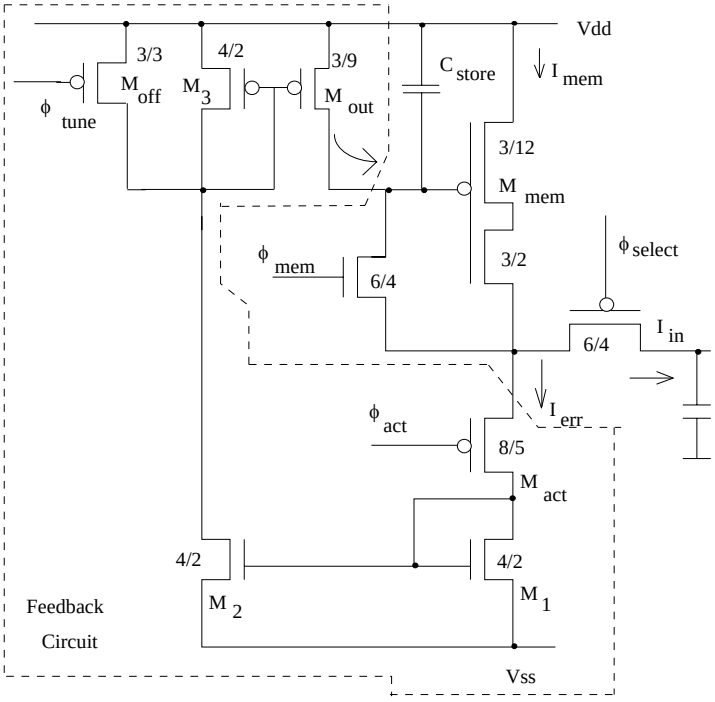

Figure 2: Schematic of a current-error feedback switch feedthrough reduction circuit.

The switch feedthrough reduction scheme operates by feeding the error current back to the controlling node. Following the memorizing cycle, ϕ_{mem} is turned off, causing a switch feedthrough on the charge storage node. The switch feedthrough is in a direction as to increase the current flowing through M_{mem}. This is followed by the feedthrough suppression cycle in which M_{off} is turned off, and M_{act} is turned on. The error current (I_{err}) flows through M_1, and is mirrored into M_{out}. The mirror ratio is such that only a fraction α of I_{err} flows through M_{out}, which is directly coupled to the storage capacitor (C_{store}). As a result of this feedback I_{err} is reduced, with a concomitant reduction in the current through M_{out}. In principle,. the current goes to zero when the error current vanishes, (i.e. $I_{mem} = I_{in}$). In practice, a tail current flows through M_{out} due to threshold mismatch and weak-inversion current. To circumvent the error caused by this current, M_{out} is shut off once the error has been reduced within a given accuracy limit. By writing the differential equation describing the negative feedback process, it can be shown that the error current as a function of time follows an exponential decay given by:

$$I_{err}(t) = I_{err}(0)\exp\left(- \frac{g_{out} + \alpha g_{mm}}{C_{store}}.t \right) \cong I_{err}(0).\exp\left(- \frac{\alpha g_{mm}}{C_{store}}.t \right) \quad (2)$$

where g_{mm} is the transconductance of the memorizing FET. There is a trade-off between the speed of feedthrough reduction and the residual accuracy, since this circuit is devoid of mechanisms to correct for overshoots. The feedback circuit was designed with α=0.5 in order to strike a compromise.

2.4 Current memory test results

The current memory cells were laid out using a CAD layout tool MAGIC and fabricated using the ORBIT 2 μm CMOS technology through the MOSIS fabrication service. A 16X1 array was fabricated with a cell size of 47X43 μm^2. A test circuit was included in the chip for inputting current into the memory cells and for measuring the output current using a reset integrator. The output of the reset integrator was monitored on an oscilloscope. The I-V characteristic of the SCFET was measured using a HP 4145 data analyzer. The results are summarized below.

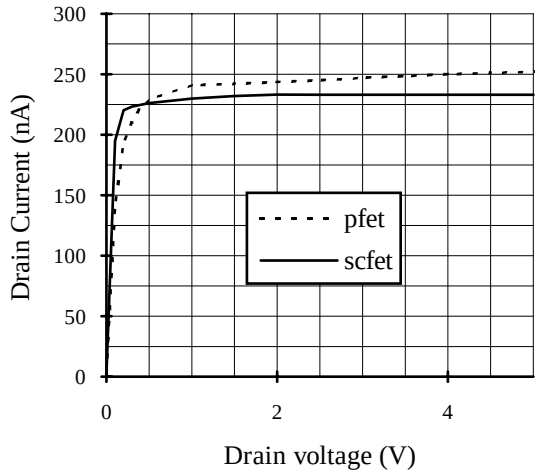

Figure 3: Measured IV characteristics of a SCFET.

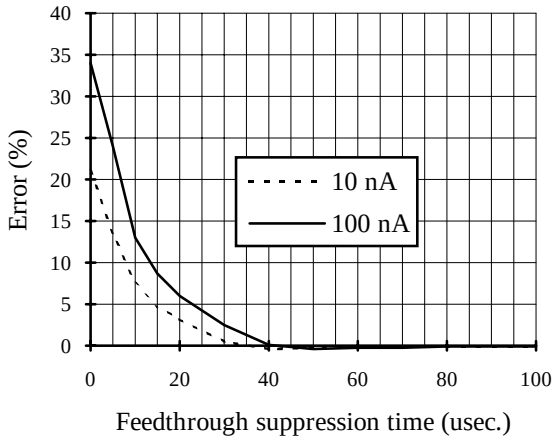

Figure 4: Measured error characteristics of the feed-through suppressed current memory vs. feedthrough suppression time.

Figure 3 shows the measured I-V characteristics of the SCFET and a p-FET of same dimensions. The increase in the output resistance due to cascoding action is evidenced by the flatter trace of the SCFET characteristics. For p-channel transistors, the increase in the output resistance by the SCFET is measured to be 22.5 times. The increase is only 15 times for n-channel transistors. Although the increment in output resistance is smaller than that using a conventional cascode circuit, it is estimated to be enough to reduce the error in the current memory due to finite output resistance below the resolution of the test set-up (which is 0.1%).

The error characteristics of the current memory circuits were measured by memorizing a current and subsequently performing a readout through the reset integrator. It was found that the relative error between two different current memory cells was always too small to be measured by our test setup. The performance of the feedthrough suppression circuit was studied for different lengths of feedthrough suppression cycles, and for different values of memorizing currents. The result, plotted in figure 4, is for two current levels (I= 10 nA, and I=100 nA). The absolute residual error was found to be less than 0.1% (i.e. below the test set-up resolution) for feedback times greater than 45 μsec. with the memorizing current varying from 10 nA to 100 nA. The error decay is nearly exponential as predicted by the equation 2.2. The deviation from the exponential decay as well as the value of the time constant predicted by the equation 2 is explained by the presence of a large displacement current caused by a large output capacitance of the test structure.

The storage times of the memory cells were measured to be 0.06 sec. (0.1% decay) at room temperature. This is well beyond the typical pixel integration times encountered in high background applications. Further, the storage time exhibited a strong temperature dependence, increasing exponentially with decreasing temperature, doubling every 7.9 K, and is found to be generation limited. The projected storage time at 100 K is 25.2 days.

3. ON-FOCAL-PLANE COLUMN-PARALLEL ADC

3.1 Sigma-delta (Σ-Δ) modulation

The rationale for using an on-focal-plane ADC is to enhance sensor performance by reducing noise introduced in transmitting analog signals off focal-plane. To eliminate EMI-related signal degradation, for simplified and more reliable system interfacing, and to partially suppress cross-talk noise, a column-parallel ADC implementation is explored.

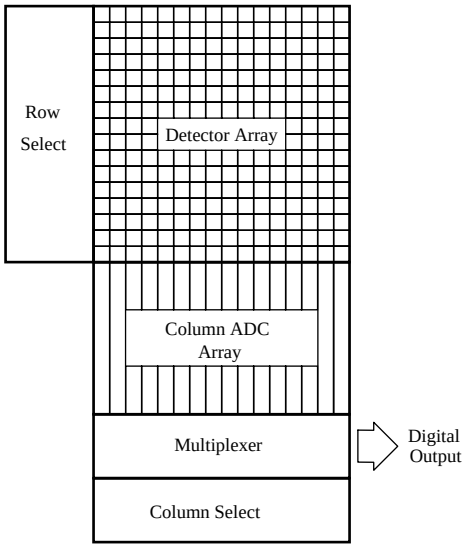

Figure 5: Semi-parallel architecture for focal-plane A/D conversion.

The choice of a focal-plane ADC architecture is governed by the requirements of low-power, small real-estate and device parameter insensitivity. A Σ-Δ modulation based ADC was chosen since it has been proven to be well-suited for VLSI implementations where high conversion rate is not a requirement [12]. Due to the averaging nature of Σ-Δ ADCs, it is more tolerant to threshold variations and inadvertent comparator triggering than slope-based ADCs. Unlike successive approximation methods, it does not require critical component matching, and compared to

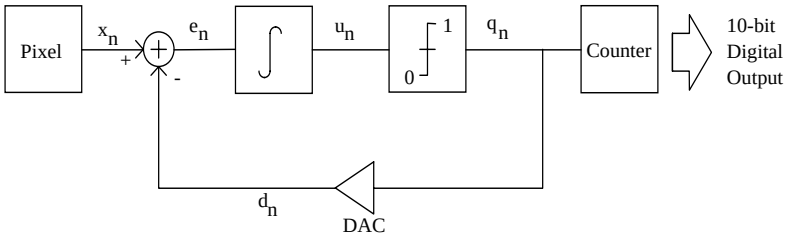

Figure 6: Block diagram of a first order Σ-Δ ADC.

flash ADCs, it uses less power and area. A column parallel architecture shown in figure 5 was used in the design in order to reduce the conversion rate of each ADC (compared to the case where the entire array is serviced by a single ADC). Another attractive feature of Σ-Δ ADC is that the conversion rate can be further decreased by cascading two or more first order Σ-Δ ADCs [13]. Such implementations are compatible with column-parallel ADC architecture.

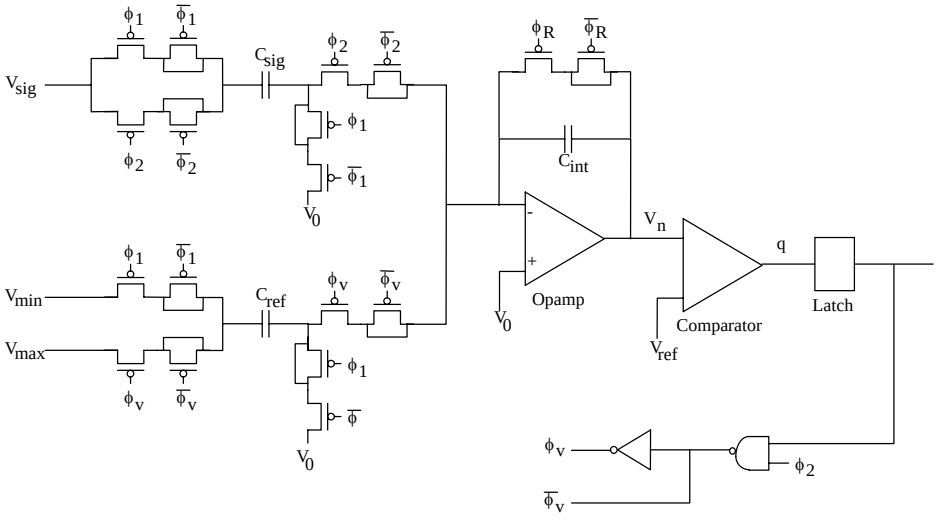

Figure 7: Switched-capacitor implementation of sigma-delta modulator.

Σ-Δ modulation combines oversampling and feedback to increase the correlation between samples and decrease the quantization error. Figure 6 shows the schematic diagram of a first order Σ-Δ ADC. The main components of a first order Σ-Δ ADC are an integrator, rough two-level quantizer (comparator), and a two-level DAC (implemented by an analog switch that selects between two analog levels V_{min} and V_{max}, depending upon output (q_n) of the comparator. The DAC is placed in the feedback loop, and its output is fed back and subtracted from the input sample. The error sample is integrated and thresholded. The repeated

integration and feedback force the average value of the DAC to track the average value of the signal. As a result of the averaging nature of the ADC, all wideband system noise is suppressed.

3.2 Σ-Δ modulator circuit

The Σ-Δ modulator was implemented with a switched capacitor integrator and comparator as shown in figure 7. The integrator has two branches, one to add signal and the other to subtract the full scale. The capacitors (C_{sig}, C_{int}, C_{ref}) are implemented with two-poly levels, and are of size 1 pF. The choice of capacitor size involves a trade-off between power dissipation and tolerable kTC noise. The op amp is implemented with SCFETs described in the previous section and will be presented in greater detail in the next section. Since the ADC operates in column-parallel mode, it needs to be laid out with a 50 μm pitch as shown in figure 5. The detailed design considerations of the first-order Σ-Δ ADC is presented elsewhere [14].

4. IN-PIXEL SIGNAL DIGITIZATION

4.1 Photoelectron counting readout

One of the major sources of noise in the most advanced IR multiplexers is the random noise introduced from clocking signals. This noise can be suppressed using multiple correlated non-destructive read techniques (MCS) [15], albeit at the cost of increased system size, focal-plane power dissipation and the reduced readout rate. Further, MCS does not reduce the MOSFET 1/f noise that is critical for low-light-level signal detection involving long integration times. Thus, even in the most advanced IR readout-multiplexers, the noise floor is 10 electrons r.m.s.

The multiplexer noise can be eliminated by incorporating an ADC in each pixel, but is unattainable using conventional ADC techniques because of power and real-estate limitations. A novel approach of in-pixel digitization of signal is to count photoelectrons within the unit cell, so that the readout is noise free. Further, using this approach, the 1/f noise is kept at minimum by minimizing the effective integration time (the integration time in photon counting readout being equal arrival times of photons). The schematic of the photoelectron counting unit cell is shown in figure 8.

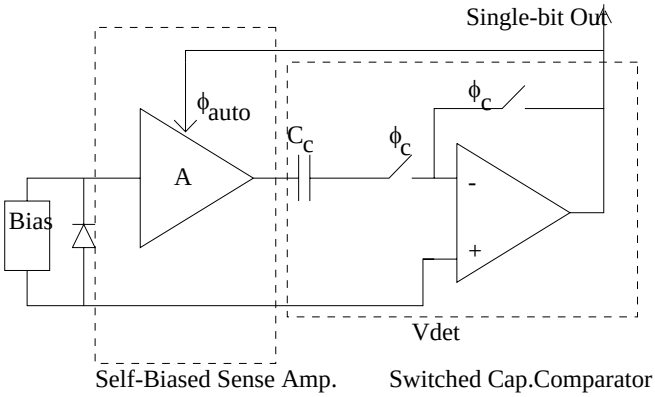

Figure 8: Schematic of a photoelectron detecting unit cell.

The photon detecting readout unit cell consists of a sense amplifier, a switched-capacitor comparator. The sense amplifier must have self-biasing capability in order to eliminate the kTC noise associated with resetting the detector. Further, it must have high enough gain (> 5000) so that the amplified voltage step due to a single electron may be larger than the offset in the comparator. Further, the sense amplifier must have sub-electron input-referred noise and must operate with extremely low power dissipation (< 5 μW). The switched-capacitor comparator operates in a manner similar to a CDS circuit. During the time interval the comparator is reset (ϕ_C closed), it memorizes the d.c. output level of the sense amplifier, and subsequently uses it as the discrimination level, thereby eliminating reset noise and further suppressing 1/f noise. Finally, to generate a digital word proportional to the incident photon flux, the single-bit output of the unit cell is used to update the contents of a separate counter array, located below the photoelectron detecting unit cells.

The unit cell comprising of the sense amplifier and the comparator can be laid out in a 60X60 μm^2 area using 2 μm CMOS design rules. Although this is large compared to state-of-the-art IR readout unit cell dimensions, the photon counting readout unit cell size can be readily reduced to a mere 25X25 μm^2 by using 0.8 μm design rules. One of the main reasons behind the feasibility of this readout approach is the fact that the minimum feature size of state-of-the-art CMOS

technology continues to shrink at an exponential rate, while the size of the imager pixel, determined by optics, is expected to remain relatively constant in size.

4.2 Design of sense amplifiers

Both single-ended and differential sense amplifiers have been explored. The common features of these amplifiers are summarized in the foregoing section. The single-ended amplifier consists of a self-biased cascode stage implemented with transistors M_1, M_c, M_L (figure 9). In this circuit both the cascode and the load bias are generated by shorting the gate and the drain of M_c and M_L, and storing it on the capacitor C_s. The gain of each stage is ~ 60, so that a two-stage cascade of single-ended amplifiers is required for implementing the sense amplifier.

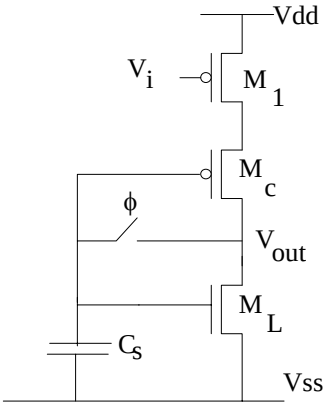

Figure 9: Circuit Diagram of self-biased cascode inverting amplifier.

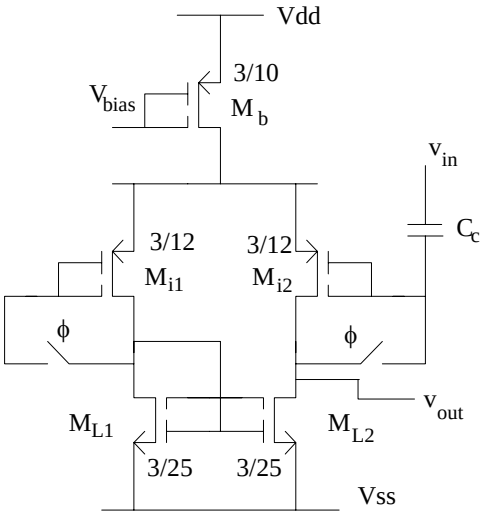

Figure 10: Circuit diagram of a high gain SCFET differential amplifier.

In order to detect ultra-low flux levels (photon flux < 1000 per-pixel per-sec.), the sense amplifiers are required to operate with response times of > 0.1 msec. [8]. For an amplifier to operate with such long response times and a small load capacitor, its output resistance needs to be increased. This is accomplished by using a double-cascode circuit implemented with SCFETs as shown in figure 10. A differential topology is used for increasing power supply rejection ratio, for independently controlling the amplifier bandwidth, and for implementation of a novel switch feedthrough reduction scheme. In the circuit shown in figure 10, $M_{i1}$and M_{i2} constitute the SCFET input transistors, $M_{L1}$and M_{L2} constitute the SCFET load transistors, and M_b is the biasing transistor. In a high gain amplifier, the switch feedthrough caused by the shutting off of ϕ can saturate the amplifier. The amplifier circuit shown in figure 10 is equipped with a novel switch feedthrough reduction scheme. Since the amplifier has a large common mode rejection ratio, the switch feedthrough is suppressed by allowing it occur in common mode.

The self-biasing operation is also equivalent to sampling and subtracting the MOSFET channel noise, thereby suppressing any correlated noise such as the 1/f noise. The noise analysis of a self-biased amplifier has been carried out and a closed-form expression of input-referred noise has been derived [8]. Using the results presented in reference 8, the expression for the input-referred noise can be written as:

$$\begin{aligned}\left(\overline{v_n^2}\right)_i &= \frac{\frac{4}{3}kT\left(g_{m1}+g_{mL}\right)}{g_{m1}^2}\pi f_c + \frac{I_b}{g_{m1}^2}\left(\frac{K_{fp}}{L_1^2}+\frac{K_{fn}}{L_L^2}\right)\left[\ln\left(\frac{T_s}{2t_r}\right)+1.85\right] \\ &= \frac{2kT\left(1+\frac{g_{mL}}{g_{m1}}\right)}{t_r\sqrt{2\mu C_{ox}\frac{W_1}{L_1}I_b}} + \frac{1}{C_{ox}\mu\frac{W_1}{L_1}}\left(\frac{K_{fp}}{L_1^2}+\frac{K_{fn}}{L_L^2}\right)\left[\ln\left(\frac{T_s}{2t_r}\right)+1.85\right]\end{aligned} \tag{3}$$

where g_{m1} and g_{mL} are the transconductances of the input and the load FETs, t_r is the response time, f_c is the cut-off frequency of the amplifier, T_s is the sample period, L_1 and L_2 are the channel lengths, μ is the mobility, C_{ox} is the oxide

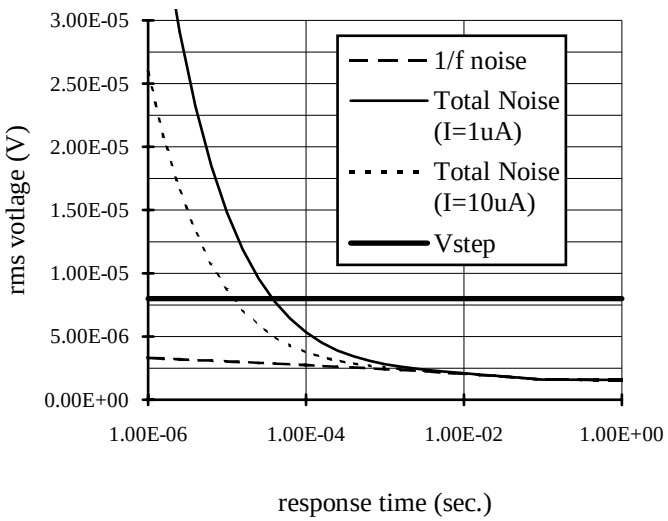

Figure 11: RMS noise voltage vs. response time.

capacitance per unit area, and K_f's are the flicker (1/f) noise coefficients. The equation 3 indicates that by lowering the input transconductance and by reducing the operating temperature, the input-referred noise of the amplifier can be decreased. This design equation allows the choice of an optimum channel length and width for maximizing the signal-to-noise ratio. Using this equation the input-referred noise of the amplifier has been calculated. Figure 11 shows the different components of noise as a function of the response time. The input capacitance is assumed to be of size 20 fF (which is a typical value). From figure 11 it can be concluded that sub-electron input-referred noise can be obtained over a large range of response times, and correspondingly for a large range of incident flux densities. Further, it can be seen that the 1/f noise is reduced to an insignificant amount by the self-biasing operation.

4.3 Results and discussion

A 16X2 array consisting of single-ended and high-gain differential amplifiers were fabricated using ORBIT 2 μm CMOS process offered through MOSIS. The frequency response and the noise spectrum of these amplifiers were measured at room temperature. The circuits performed as expected.

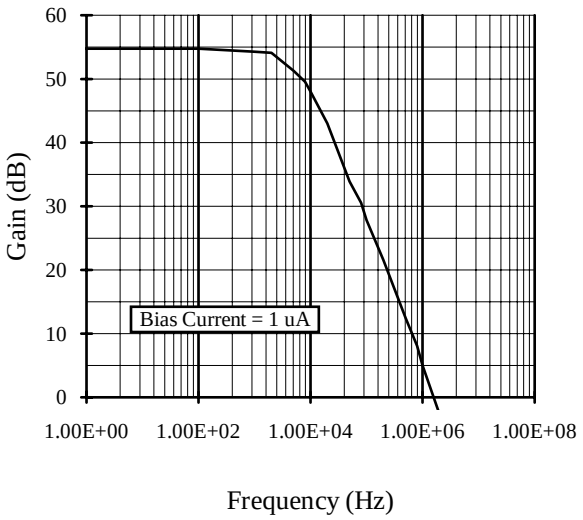

Figure 12: Transfer function of SCFET differential amplifier.

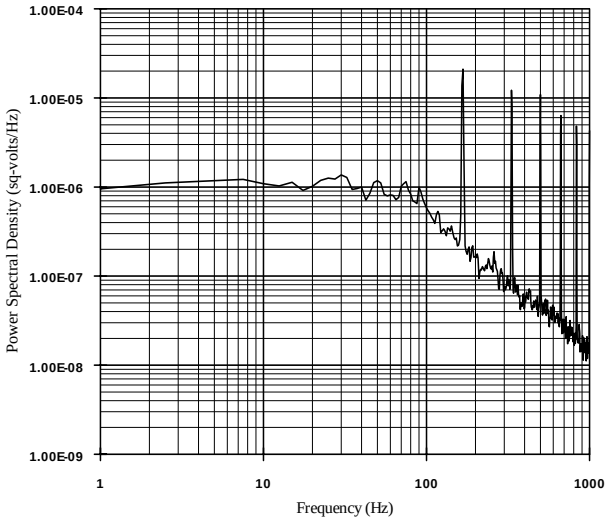

Figure 13: Output noise power spectral density of two-stage amplifier (sample rate = 166.3 Hz).

The single-ended amplifier exhibited an input d.c bias range between 1.05 to 1.65 V, with a gain of 56 and gain variation of <10%. The transfer characteristic of the self-biased differential amplifier is shown in figure 12. The low frequency gain is extremely high for a single-stage operating at room temperature being close to 500 at 1 μA of bias current, and can be further decreased by lowering the bias current. Thus, through the incorporation of the SCFET, the gain has been increased by approximately a factor of 10, further corroborating results obtained in figure 3. Further, the measured transfer function is characterized by a single pole response and the measured phase margin is 55°, indicating that the differential amplifier is unconditionally stable.

Figure 13 shows the measured output noise power spectral density of the single-ended, two-stage, self-biased amplifier operating with a 166.3 Hz sample rate. It can be seen that the power spectral density is flat at low frequencies, indicating the 1/f noise suppression capability of the circuit. For the measured two-stage amplifier gain is 2538.31, and the calculated storage capacitor size of 260 fF, the noise power calculated from the measured power spectral density (shown in figure 13), is almost entirely accounted for by the reset noise on the storage capacitor. The reset noise can be easily eliminated by using CDS-like circuits (such as the switched-capacitor comparator), leading to extremely low-noise amplifier performance.

5. CONCLUSIONS

In conclusion, low-power low-noise circuits for enhancing IR focal-plane imager performance are presented. A current-mode background suppressing readout scheme using current memory and CTIA is described. New current memory circuits were designed and tested for operation at ultra-low currents. The current memory circuits operate with $< 0.1\%$ error over a current range of 10-200 nA, thereby allowing the in-pixel background suppression circuits to operate with a thousand-fold background suppression capability. On-focal-plane digitization schemes are presented for reduction of system noise required in ultra-low-IR-signal detection. The first approach features implementation of a first order Σ-Δ ADC operating in column-parallel mode that is currently being tested. A more novel approach involves counting photoelectrons within each readout pixel. The low-noise, high-gain, low-power, self-biased operation of unit cell sense amplifiers has been demonstrated. For further improvement of signal-to-noise ratio, low temperature operation and the use of input-transconductance enhancing circuits are currently under investigation. For reducing real estate requirements, an ultra high gain amplifier implemented with controlled positive feedback is being explored.

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7. REFERENCES

1. J. Woolaway, "New Sensor Technology for the 3- to 5- μm Imaging Band," Photonics Spectra, vol. 26, pp. 113-119, 1991.
2. J. Mooney, F. Shepherd, W. Ewing, J. Murguia, and J. Silverman, "Responsivity Non-uniformity Limited Performance of Infrared Staring Cameras," Opt. Eng., vol. 28, pp. 1151-1161, 1989.
3. A. Fowler, R. Joyce, I. Gatley, J. Gates, and J. Herring, "Evaluation of a 256 x 256 PtSi Array for Infrared Ground Based Astronomy," Proc. SPIE, vol. 1107, pp. 22 - 31, 1989.
4. E. Fossum, "Future Directions in Focal-Plane Signal Processing for Spaceborne Scientific Imagers, Proc. SPIE, vol. 1541, pp. 62 - 67, 1991.
5. N. Bluzer and A. Jensen, "Current Readout of Infrared Detectors," Opt. Eng., vol. 26, pp. 241-248, 1987.
6. D. Scribner, M. Kruer, and J. Killiany, "Infrared Focal Plane Array Technology," Proc. IEEE, vol. 79, pp. 66-85, 1991.
7. W. Kosonocky, "A Review of Infrared Image Sensors with Schottky-Barrier Detectors," Optoelectron. Devices and Tech., vol. 6, no. 2, pp. 173-203, 1991.
8. B. Pain, "*Low-Noise CMOS Circuits for On-Chip Signal Processing in Focal-Plane Arrays*," Ph.D. Dissertation, Columbia University, New York, 1993.
9. S. Daubert and D. Vallancourt, "Operation and Analysis of Current Copier circuits," Proc. IEEE, vol. 137, pp. 109-110, 1990.
10. G. Wegmann and E. Vittoz, "Analysis and Improvements of Accurate Dynamic Current Mirrors," IEEE J. Solid-State Circuits, vol. SC-25, pp. 699-705, 1990.
11. H. Lie, "Switched Capacitor Feedback Sample-and-Hold Circuit," U.S. Patent 4 585 956, Apr. 1986.

12. J. Candy and G. Temes, "Oversampling methods for A/D and D/A conversion," *Oversampling Delta-Sigma Data Converters*, IEEE Press, pp. 1-25, New York, 1992.
13. J. Robert and P. Deval, "A Second-Order High-Resolution Incremental A/D Converter with Offset and Charge Injection Compensation", IEEE J. Solid State Circuits, vol. SC-23, pp. 736-741, 1988.
14. S. Mendis, B. Pain, R. Nixon, and E. Fossum, "Design of a Low-Light-Level Image Sensor with On-Chip Sigma-Delta Analog-to-Digital Conversion", Proc. SPIE, vol. 1700, pp. 19-31, 1993.
15. A. Fowler and I. Gatley, "Noise Reduction Strategy for Hybrid IR Focal Plane Arrays," Proc. SPIE, vol. 1541, pp. 127-133, 1991.