Low-Light-Level Image Sensor with On-Chip Signal Processing

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ABSTRACT

The design of a low-light-level CMOS active-pixel-sensor (APS) with on-chip, semi-parallel analog-to-digital (A/D) conversion is presented. The imager consists of a 128x128 array of active pixels at a 50 μm pitch. Each column of pixels shares a 10-bit A/D converter based on first-order oversampled sigma-delta (Σ-Δ) modulation. The 10-bit outputs of each converter are multiplexed and read out through a single set of outputs. A semi-parallel architecture is chosen to achieve 30 frames/second operation even at low light levels. The sensor is designed for less than 10 e^- rms noise performance. A 28x28 active-pixel-sensor (APS) with 40x40μm^2 pixels as well as individual elements of the sigma-delta modulator have been fabricated and tested using MOSIS* 2 μm CMOS technology.

1. INTRODUCTION

On-chip analog-to-digital (A/D) conversion can be used to improve sensor performance by minimizing read out noise introduced in transmitting analog signals off the focal plane. A focal-plane A/D converter has to be robust, low-power and compact. The architecture chosen to implement focal-plane A/D conversion for low-light-level imaging is a semi-parallel approach using first-order sigma-delta modulation and an array of active pixel sensors (Figure 1).

The semi-parallel architecture was chosen as a trade-off between a serial system with a single A/D converter and a completely parallel system with an A/D converter for each pixel. A major disadvantage of the serial system is that it requires high operating speeds since conversion of each pixel must be done sequentially. This in turn introduces resolution problems due to the limited accuracy attainable at high conversion rates. On the other hand, a completely parallel system reduces the required operating speed but requires too much area to be included in each pixel. With a semi-parallel architecture, where an entire column of pixels shares a single A/D converter, the area available for each converter is limited primarily by the pixel pitch, and the number of conversions is proportional to the number of rows rather than the total number of pixels.

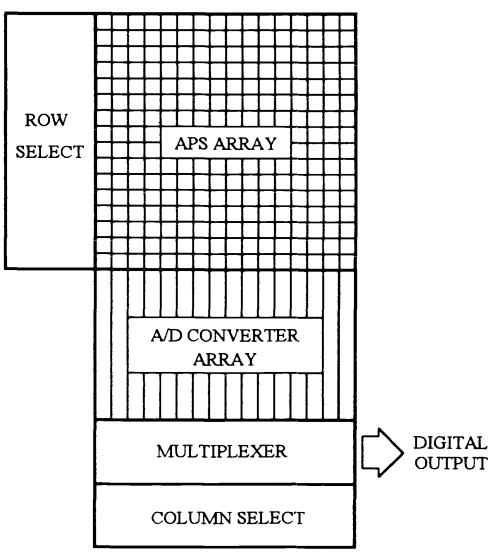

Figure 1: Semi-parallel architecture for focal plane A/D conversion.

A/D conversion based on oversampled sigma-delta (Σ-Δ) modulation was selected since it has been proven to be well suited for VLSI applications where high conversion rate is not a requirement [1]. Due to the averaging nature of sigma-delta modulation, it is more robust against threshold variations and inadvertent comparator triggering than single-slope/dual-slope methods and requires less component accuracy than successive approximation methods. It also uses less power and real estate than flash A/D converters. A semi-parallel architecture with an array of A/D converters reduces the conversion rate of each converter sufficiently to allow the use of sigma-delta modulation. Sigma-delta modulation is suitable for VLSI circuits since it is easier to achieve high oversampling ratios than to produce precise analog components in order to reduce component mismatch.

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First-order sigma-delta modulation with a single-bit or two-level quantizer is used for the A/D converter since it is simple, compact, robust and stable against overloading. The output of such a modulator can be filtered by taking a simple average over a fixed number of bits. To generate an N-bit digital word, 2^N output bits are averaged for each pixel [2].

Active-pixel-sensor (APS) arrays operating at video rate are particularly suitable for low-light-level imaging where signal levels are typically only a few tens to hundreds of electrons. An active-pixel-sensor has active transistors within the unit cell which allow random access and read out of the signal over a metal wire [3]. This eliminates signal degradation due to charge-transfer inefficiency suffered by CCD imagers where signal charge is read out sequentially by transferring it through the semiconductor. The APS helps overcome this problem, especially for low-light-level applications where pixel dimensions are large.

This paper presents the design of a CMOS compatible focal-plane A/D converter for an active-pixel-sensor imager. Relevant background information on A/D conversion based on first-order sigma-delta modulation is presented. The system architecture and design considerations of the active-pixel-sensor array and the A/D converter are discussed. The projected performance of the system and initial results of an APS test chip are presented and current research is summarized.

2. SIGMA-DELTA MODULATION

2.1 Background

Since its introduction 30 years ago [4], oversampled sigma-delta modulation has become a popular method for A/D conversion. Sigma-delta modulation uses oversampling and integration of the signal prior to quantization to increase the correlation between samples and decrease the quantization error. The main components of the first-order sigma-delta modulator are the integrator, quantizer and feedback D/A converter as shown in Figure 2(a). The quantities x_n, u_n, q_n and e_n are respectively, the input, integrator output, quantizer output and quantizer error during the n-th cycle.

During each pixel conversion period, the input to the sigma-delta modulator is the analog output signal from the pixel, which remains nearly constant at a value between 0 and x_{max}. The two level-quantizer is a comparator with a threshold equal to V_{ref} corresponding to x_{max}, and output levels corresponding to a digital "1" and "0". In this case, the feedback D/A is a switch that chooses between two preset levels depending on the comparator output q_n.

The operation of the sigma-delta modulator is illustrated in Figure 2(b). During each cycle, the integrator adds the current input x_n to the previous output. When the integrator output crosses the comparator threshold, an amount equal to the full scale x_{max} is subtracted during the following cycle. Therefore, the output q_n oscillates between "0" and "1" such that the average over many cycles is approximately equal to the input. This can be summarized by the recursive relations

$$\begin{aligned} u_n &= u_{n-1} + e_{n-1} \\ e_{n-1} &= x_{n-1} - d_{n-1} \end{aligned} \tag{2.1}$$

where

$$\begin{aligned} d_{n-1} &= 0 \quad \text{for } q_n = 0 \\ d_{n-1} &= x_{max} \quad \text{for } q_n = 1 \end{aligned}$$

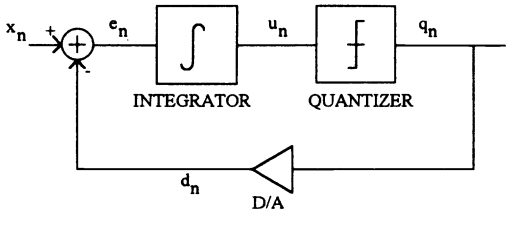

Figure. 2(a): First-order sigma-delta modulator with a two level quantizer

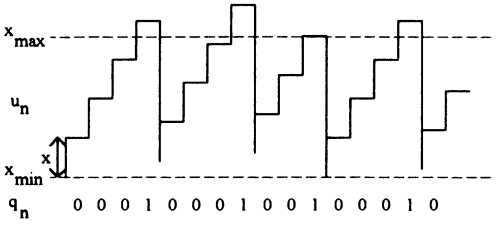

Figure 2(b): Simulated integrator output u_n and comparator output q_n for a constant input x.

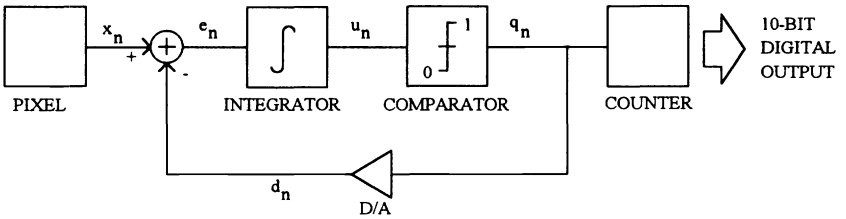

Figure 3: Block diagram of A/D converter

In this design, q_n is averaged over 1024 samples by counting the number of "1"s using a 10-bit ripple counter. The block diagram for this system is shown in Figure 3.

2.2 Quantization noise in sigma-delta modulation

Quantization noise in sigma-delta modulation depends on the order of the modulator as well as the type of filter used to decimate the signal. In [1], the rms noise in the signal band in a first-order sigma-delta modulator with a busy input is expressed as

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}(OSR)^{-3/2} \tag{2.2}$$

where OSR is the oversampling ratio defined as the ratio between the sampling frequency and the Nyquist frequency of the input signal. This derivation assumes that the quantization noise can be represented by an additive white noise source with equal probability of lying in the range $\pm\Delta/2$, and rms value $e_{rms} = \Delta/\sqrt{12}$. The average signal-to-noise ratio is then predicted as

$$\frac{\Delta}{n_0} = \frac{6}{\pi}(OSR)^{3/2} \tag{2.3}$$

which improves by 1.5 bits for each doubling of the oversampling ratio. When the output signal is averaged over each Nyquist interval, the noise in the signal band is

$$n_0 = \sqrt{2}e_{rms}(OSR)^{-1} \tag{2.4}$$

and the average signal-to-noise ratio is

$$\frac{\Delta}{n_0} = \sqrt{6}(OSR) \tag{2.5}$$

which corresponds to approximately 9.5 bits of accuracy for an oversampling ratio of 1024. Although a constant input does not satisfy the assumptions made in the derivation in [1], it has been shown in [5] that the results may still hold.

Quantization noise in a first-order sigma-delta modulator with a constant input is also highly dependent on the input level [1]. Analysis of such pattern noise can be found in references [1], [5] and [6].

3. DESIGN

3.1 Architecture

The chip consists of an imaging area, an array of A/D converters with multiplexed outputs, and control circuits for row and column selection as shown in Figure 1. The imaging area is a 128x128 array of active pixel sensors which is scanned row by row. The row-control circuits decode the 7-bit row-address and provide the clock signals needed by each row of pixels. Each column of pixels shares a single A/D converter and the array of converters operate in parallel to convert a row of pixel outputs. Each A/D converter consists of a first-order oversampled sigma-delta modulator whose output is averaged by a 10-bit counter. The counter outputs are latched at the end of each conversion period and read out while the next row is being converted. The column control circuit decodes the 7-bit column address for the readout operation.

The circuits were designed for a 2 μm double-poly CMOS process for fabrication through the MOSIS foundry service. With these design rules, the total chip area is approximately 7 mm x 10.4 mm. Of this, the APS array occupies an area of 6.4 mm x 6.4 mm and each sigma-delta modulator circuit occupies an area of 50 μm x 3.7 mm to fit within the column pitch of 50 μm.

3.2 CMOS Active Pixel Sensor

The active pixel sensor in the imager is effectively a single charge-coupled-device (CCD) stage with a reset transistor, an input transistor of a source-follower and a row-select transistor. The output is either a floating-gate (Figure 4(a)) or a floating-diffusion (Figure 4(b)) structure. In either case, the circuitry shown within the dotted line is contained in each pixel unit cell, and the source-follower load shown outside the dotted line is common to a column of pixels. The CCD stage is implemented using conventional CMOS technology, and consists of a photo-gate (PG), transfer-gate (TX) and the output structure. The pixel with a floating-gate output contains an anti-blooming gate and drain (ABG and ABD) which are also used to reset the pixel. In the pixel with a floating-diffusion output, the design of the reset transistor results in a lateral anti-blooming drain.

During the signal integration period, photo-generated signal-charge is collected under the photo-gate. The anti-blooming structure in each pixel prevents a full well from over-flowing into adjacent pixels. When the pixel is ready to be read out, the row-select transistor for that row is turned on and all the other rows turned off.

In the floating-gate pixel, the photo-gate is pulsed repeatedly to move the signal-charge back and forth from the photo-gate to the floating-gate. The output swings between two levels which are sampled at the input to the sigma-delta modulator (Figure 4(c)). Reset noise is eliminated by this operation since the output signal is read differentially, and 1/f noise is reduced since the signal is modulated at the oversampling rate. The multiple read operation also reduces white noise. The floating gate is reset once per frame to ensure that its voltage does not drift beyond the input range of the sigma-delta modulator.

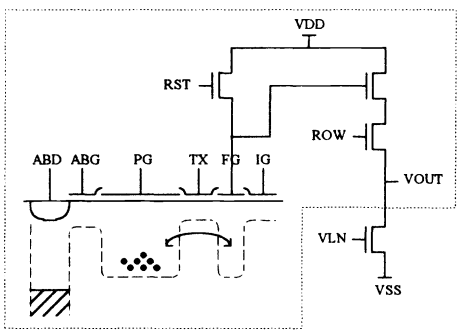

Figure 4(a):Active-pixel-sensor unit-cell with floating-gate output.

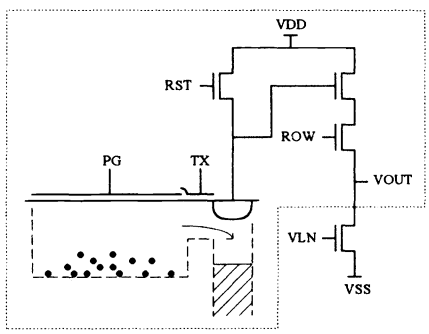

Figure 4(b):Active-pixel-sensor unit-cell with floating-diffusion output.

In the floating-diffusion pixel, the reset level and signal level are stored on two sampling capacitors, and these values are sampled repeatedly by the sigma-delta modulator. Similar to the floating-gate pixel, reset noise is eliminated as the output is read differentially. However, the reduction of 1/f noise is less and the sampling capacitors add another source of kTC noise.

The dimensions of the transistors within the unit cell need to be small to maintain a reasonably large fill factor which is defined as the ratio of the photo-gate area to the pixel area. On the other hand, the transistors of the source-follower need to be large enough to drive the switched capacitors on the sigma-delta modulator at the oversampling rate, and to reduce the 1/f noise contribution. The sensitivity (S) of the detector is given by

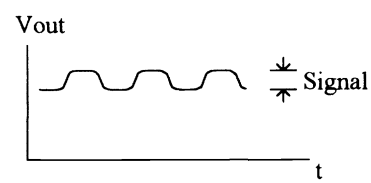

Figure 4(c): Pixel output voltage.

$$S = \frac{q}{C_{out}} A_0 \tag{3.1}$$

where q is the electron charge, C_{out} is the capacitance of the output node and A_0 is the gain of source follower.

A 50x50 μm^2 floating-gate pixel designed with 2 μm design rules has a fill-factor of 30% . A similar floating-diffusion pixel has a fill-factor of 40%. Using smaller design rules can reduce the pixel size or dramatically increase the fill-factor as shown in Figure 6. Moving from 2 μm design rules to 0.8 μm design rules reduces the pixel size from 50x50 μm^2 to 20x20 μm^2 or increases the fill-factor from 30% or 40% to almost 90%. It can also improve the sensitivity as the output node capacitance is reduced.

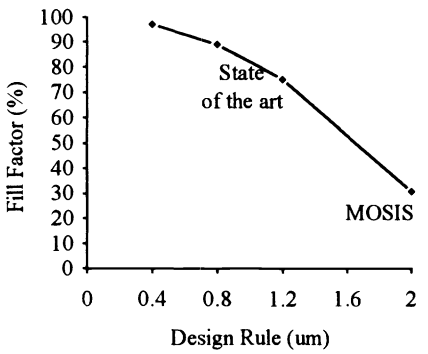

Figure 5(a): Fill-factor vs. design rule for a 50 μm x 50 μm pixel.

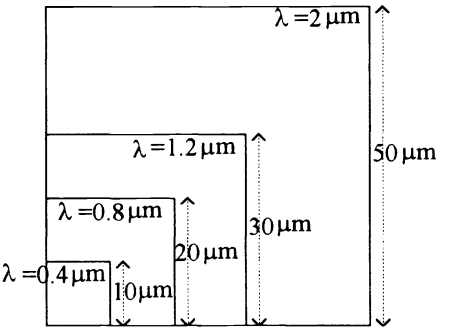

Figure 5(b): Pixel size scaling with design rule for a fill-factor of 30%.

3.3 A/D Converter

The A/D converter has two parts: the sigma-delta modulator which is implemented with a switched-capacitor circuit and the filter which is implemented with a counter.

3.3.1 Sigma-delta modulator circuit

The sigma-delta modulator is implemented with the switched capacitor integrator and comparator shown in Figure 6. The integrator has two input branches, one to add the signal and the other to subtract the full scale. P-type MOSFET switches are used since they show better noise performance than N-type switches. MOS capacitors which are controlled by complementary clock signals are included in the signal path to reduce switch feed-through. The switched-capacitors C_{sig} and C_{ref}, and the integrating capacitor C_{int} should be large to minimize kTC noise, but the size is limited mainly by the ability of the source-follower to drive them at the oversampling rate and the available area under each column of pixels. Therefore, all the capacitors are designed to be poly1-poly2 capacitors of 1 pF .

The control signals ϕ_1 and ϕ_2 are two non-overlapping clocks that read the two signal levels of the pixel output. Clock ϕ_V is synchronous with ϕ_2, and is generated from the output of the comparator so that it is on only when the comparator output is "1". During each cycle, the amplitude of the modulated signal (ΔV_{sig}) is integrated across C_{int}. In addition, when the comparator output is "1", the maximum signal swing (ΔV_{max}) is subtracted from the integrator output. A reset switch is included across the feedback capacitor to reset the integrator at the beginning of each pixel conversion. If it is assumed that the op amp and the switches are ideal, the difference equation describing this operation for the n-th cycle can be written as

$$Vout_n = Vout_{n-1} + \frac{C_{sig}}{C_{int}} \Delta Vsig_n - \frac{C_{ref}}{C_{int}} Vq_{n-1} \tag{3.2}$$

where V_q is 0 when q is "0" and V_q is ΔV_{max} when q is "1".

The op amp is implemented with self-cascoding transistors (SCFETs) [7] as shown in Figure 7 in order to increase the gain of the input differential stage. The second stage consists of a source-follower to ensure single-pole frequency response without the addition of a compensation capacitor.

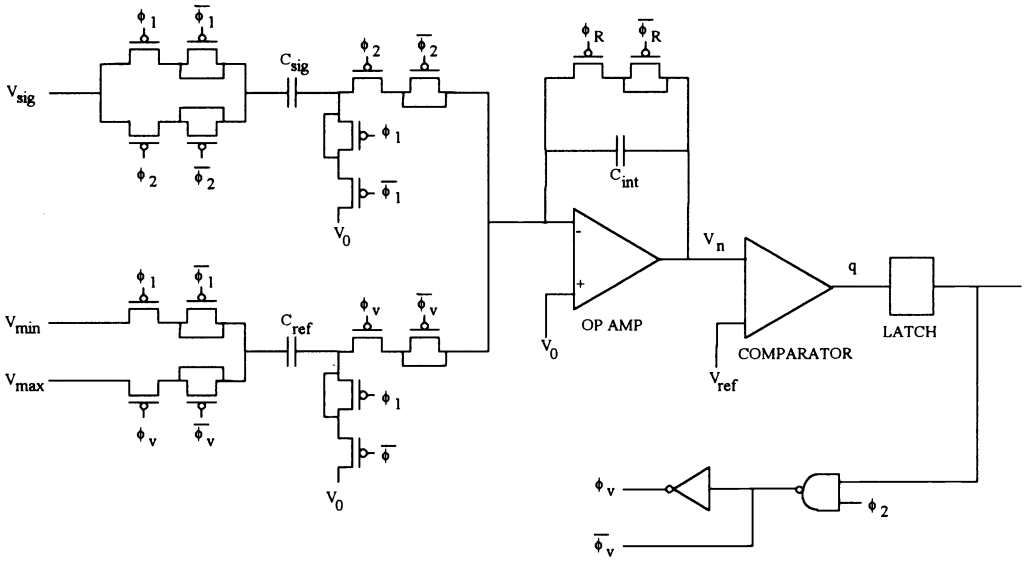

Figure 6: Switched-capacitor implementation of sigma-delta modulator.

The quantizer is a strobed comparator (Figure 8) whose inputs are the integrator output and the reference level corresponding to the full scale of the input. When the inputs are ready for comparison, the strobe signal is turned on, and the output is latched after it is allowed to settle. When the comparison is completed, the strobe signal is turned off to make the comparator idle and thus reduce power consumption.

The latched output of the comparator is used to generate the clock signal ϕ_V and its complement for the next integration cycle as shown in Figures 6 and 9. It is also used to generate the two non-overlapping clocks required as inputs to the counter.

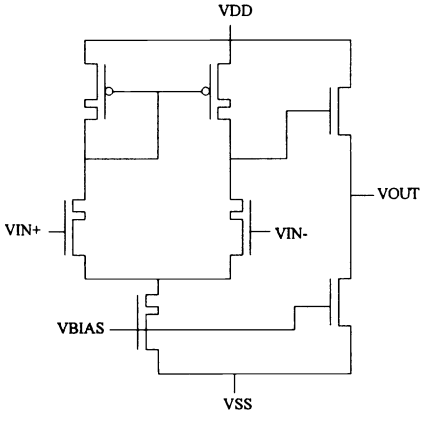

Figure 7: Op amp circuit

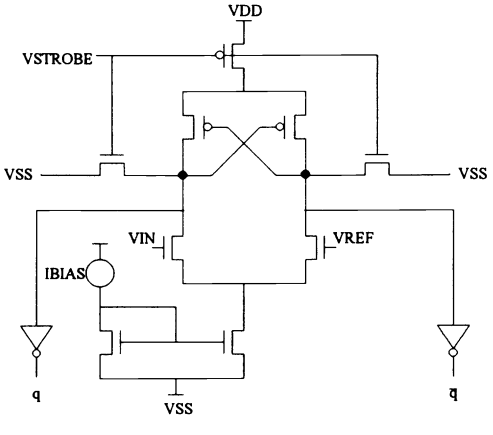

Figure 8: Strobed comparator circuit

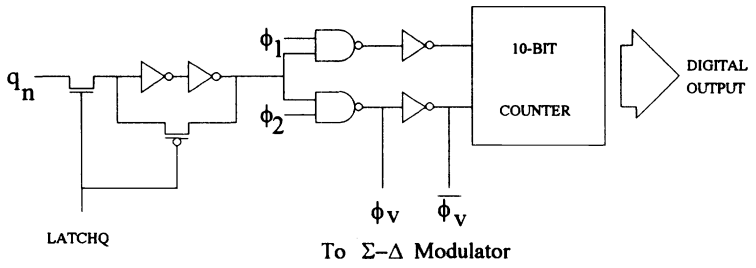

Figure 9: Logic circuit for feedback control and counter inputs

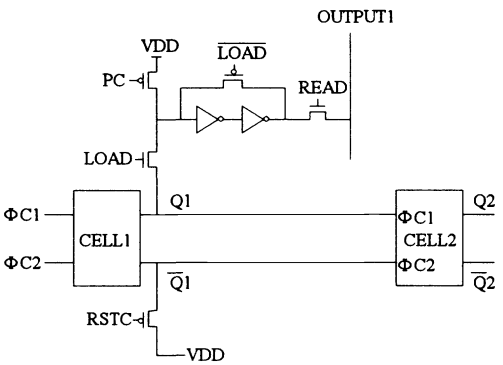

Figure 10 (a): Counter architecture

3.3.2 Counter Circuit

The 10-bit binary counter that averages the output of the sigma-delta modulator has 10 pipelined stages (Figure 10(a)) with a counter-cell (Figure 10(b)) and latch in each stage. The inputs to the first counter stage are the signals generated from the comparator output. The inputs to the other stages are the outputs from the previous stage. Each counter cell is reset to zero at the beginning of a pixel conversion. The sigma-delta modulator output is averaged by counting the number of "1"s occurring in 1024 sigma-delta outputs for each pixel. These values are latched at the end of each conversion period and read out during the next conversion period. Since the linear array of sigma-delta modulators and counters operate in parallel to convert one row of pixels at a time, the latched counter outputs are read out column by column during the next conversion period.

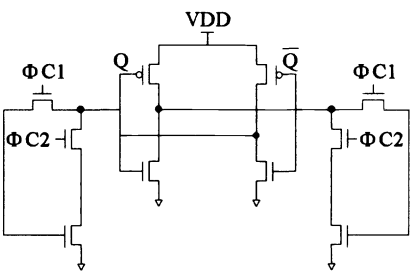

Figure 10(b): Counter cell

4. PROJECTED PERFORMANCE

4.1 Simulated operation

The basic operation of the sigma-delta modulator with constant input was simulated with the recursive relations given in equation (2.1). The switched-capacitor circuit, op amp, comparator, counter and the complete A/D converter circuit were simulated using the PSPICE circuit simulator. The power consumption for one A/D converter is 415 μW at a speed of 10^3 conversion/s which is limited by the op amp performance. The total power consumption for a 128x128 APS array with a sigma-delta A/D converter for each column, and row and column control circuits is approximately 53 mW.

4.2 Noise sources

The main noise sources in the sigma-delta modulator circuit are 1/f noise and white noise of the input transistors at each stage and the kTC noise of the switched-capacitors. For each stage, the input-mean-square voltage-noise spectral density of 1/f noise is given by

$$S_{n_f} = \frac{K_f}{K' C_{ox} WL} \frac{1}{f} \tag{4.1}$$

where K_f is a process dependent parameter, C_{ox} is the oxide capacitance, K' is the transconductance parameter, and, W and L are respectively the width and length of the transistor [8]. Similarly, the spectral density of white noise is given by

$$S_{n_w} = \frac{8}{3} \frac{kT}{g_m} \tag{4.2}$$

where g_m is the transistor transconductance. The kTC noise in each branch of the switched-capacitors and the sampling capacitors of the floating-diffusion pixel can be expressed in input referred noise electrons as

$$\langle n_{sc} \rangle = \frac{1}{S}\sqrt{\frac{kT}{C}} \tag{4.3}$$

where S is the sensitivity of the APS unit cell given in equation (3.1), C is the capacitance, k is Boltzmann's constant, and T is temperature. Table 1 summarizes these contributions in input referred rms noise electrons. The largest noise component is op amp white noise due to the large bandwidth needed for the high oversampling ratio. However, oversampling reduces the white noise and kTC noise components by the square root of the number of samples taken.

Table 1: Summary of noise sources

Noise Source	Input Referred rms Noise Electrons	
	Floating-gate pixel	Floating-diffusion pixel
Source-follower 1/f noise	2.6 e^-	2.6 e^-
Source-follower white noise	3.5 e^-	3.5 e^-
Switched capacitor kTC noise	2.1 e^-	2.1 e^-
Sampling capacitor kTC noise		0.7 e^-
Op amp 1/f noise	2.4 e^-	2.4 e^-
Op amp white noise	5.3 e^-	5.3 e^-
Comparator noise	Negligible	Negligible
Total	7.57 e^-	7.6 e^-

4.3 Effects of op amp non-idealities

The transfer function of the integrator in the sigma-delta modulator with ideal components can be expressed as

$$H(z) = \frac{C_1}{C_2}\frac{z^{-1/2}}{1-z^{-1}} \tag{4.4}$$

Table 2: Effects of op amp non-idealities

NON-IDEALITY	TRANSFER FUNCTION	EFFECT
Ideal transfer function	$H(z) = \frac{C_1}{C_2}\frac{z^{-1/2}}{1-z^{-1}}$	Ideal behavior
Finite op amp gain	$H(z) = \frac{C_1}{C_2}\frac{\frac{1}{(1-1/A-AC_1/C_2)}z^{-1/2}}{\left[1-(1-C_1/C_2-1/A)z^{-1}\right]}$	Non-linearity
Limited op amp bandwidth	$H(z) = \frac{C_1}{C_2}\frac{z^{-1/2}\left[(1-\varepsilon)+z^{-1}\varepsilon\left(\frac{1}{C_1/C_2+1}\right)\right]}{1-z^{-1}}$ where $\varepsilon = e^{-BT_s}$	Limits oversampling rate
Non-zero switch resistance	$H(z) = \frac{C1}{C2}\frac{z^{\frac{-1}{2}}\left[1-2e^{-T_s/4R_{on}C1}\right]}{1-z^{-1}}$	Negligible effect

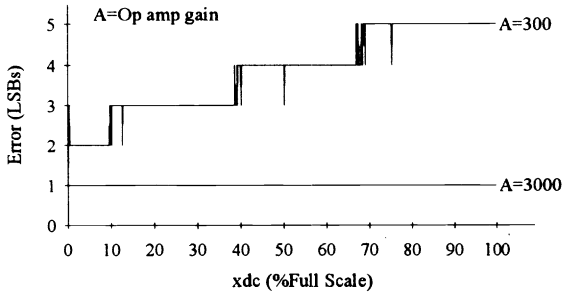

Figure 11: Effect of finite op amp gain vs. d.c. input

where C_1 and C_2 are the capacitors in the forward and feedback paths respectively. However, non-idealities of circuit components modify this expression and the actual transfer function includes a combination of these effects. The effects of finite op amp gain, limited op amp bandwidth and non-zero switch resistance are summarized in table 2.

The most important of these effects is finite op amp gain since it affects the poles of the transfer function. This introduces a non-linearity due to damped integration as a result of the attenuation in the feed-back path. This effect was simulated for op amp gains of 300 and 3000, using the modified recursive relation

$$u_n = \alpha u_{n-1} - \beta(x_n - q_{n-1}) \tag{4.5}$$

where α depends on the op amp gain and takes on a value less than 1. The simulation was carried out for constant inputs from 0 to full scale in integer multiples of the least significant bit (which is 1/1024th of full scale). The simulation involved integration over 1024 cycles and the output was defined as the number of "1"s in that output stream. The error plotted in Figure 11 is expressed as the difference between the output with damped integration and the output of the ideal integrator that has no damping. By choosing an op amp gain at least as high as the oversampling ratio, the effect of finite gain can be limited to less than 3 dB [1].

The effects of limited op amp bandwidth and non-zero switch resistance are not as crucial as the effect of op amp gain since they change only the zeros of the transfer function and not the poles which affect stability of the sigma-delta modulator.

5. CMOS APS TEST CHIP

5.1 Architecture

The APS test chip shown in Figure 12 was fabricated on a 2.22x2.25 mm^2 MOSIS tiny chip. The test chip consists of a 28x28 array of active pixels, row and column decoders and clock generator circuits, and an array of output circuits. The pixel unit cell (within the dotted outline) and output circuit are shown in Figure 13. The pixel unit cell is the floating-diffusion pixel described in section 3.2, but measures 40x40 μm^2 rather than 50x50 μm^2. The output circuit is common to a column of pixels and has two branches to sample the reset level and the signal level. Each output branch has a sampling switch and a 1 pF sampling capacitor followed by a second source follower stage. The load transistors of the second source followers are common to all the columns. The row and column decoders generate the row and column addresses based on 5-bit input addresses to the chip. The clock generator circuits use the decoded row address to generate the photo-gate (PG) and reset (RST) signals for each row whose high and low levels can be set independently of the rail voltages.

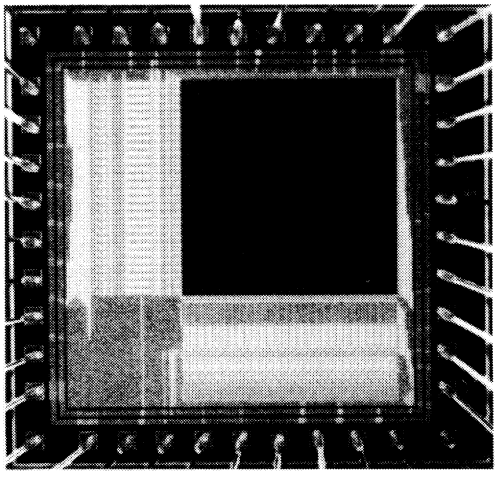

Figure 12: Photograph of CMOS APS test chip.

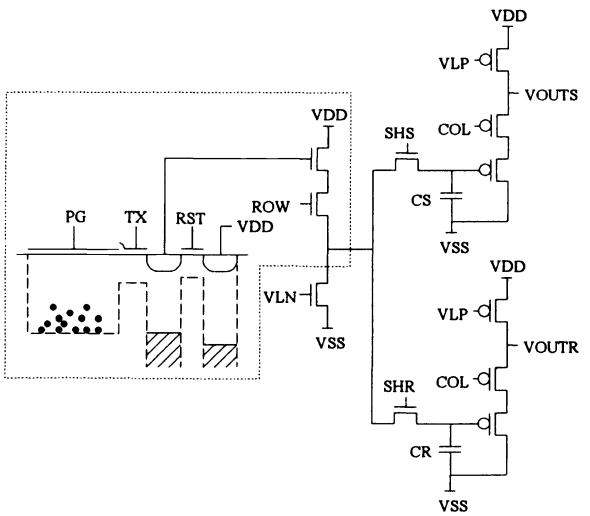

Figure 13: Pixel unit cell and output circuit.

Figure 14: Image from CMOS APS test chip.

5.2 Operation

The basic operation of the pixel sensor is described in section 3.2. The chip is TTL compatible with rail voltages of +5V and 0V. An additional 2.5V source is needed for the d.c. level of the transfer-gate (TX) and the source follower loads VLN and VLP, which can easily be generated on-chip in future designs. All other clock levels are 5V and 0V.

Signal-charge is integrated under the photo-gate which is biased at 5V with the transfer gate d.c. biased at 2.5V. When a row of pixels is ready to be read-out, the appropriate row transistor (ROW) of each pixel is turned on. The output node is reset by briefly pulsing the reset gate (RST) and the reset level is sampled onto one of the sampling capacitors, CR. The photo-gate (PG) is then pulsed low to 0V and the signal charge is transferred to the output node. The signal level is sampled onto the other sampling capacitor, CS. The stored reset and signal levels for each row of pixels are read out before the next row of pixels is sampled. The column select transistor (COL) is used to scan the stored signals.

5.3 Experimental Results

The APS sensor was operated as described above and the raw image output from the chip was displayed on a screen. A photograph of such an image is shown in Figure 14. Using discrete active-pixels on another chip, the output sensitivity was measured to be 4 $\mu V/e^-$ for the floating-diffusion pixel and 2.4 $\mu V/e^-$ for the floating-gate pixel. The maximum signal was approximately 600 mV corresponding to 150,000 electrons. No lag or blooming was observed. The fixed pattern noise was approximately 1.5%. Dark current was measured to be 1-10 nA/cm^2 at room temperature. In general, the imager performance was better than expected.

6. CONCLUSIONS

The design of a focal-plane A/D converter based on first order sigma-delta modulation has been presented. The predicted performance of the system in terms of speed of operation and noise is currently limited by the op amp. The APS test chip yielded promising results. Other chips currently being fabricated are a 128x128 APS array, a 28x28 APS array with floating-gate output, and a 28x28 APS array with higher fill factor. Current research also includes testing discrete sigma-delta modulator circuits which have been fabricated through the MOSIS foundry service. Future work will include improvements of the current design and integration into a full sensor.

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* MOSIS is the MOS Implementation Service provided by DARPA and managed by USC's Information Sciences Institute. The service provides quick turnaround, low cost foundry access to CMOS processing.