

## **An Active Pixel Sensor Fabricated Using CMOS/CCD Process Technology**

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### **Abstract**

This paper describes the integration of the active pixel sensor (APS) architecture normally fabricated in conventional complementary metal oxide semiconductor (CMOS) technology with a pinned photodiode (PPD) device using a mixed process technology. This new technology allows mix and match of CMOS and high performance charged coupled device (CCD) modules. The PPD [1] becomes the photoactive element in an XY-addressable area array with each pixel containing active devices for the transfer, readout and reset functions. It is a standard photo-sensitive element, available in a high performance true two-phase CCD technology developed previously for CCD-based image sensors [2]. An n-well 2- $\mu\text{m}$  CMOS technology was combined with the CCD process to provide the best features from both. A Design of Experiment approach was used with Technology Computer Aided Design (TCAD) tools to develop and optimize the new mixed process technology without sacrificing any CCD performance while minimizing impact to the CMOS device characteristics [3]. By replacing polysilicon photocapacitor or photogate in conventional APS with the pinned photodiode, deficiencies in poor blue response and high dark current are minimized [4].

A  $256 \times 256$  pixel PPDAPS is designed with a pixel pitch of  $40\mu\text{m}$ . The imager is 1.2 cm square realizing a fill-factor of 30%. It is designed to operate on standard 5V TTL voltage. Architecture and details of the imager is presented along with modeling results of its performance. Issues in the CCD/CMOS process integration are also discussed. Characteristics of the CMOS/CCD technology are obtained from measurements on conventional CCD linear image sensors and CMOS test circuits. Performance of the PPDAPS is measured using test structures containing the actual pixel layout from the  $256 \times 256$  imager. This work demonstrates the promise of incorporating image-sensor CCD technology in CMOS APS.

### **References**

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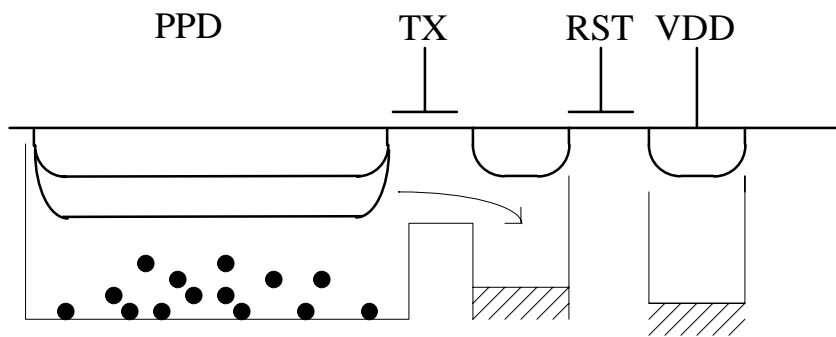


Figure 1. Schematic cross-section of the Pinned Photo Diode Active Pixel Sensor. Charges integrated in the PPD is moved into the floating sensing diffusion for readout by the transfer gate TX. Afterwards the signal is reset via the reset gate RST to power supply voltage VDD.

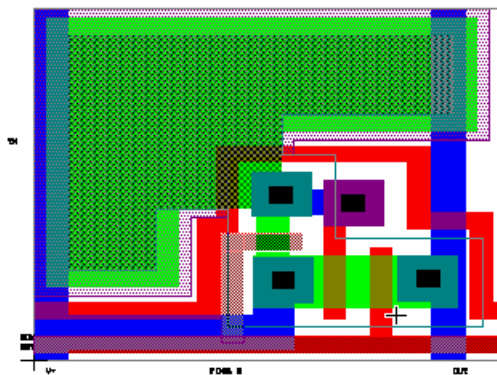


Figure 2. Details of a pixel. The pixel size is 40 $\mu$ m square and contains the pinned photodiode and 3 transistors.

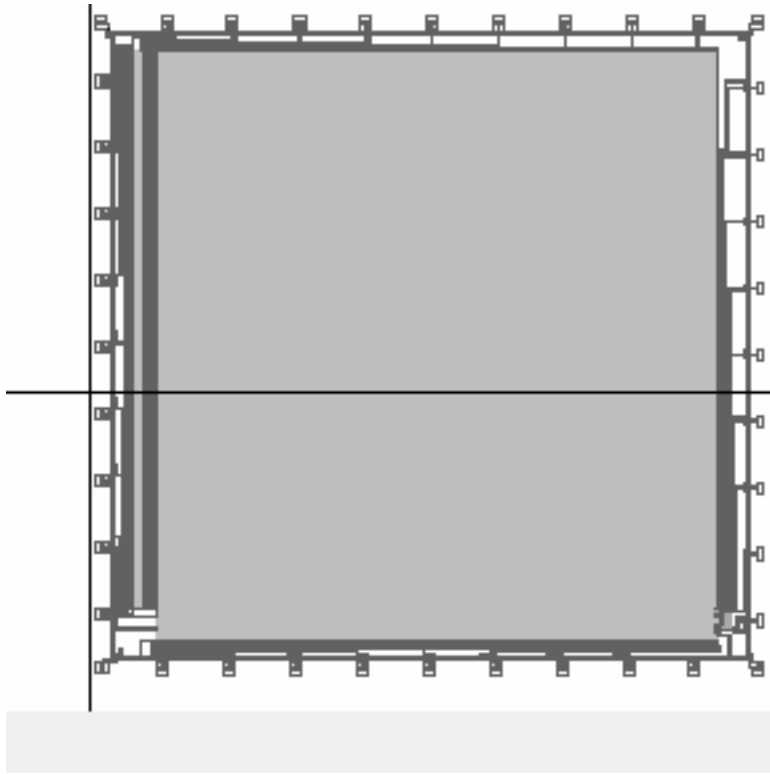


Figure 3. Layout of the  $256 \times 256$  pinned photodiode APS. The imager measures 1.2 cm a side with a 40 pin pad frame.