Image Sensor with Image Smoothing Capability
Using a Neuron MOSFET

Jun-ichi Nakamura
Olympus America Inc, Torrance, CA 90505
Eric R. Fossum
Jet Propulsion Laboratory, Pasadena, CA 91109

ABSTRACT

A novel image sensor with image smoothing capability is described. The image smoothing is performed in real time by a neuron MOSFET implemented on-chip. The neuron MOSFET has multiple input gates and a floating gate. The floating gate is capacitively coupled to the input gates, thereby performing gate-level weighted sum operations.

A pixel output node of the image sensor is connected to the input gates of several neuron MOSFETs which are implemented on the periphery of the imaging area. The pixel output is weighted by the input gate's capacitance value and summed up on the floating gate. Thus the filter characteristic is determined by the input gates' capacitance values and the number of pixels connected to the input gates of a neuron MOSFET. An active pixel sensor (APS) approach is suitable for the architecture because of its large driving capability.

SPICE simulation results and experimental results of a linear array and a test structure are reported. The linear array outputs smoothed image and raw pixel signal. An edge detected signal can be obtained by subtracting the smoothed signal from the pixel signal. An area array configuration is also introduced.

1. INTRODUCTION

The integration of image acquisition and image/signal processing functions on the focal-plane of an imaging system is referred to as focal-plane processing[1]. It is expected that focal-plane processing leads to increased sensor imaging performance, reduced sensor system size and weight and increased sensor system throughput. In addition, electronics integration has historically led to improved circuit reliability and decreased cost.

Most image processing involves a local neighborhood of pixels. For example, edge detection requires comparison of the pixel value to that of its nearest neighbors. Many local neighborhood operations can be cast as a local convolution or weighting of the nearest neighbors over some window region, typically 3×3 or 5×5 in size. Hence, the values of the neighbors must be available simultaneously in order to perform the operation. Unfortunately, in conventional readout architectures the serial output data stream retains horizontal neighbors in close proximity but vertical neighbors are separated in time by a one row delay. Circuitry to reconstruct the local neighborhood after readout must be utilized prior to image processing[1].

The active pixel sensor(APS)[2] approach can avoid the need to implement the reconstruction circuitry by using its non-destructive readout (NDRO) capability[3]. Takayanagi et al demonstrated a Charge Modulation Device(CMD) image sensor (which is one of the APS's) for real-time image processing[4]. It has 9 output ports which output 3×3 local neighboring pixel values in parallel. The 3×3 neighbors are read out simultaneously using the NDRO capability. This architecture is flexible because the kind of image processing is determined by an off-chip circuitry.

A new architecture of image sensors for image smoothing is proposed. In contrast to the CMD image sensor, this architecture allows for on-chip image processing which would be preferable for fixed image processing. It utilizes a

neuron MOSFET[5] which performs a weighted sum operation and uses the NDRO capability of the APS. The APS approach is suitable for the use of neuron MOSFETs because of its charge amplification capability.

In this paper, an image sensor with image smoothing capability using a neuron MOSFET is reported. After brief review of the neuron MOSFET in Section 2, image smoothing architecture is described in Section 3. In order to confirm the concept, SPICE simulation was performed and a linear array and test structures were designed, built and characterized. These results are described in Section 4. Finally, an area array configuration is introduced.

2. BRIEF REVIEW OF A NEURON MOSFET

The neuron MOSFET (abbreviated as ν-MOS) was first proposed by Shibata and Ohmi in 1991[5]. The basic structure of the neuron MOSFET is illustrated in Fig. 1[5, 6]. It consists of a conventional MOSFET and a gate electrode which is electrically floating and N input gates capacitively coupled to the floating gate. It is assumed that no charge injection occurs during device operation.

The net charge in the floating gate Q_{FG} is given by

$$Q_{FG} = Q_0 + \sum_{i=1}^{N} (-Q_i)$$

$$= \sum_{i=0}^{N} C_i \cdot (\phi_{FG} - V_i) \tag{1}$$

where V_i ($i=1 \sim N$) are the input signal voltages, C_i ($i=1 \sim N$) are the capacitive coupling coefficients between the floating gate and each input gate, V_0 the substrate potential, C_0 the capacitive coupling coefficient between the floating gate and the substrate, and Q_i ($i=0 \sim N$) is the charge in each of the capacitors. Assuming the substrate is grounded, the floating gate potential ϕ_{FG} is represented as

$$\phi_{FG} = \frac{Q_{FG} + \sum_{i=1}^{N} C_i \cdot V_i}{\sum_{i=0}^{N} C_i}$$
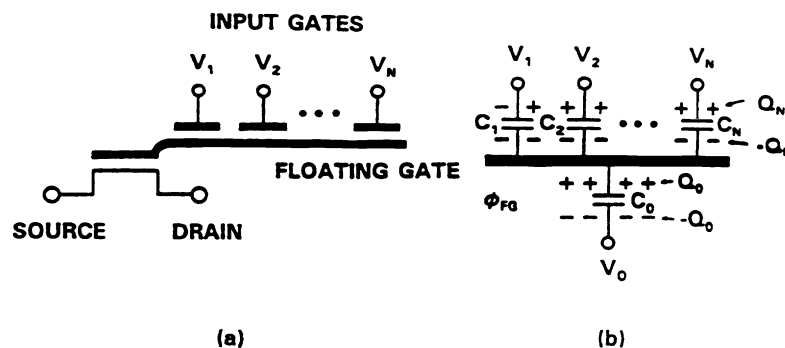

Fig. 1   (a) A schematic of a neuron MOSFET,   (b) relationship between terminal voltages and capacitance values.

$$= \phi_{FGO} + \frac{\sum_{i=1}^{N} C_i \cdot V_i}{\sum_{i=0}^{N} C_i} \tag{2}$$

where ϕ_{FGO} denotes the initial floating gate potential.

Eq. (2) states that the floating gate potential is determined as a linear sum of all input signals weighted by the capacitive coupling coefficients. This weighted sum operation does not dissipate any power except during the charging and discharging of the input gate capacitors. C_0 and C_i ($i = 1-N$) are given by

$$C_0 = \frac{\epsilon L W}{t_{ox}} \tag{3}$$

$$C_i = \frac{\epsilon A_i}{t'_{ox}} \tag{4}$$

where L denotes the gate length, W the gate width, t_{ox} the gate oxide thickness of the MOSFET and A_i the input gate area, t_{ox}' the SiO_2 thickness between the input gates and the floating gate, respectively. In order to couple the input voltages effectively to the floating gate, the input gate's capacitance value is designed to be;

$$\gamma = \frac{\sum_{i=1}^{N} C_i}{\sum_{i=0}^{N} C_i} = \frac{C_{TOT} - C_0}{C_{TOT}} = 1 \tag{5}$$

The MOSFET turns on when ϕ_{FG} exceeds its threshold voltage V_{TH}.

3. IMAGE SMOOTHING ARCHITECTURE

The conceptual diagram of a smoothed output image sensor is shown in Fig. 2. For simplicity, a linear array comprised N pixels ($n = 1-N$) is assumed. Pixels are reset at the reset voltage V_R through reset transistors(not shown). After the reset, the pixel voltage changes due to the charge accumulation induced by the incident photon flux. Each neuron MOSFET has multiple input gates(in this case, 5 gates; one from a particular pixel and four from the adjacent pixels) to which pixels' voltages are input. Each input gate area is designed to obtain a desired filter characteristic. The floating gate voltage change of the n-th neuron MOSFET is given by

$$\Delta \phi_{FG}(n) = \sum_{k=-2}^{k=+2} h(k) \cdot \Delta V(n+k) \tag{6}$$

where h(k) is a response function of the filter and $\Delta V(n+k)$ is the $(n+k)$-th pixel voltage change, respectively. The input gate area A_i is designed so that desired filter characteristics are obtained and $\gamma = 1$, that is, $C_0 = C_{TOT}$, based on the values of t_{ox} and t_{ox}', L and W.

An active pixel sensor(APS)[2] is defined as a sensor with one or more active transistors located within each pixel. For a photodiode array, the pixel output is dependent on the capacitance at the output node. This is not the case for an APS array due to the active transistors inside each pixel. These transistors provide current driving capability, which results in the output signal being essentially independent of the capacitance at the output. This is a desirable feature

for this architecture since each pixel has to drive the input gates of several neuron MOSFETs.

The output voltage which corresponds to the floating gate voltage of the neuron MOSFET is obtained by scanning the switching MOSFETs M_S sequentially, as shown in Fig. 2.
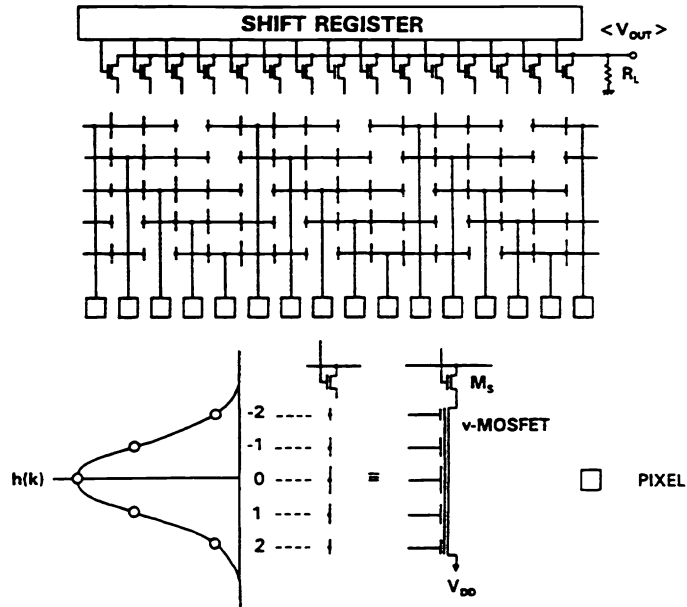

Fig. 2   The conceptual diagram of a smoothed output image sensor. M_S and h(k) represent the switching MOS-FET and the response function of the filter.

4. LINEAR ARRAY

4.1. Circuit Configuration and Pulse Timing

In order to confirm the basic concept of the image smoothing, a linear array was designed, built and evaluated. Fig. 3 shows a circuit configuration of the linear array with image smoothing capability. The number of pixels is 65 and the pixel size is 18×18 μm^2 with 21 μm spacing. The sensor was built with the commercially available 2 μm double poly, double metal CMOS process.

Each pixel has a photodiode, which is buffered by a source follower. The linear array has two outputs. One output is the smoothed image output in which the pixel signal is convoluted by the response function h(k), and the other corresponds to individual pixel signal. These two outputs will be used for the edge detection of an input image. An additional input gate, which is common to each neuron MOSFET, is added to balance the two outputs.

The layout of the neuron MOSFET array is shown in Fig. 4. Each neuron MOSFET has 5 input gates as shown in Fig. 2. In order to reduce the parasitic capacitance formed by the floating gate and the substrate, the floating gate region between input gates is trimmed.

The pulse timing diagram required for the operation is shown in Fig. 5, along with waveformes obtained by SPICE simulation. During the reset period, both the photodiode and the floating gate are reset at V_{RS} and V_{RFG}, respectively. Pulse ϕ_T turns on and the gate of load transistor M_{LD} is biased at V_{LD} so that the M_{LD} acts as an active load, thereby charging the input gates at the reset levels ($t=t_1$). After the reset, the pulses ϕ_T and ϕ_{LD} are released, causing both
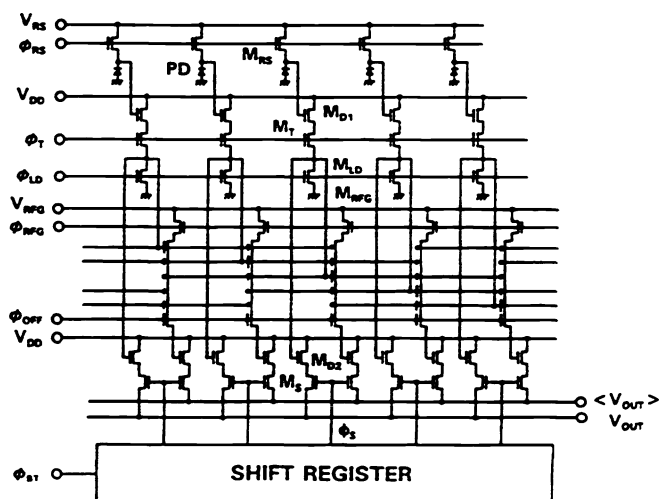
Fig. 3   Circuit configuration of the linear array with image smoothing capability.
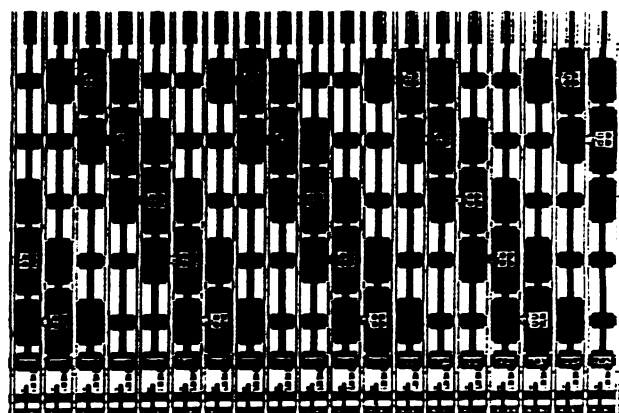

Fig. 4   Layout of the neuron MOSFET array. The filter characteristics extracted from this layout are shown in Fig. 7.

the input gate and the floating gate to be floating during the integration period. At $t=t_2$, when pulses ϕ_T and ϕ_{LD} are applied, the source follower is activated and the signal voltage appears on the input gate. The input gate voltages are weighted and summed on the floating gate as described in Section 3. After the pulses ϕ_T and ϕ_{LD} return to low, the shift register is driven by the shift register start pulse ϕ_{ST}. The smoothed output $< V_{OUT} >$ and the pixel output V_{OUT} appear in parallel, when the select pulse ϕ_S is applied at $t=t_3$.

The pulse timing mentioned above suppresses the fixed pattern noise (FPN) caused by the threshold voltage variation of the driver MOSFETs M_{D1}, since the voltage change of the floating gate at $t=t_2$ consists of only the signal voltage change, while the threshold voltage variations appear at the input gate both at $t=t_1$ and at $t=t_2$.
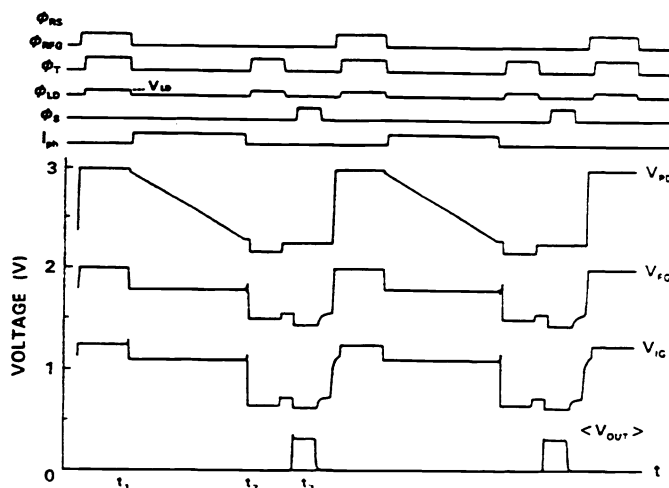

Fig. 5   Pulse timing diagram. Two cycles of operation are shown.

Edge detection is performed by subtracting $<V_{OUT}>$ from $V_{OUT}{}^7$, as shown in Fig. 6.
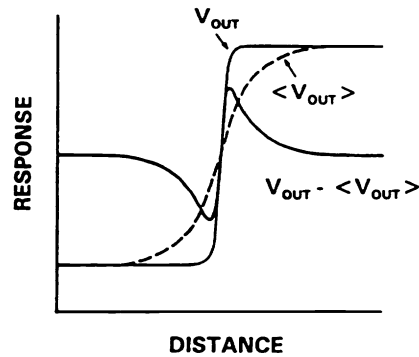

Fig. 6   Model illustrating the mechanism of the generation of pixel response to spatial edge in intensity (from [7]).

4.2. Experimental Results

Fig. 7 shows the extracted filter characteristics obtained by scanning a He-Ne laser beam ($\lambda = 633$nm) along 5 pixels which are connected to one neuron MOSFET. The designed characteristics, which are calculated from the layout shown in Fig. 4, are also plotted in the figure. The characteristics are in good agreement.

The effect of the pulse ϕ_{OFFSET}, obtained with a test structure, is shown in Fig. 8. The test structure consists of a unit pixel and its associated readout circuit. In this case, the MOSFET M_T always turned on and the photodiode in the pixel was illuminated with constant light intensity. The output waveform represents the floating gate voltage change. It is seen that the output is controlled by the pulse. This additional control signal might be used to suppress the fixed pattern noise originated from the threshold voltage variation of the neuron MOSFETs.
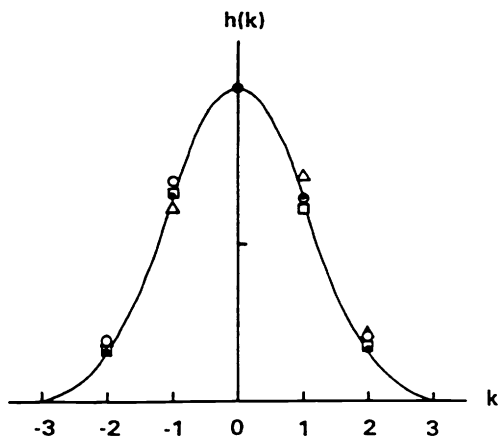

Fig. 7   Extracted filter characteristics obtained by scanning a He-Ne laser beam ($\lambda = 633$nm). The designed characteristics ($\bullet$) are also shown.
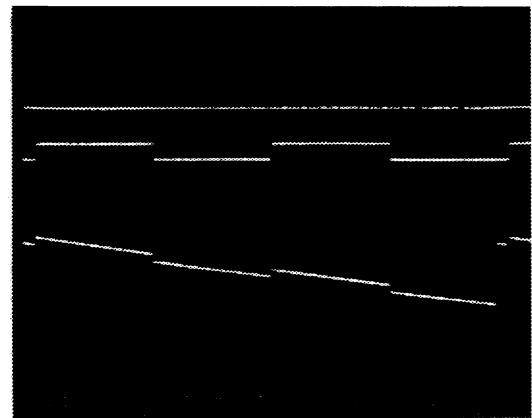
Fig. 8   Effect of the pulse ϕ_{OFFSET}. The upper, the middle and the bottom traces are the reset pulse ϕ_{RS}, the pulse ϕ_{OFFSET} and the smoothed output waveform, respectively.

5. AREA ARRAY CONFIGURATION

Based on the results described above, an area array configuration is proposed. Figure 9 shows an area image sensor which provides an edge detection function for an image. The sensor consists of a pixel array, a switch array, a neuron MOSFET array, a vertical scanning circuit and a horizontal scanning circuit with horizontal selection switches.

The pixel array consists of $M(V) \times N(H)$ pixels. Each pixel is connected to the vertical select line which carries vertical select pulse ϕ_{Vj} ($j = 1 \sim M$), and to the vertical signal line. In order to perform 3×3 local mask operation at each neuron MOSFET, the pixels on a column, T_{ij} ($i = 1 \sim N$), are accessed three times by the vertical scanner, as in the same manner in the literature[4]. Therefore, the pixel must have nondestructive readout capability.

The circuit configuration of the neuron MOSFET array and the horizontal select switch array is shown in Figure 10. The vertical signal lines from the pixel array are connected to the switch array where they are fed to proper input gates of the neuron MOSFET. This operation is controlled by pulses ϕ_-, ϕ_0 and ϕ_+, which are applied in order during the horizontal blanking period. The 3×3 pixel data are weighted and summed on the floating gate of each neuron MOSFET. The horizontal selection switches turn on in order in accordance with the application of the horizontal select pulses ϕ_{Si} from the horizontal scanning circuit. The pixel output V_{OUT} and the smoothed output $< V_{OUT} >$ are obtained at load resistors. These two output signals are used to reproduce an edge detected image, in the same manner as shown in Fig. 6.
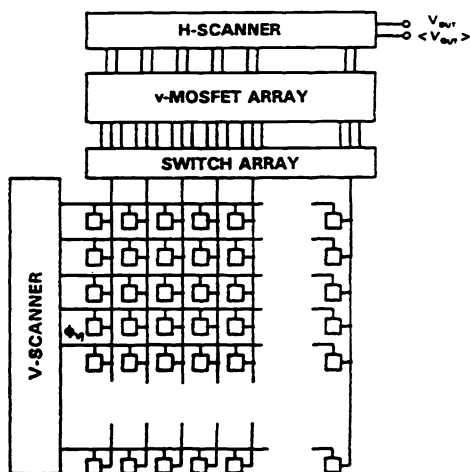

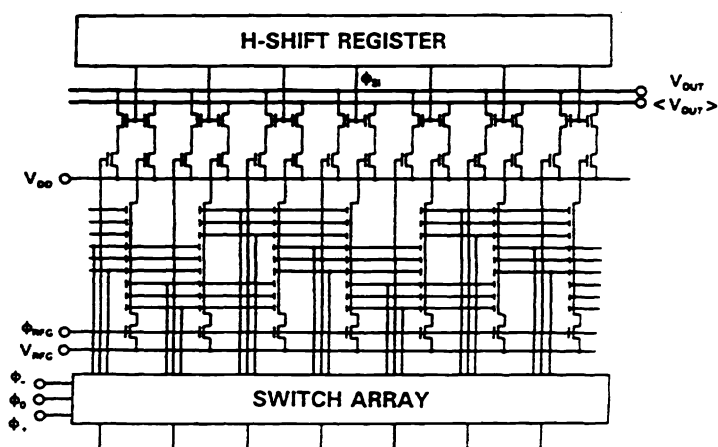Fig. 9   Proposed area array configuration.

Fig. 10   Circuit configuration of the neuron MOSFET array and the horizontal select switch array in the proposed area sensor.

6. CONCLUSION

A novel image smoothing architecture using a neuron MOSFET has been demonstrated. An active pixel sensor (APS) approach has been used for the architecture due to its nondestructive readout (NDRO) and charge amplification capabilities. This approach to image smoothing has been confirmed by SPICE simulation, as well as experimentally. A linear array and test structures were designed, built and tested. Further characterization is being performed as well as the design of an area array.

This architecture is suitable for high density image sensors, since the image processing block is located on the periphery of the imaging area. Since the image sensor outputs the smoothed image signal in real time, neither an A/D converter nor memory devices are needed prior to processing. The edge detected signal which is produced by subtracting the smoothed image signal from the pixel signal would be fed to a processing block which performs more complicated task, such as image recognition, without requiring a computationally intensive preprocessing block. Thus, the proposed image sensors will produce high performance, compact and light weight smart imaging systems.

ACKNOWLEDGEMENT

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