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GaAs CCD Readout for Engineered Bandgap Detectors

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ABSTRACT

GaAs and related heterostructure charge-coupled devices (CCDs) for detector array readout multiplexer applications are described. Features of resistive-gate CCDs are compared with capacitive-gate CCDs for this application. Design examples of GaAs CCD readouts for linear and 2-dimensional detector arrays with different detection methods and signal coupling schemes are described. Recent progress in 2-dimensional electron gas (2DEG) $Al_{0.3}Ga_{0.7}As$/GaAs resistive-gate CCDs is also presented. The 2DEG resistive-gate CCD has a higher transfer speed, a larger charge handling capability, and a reduced clock swing over the conventional buried-channel GaAs CCD.

1. INTRODUCTION

Silicon CCDs have proven their excellence in imaging applications. While silicon CCDs have demonstrated best responsivity in the visible wavelengths, applications for the near UV and X-ray spectrum[1] as well as the infrared spectrum[2,3] have been also found. However, the efficiency of Si-based detectors for wavelengths other than the visible and SWIR is relatively poor, demanding a significant effort in materials technology to improve the responsivity and detectivity.

With the maturing of molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) technology, the responsive spectrum of detectors has been broadened by the bandgap engineering of various material systems[4]. Examples of these advanced detectors are GaAs/AlGaAs and InAlAs/InGaAs quantum well structures utilizing internal photoemission[5].

In spite of the bright future of these advanced detector structures, their scientific application is impeded by the lack of monolithic readout multiplexers for detector arrays. GaAs and related heterostructure CCDs are primary choices for the readout structure for engineered detectors with tailored responsivity since most of the detectors can be integrated on a GaAs substrate. Due to the lack of stable native oxides on GaAs, buried-channel structure CCDs based on Schottky barriers rather than insulated gates have been developed, resulting in inherent radiation hardness and anti-blooming features. There are two types of GaAs CCDs which can be classified according to their gate structure: capacitive-gate CCDs (CGCCD) and resistive-gate CCDs (RGCCD).

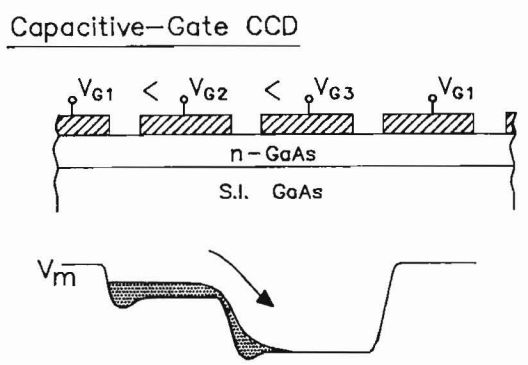

Fig. 1a Schematic illustration of the device structure and channel potential of a CGCCD.

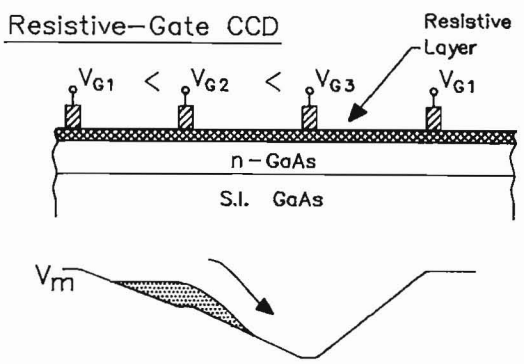

Fig. 1b Schematic illustration of the device structure and channel potential of a RGCCD.

In a CGCCD, shown in Fig. 1a, the phase electrodes are formed by metal gates separated by small inter-electrode gaps. Coupling of adjacent potential wells is achieved by the fringing field induced by the bias voltages applied to the metal gates. If the length of the gates is large, the fringing field effect is decreased, resulting in low transfer speed limited by carrier diffusion instead of drift. The presence of gaps between gate electrodes introduces potential troughs under the gap regions. Effects of the inter-electrode gap are a reduction of charge transfer efficiency (CTE) and dynamic range and an increased minimum clock swing for CCD operation.

The effect of the potential trough is minimized by reducing the gap size and employing a thick channel layer with a relatively low doping concentration. However, the former requires a submicron gap size that is hard to obtain by conventional photolithography and the latter reduces the integrability with high performance MESFET circuitry in which a highly doped thin channel layer is required. Overlapping gate structure CCDs[6] can produce submicron gaps by introducing a thin dielectric spacer between gate electrodes. Alternatively, recessing the gap regions[7,8] can reduce the potential trough depth, thus permitting a gap size bigger than 1 um.

In a RGCCD, shown in Fig. 1b, gap-related problems are completely eliminated since the gap region is covered by a resistive material (cermet) which controls the potential under the region. Narrow finger electrodes with wide spacing are formed to apply clock signals to the resistive layer. The elimination of gaps promises improved CTE and compatibility of the CCD channel with high performance FETs with a highly doped thin active layer. In addition to the elimination of the gap-related problems, RGCCDs enjoy the high charge transfer speed enhanced by the electric field applied by the resistive layer. Another advantage is that the cermet[9], usually used as the resistive layer, has lower leakage current than most metals on GaAs and related heterostructure materials, which translates into a larger dynamic range. RGCCDs have demonstrated operation at clock frequencies higher than 1 GHz with high CTE[10].

If side-injection gates from parallel multiplexers are coupled through a capacitive-gate structure into a RGCCD serial multiplexer, the CTE of the serial multiplexer seriously degrades[11]. A three-dimensional device simulation has been performed for this structure, showing a potential trough under the gap region along the serial multiplexer. The potential trough not only traps signal charge transferred from the side-injection gates to the serial multiplexer but also impedes charge transfer along the serial multiplexer, resulting in an overall performance degradation of the readout multiplexer. Extension of the resistive-gate structure for parallel-serial readout multiplexers is required to eliminate the gap-related problem. A computer simulation for a side-injection gate coupled through a resistive gate structure shows elimination of the potential trough problem. The schematic of the side-injection gate for the computer simulation is shown in Fig. 2a. The potential distribution in the resistive gate is shown in Fig. 2b with G2 and G3 at higher bias voltage than G1 and G4. Although a potential barrier instead of a potential trough is formed along the serial multiplexer, it can be stretched by the next phase clock voltages on the gate electrodes, as shown in Fig. 2c. The potential in the CCD channel closely follows that in the resistive gate.

2. DETECTION AND COUPLING

While bandgap engineered III-V detectors are still in their infancy, various types of detectors are emerging. The advanced detectors include heterostructures and multiple quantum wells utilizing internal photoemission, strained layers, and resonant tunneling. To investigate the feasibility of monolithic integration of GaAs and related heterostructure CCDs with advanced III-V detectors, a new mask set was designed. The mask set will be the workhorse for focal-plane array studies with advanced III-V detectors. For maximum versatility (since optimal detector structures are yet unresolved) a multiproject type mask set was designed. Multiplexers for different types of detectors, including photoconductors and photodiodes, with various detection and signal coupling schemes are included. By utilizing appropriate portions of the mask, different multiplexers with different detector structures can be selected for experimentation. The design also included both resistive-gate and capacitive-gate structures for performance comparison between them. Two basic detection methods were included: direct detection and indirect detection.

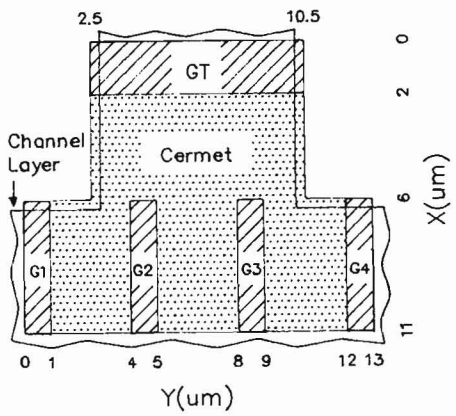

Fig. 2a Schematic of a portion of the side-injection gate utilizing a resistive-gate structure for the computer simulation.

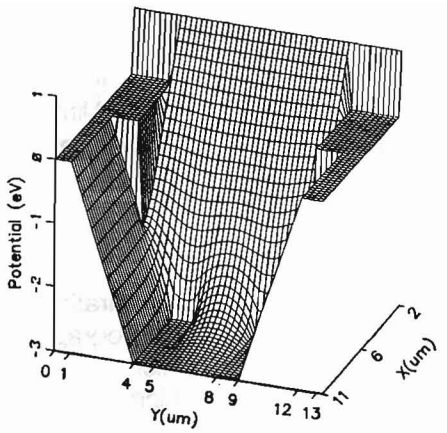

Fig. 2b Potential profile of the resistive layer with GT=-1 V, G1=G4=0 V, G2=G3=3 V.

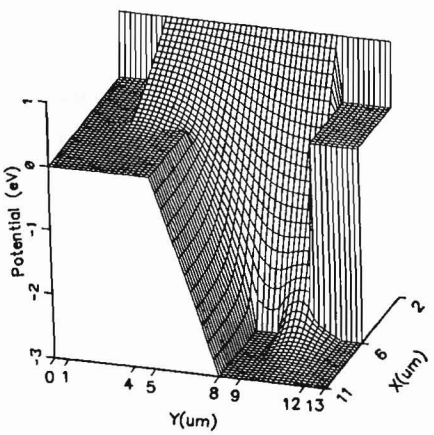

Fig. 2c Potential profile of the resistive layer with GT=-1 V, G1=G2=0 V, G3=G4=3 V.

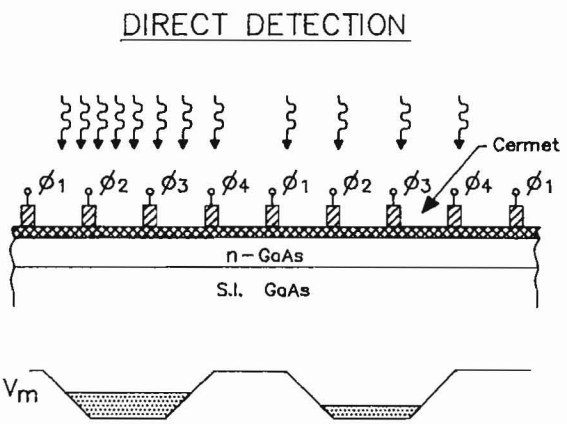

Fig. 3a Schematic cross section and channel potential of a RGCCD side-injection gate for a direction detection method.

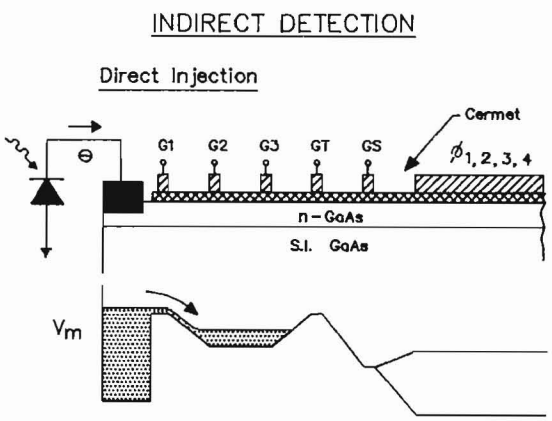

Fig. 3b Schematic cross section and channel potential of a RGCCD side-injection gate for a direct injection scheme (indirect detection).

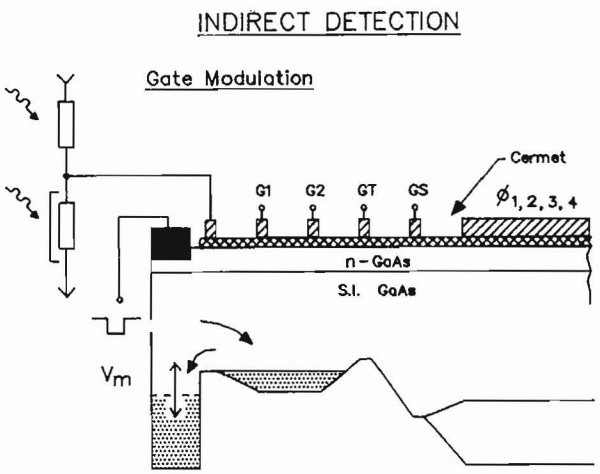

Fig. 3c Schematic cross section and channel potential of a RGCCD side-injection gate for a gate modulation scheme (indirect detection).

In the simplest direct detection method, signal charge is optically generated and stored in the CCD channel. For MWIR and LWIR III-V detectors, signal charge can be generated by a detector vertically integrated with the CCD channel, and then transferred to the CCD channel. The imager can be used with backside illumination through a large bandgap substrate, or with frontside illumination through the resistive layer. This type of detection method requires a large charge handling capability in the case of a LWIR imaging application because of the high background signal (unless the QE is low). A 2DEG CCD is naturally suited for this application since its charge handling capability is higher than the conventional GaAs CCDs. The schematic device structure and channel potential of a direct detection RGCCD multiplexer is shown in Fig. 3a.

In the indirect detection method, the optical signal is converted into an electrical signal through the detector. Candidate detectors include photodiodes and photoconductors that can be grown above the CCD channel and delineated by mesa etching. Within the confines of lattice matching, independent optimization of the detector and CCD channel structures is permitted in the indirect detection method. The electrical signal is coupled most easily into the CCD channel by two different coupling schemes: direct injection and gate modulation.

In the indirect injection scheme, photodiode type detectors are used to transduce the optical signal into an electrical signal. The electrical signal charge is directly fed through the input ohmic contact into the storage well of the CCD multiplexer side-injection gate. The requirement for the charge handling capability of the CCD channel is the same as that of the direct detection method. The schematic device structure and channel potential of a direct injection scheme RGCCD is shown in Fig. 3b.

In the gate modulation scheme, a serial connection of photoconductor or photodiode type detectors can be employed to generate the electrical signal. One of the detectors in series will be covered by a light shield implemented by the second metallization. The optical signal will be converted into a voltage signal at the electrical tap in the middle of these serial detectors. The electrical signal is fed to the first gate electrode of the side-injection gate and used to modulate the size of the storage well. A fill-and-spill input technique will be used to inject signal charges into the storage well that corresponds to the optical input signal. The schematic device structure and channel potential of the gate modulation scheme RGCCD is shown in Fig. 3c.

Linear arrays are designed with both capacitive-gate and resistive-gate structures for different detection methods and coupling schemes. The arrays are 32 stages long with a 28x28 um^2 pixel size and a four phase clock scheme. A double stage source follower with on-chip load FETs was employed to read out the signal from the CCD multiplexer. To reduce the feed through from the CCD clock signal and the reset signal, an output shield gate and a reset FET with an extra shield gate were used respectively. The capacitive-gate CCDs employed 1 um gap spacing and 6 um gate length and the resistive-gate CCDs employed 2 um electrode length with 4 um spacing. A 32x32 2-D array for the direct detection method with the resistive-gate structure is also designed. A double metallization process will be used to implement these devices. A test site for evaluating the fabrication process and device electrical characteristics is also included.

3. 2DEG AlGaAs/GaAs RGCCD

Two-dimensional electron gas (2DEG) heterostructure materials are attractive for high performance CCD applications since they provide various advantages over GaAs. The advantages include a larger charge handling capacity ($>1x10^{12}/cm^2$), translating into a larger dynamic range, a higher electron mobility at low electric field and temperature, an integrability with high performance 2DEGFET circuitry, a high sensitivity input signal injection capability, and a lower clock voltage swing requirement for the CCD operation.

RGCCD delay lines were fabricated on uniform- and planar-doped AlGaAs/GaAs heterostructure materials and tested to investigate their feasibility for the readout multiplexer of advanced detectors. Previous work elsewhere on this material employed the capacitive-gate structure, demonstrating relatively poor CTE (0.98)

at a maximum frequency of 83 KHz[12]. Low CTE is attributed to the inter-electrode potential trough which has a more serious effect on modulation-doped materials because the channel is very close to the gate (~300Å) and the high bandgap material is highly doped (~$2x10^{18}/cm^3$).

The schematic device structure and energy band diagram of a uniform-modulation-doped AlGaAs/GaAs RGCCD is shown in Fig. 4 and Fig. 5, respectively. The material structure is composed of a 300Å thick GaAs cap layer with $4x10^{18}/cm^3$ Si doping, a 350Å thick AlGaAs layer with $2x10^{18}/cm^3$ Si doping, and a 30Å undoped AlGaAs spacer layer on top of the undoped GaAs channel layer. The planar-modulation-doped material is composed of a 300Å thick GaAs cap layer, a 350Å thick undoped AlGaAs layer, an AlGaAs layer with $5x10^{12}/cm^2$ Si planar doping, and a 30Å undoped AlGaAs spacer layer on top of the undoped GaAs channel layer. Both materials were grown at Columbia University by an MBE system on <100> semi-insulating GaAs substrates.

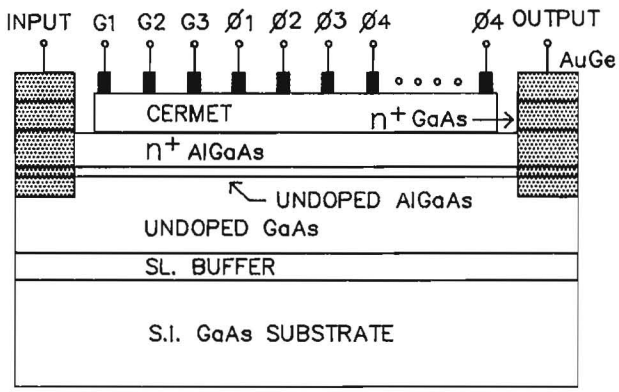

Fig. 4 Schematic cross section of a 2DEG RGCCD.

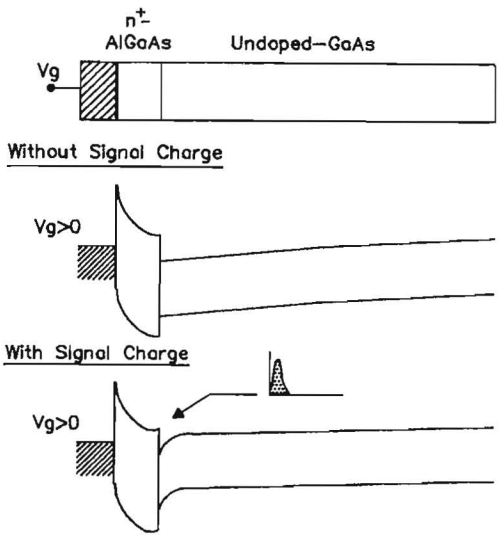

Fig. 5 Energy band diagram of a 2DEG CCD.

Both materials underwent the same processing steps. After a 4000Å deep mesa etching, AuGe ohmic contacts were formed and annealed at 425 C for 45 sec under a forming gas ambient. The GaAs cap layer and 50Å of the underlying AlGaAs layer was etched using the AuGe pattern as a mask. Cermet was e-beam evaporated on the CCD channel with an equal weight mixture of Cr and SiO powder sources, forming a Schottky contact to the underlying AlGaAs layer. The cermet was 2500Å thick with sheet resistance of 350 KΩ/□. The first Cr/Au metallization was done by e-beam and thermal evaporations, respectively, to form finger electrodes and gates for the output amplifiers. A 3500Å thick SiO layer was e-beam evaporated and lifted-off to form via holes. The second Cr/Au metallization was used to connect electrodes with the same phase.

Three types of RGCCD delay lines were fabricated: a 50 stage (200 electrodes) RGCCD with 2 um long electrodes spaced by 1 um, a 32 stage (128 electrodes) RGCCD with 1 um long electrodes spaced by 4 um, and a 13 stage (52 electrodes) RGCCD with 1 um long electrodes spaced by 10 um. All delay lines are 100 um wide and designed to operate with a 4 phase clocking scheme. A 1 um long and 100 um wide MODFET source follower with the same size on-chip load is used to read out the signal from the CCD channel. A dual-gate MODFET with a 1 um long and 25 um wide gate is used to reset the output of the CCD channel.

The operation of the delay lines was performed at both low and high frequencies. The high frequency test was performed for clock frequencies between 0.6 GHz and 1 GHz. The CTE measuredfor the 2 um gate spacing and 4 um gate spacing RGCCDs at 1 GHz clock frequency was 0.999 at room temperature. The CTE was slightly lower for the 10 um gate spacing RGCCD at this frequency. The result of 1 GHz operation of the 32 stage, 4 um gate spacing RGCCD on the uniform-doped AlGaAs/GaAs material is shown in Fig. 6.

The low frequency test was done at clock frequencies up to 13.3 MHz which is the maximum available with our low frequency test station. The measured CTE of the three types of RGCCDs on the uniform-doped material was 0.999 at 13 MHz clock signal at room temperature. The CTE degraded due to dark current as the clock frequency decreased; for example, 0.98 at 1.5 MHz for the 4 um spacing delay line. The CTE of the RGCCDs on the planar-doped AlGaAs/GaAs material was better than 0.999, and did not degrade for clock frequencies as low as 130 KHz as shown in Fig. 7.

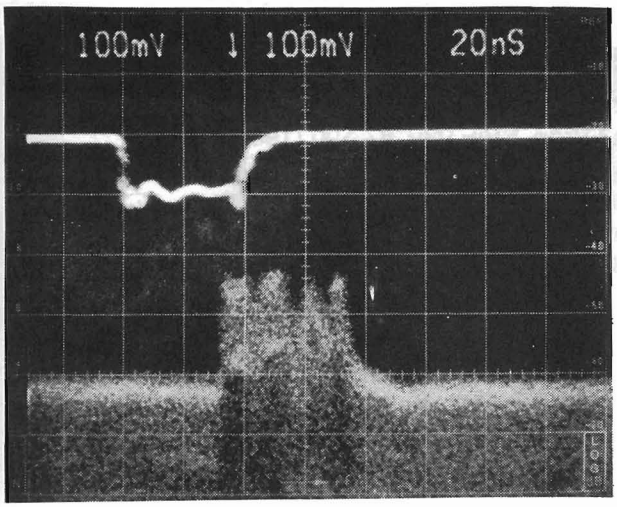

Fig. 6 Waveforms of electrical input and delayed output signals of a 32 stage uniform-doped 2DEG RGCCD at 1 GHz clock frequency.

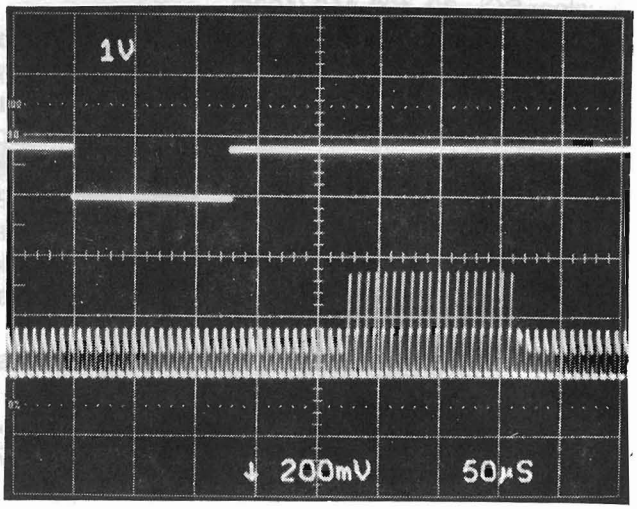

Fig. 7 Waveforms of electrical input and delayed output signals of a 32 stage planar-doped 2DEG RGCCD at 133 KHz clock frequency.

In order to characterize the performance at low frequency, the temperature of the CCD was lowered during the operation. Improvement of the CTE and the output signal amplitude was observed as the device was cooled down. Electrical measurement of the cermet Schottky diodes on both materials showed that the room temperature leakage current on the planar-doped AlGaAs was about two orders of magnitude lower than that of the diode made on the uniform-doped AlGaAs (20 uA/cm^2 and 2 mA/cm^2 respectively). These results suggest that the low frequency performance of 2DEG AlGaAs/GaAs RGCCDs is limited by the thermally-activated leakage current, though the carrier transport mechanism responsible for the excessive leakage current is not yet fully understood.

4. DISCUSSION AND CONCLUSIONS

Room temperature operation of high performance 2DEG AlGaAs/GaAs RGCCDs at 1 GHz has been demonstrated, showing promise of high speed signal processing and readout multiplexer applications. A new high frequency test station capable of driving CCDs with clock frequencies between 1 GHz and 4 GHz will be set up to evaluate the high speed limit of these devices. Research on a new material system (2DEG InAlAs/InGaAs heterostructure) in which higher transfer speed and larger dynamic range are expected is also under way. Further efforts to understand the transport mechanisms responsible for the gate leakage currents on the 2DEG material systems is suggested. Design examples of CCD readout multiplexers on GaAs and related heterostructure materials were presented. A multiproject e-beam mask set will be delivered soon, and monolithic integration of 2DEG CCDs with advanced engineered bandgap detectors will be attempted with the new mask set. Significant advancement in the understanding of 2DEG CCD focal-plane arrays for advanced III-V detectors is anticipated from this work.

5. ACKNOWLEDGMENTS

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