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Pushing the Envelope

On-chip integration yields high-performance devices.

By Eric Fossum, Photobit Corp.

It has been about eight years since the complementary-metal-oxide-semiconductor (CMOS) active-pixel-image sensor was proposed as a next-generation mainstream image sensor technology poised to penetrate the existing charge-coupled-device (CCD) detector market. Today, the bold predictions made in the early 1990s have come to pass. Compared with CCD detectors, CMOS active pixel sensors (APSs) offer the advantages of reduced power consumption, higher speed operation, increased levels of on-chip integration, lower system cost, and higher compatibility with modern integrated circuit fabrication processes. CMOS APS devices hold records for highest throughput and lowest power consumption. According to estimates from the past year, cameras shipped from Taiwan were more likely to incorporate CMOS image sensors than CCD detectors.

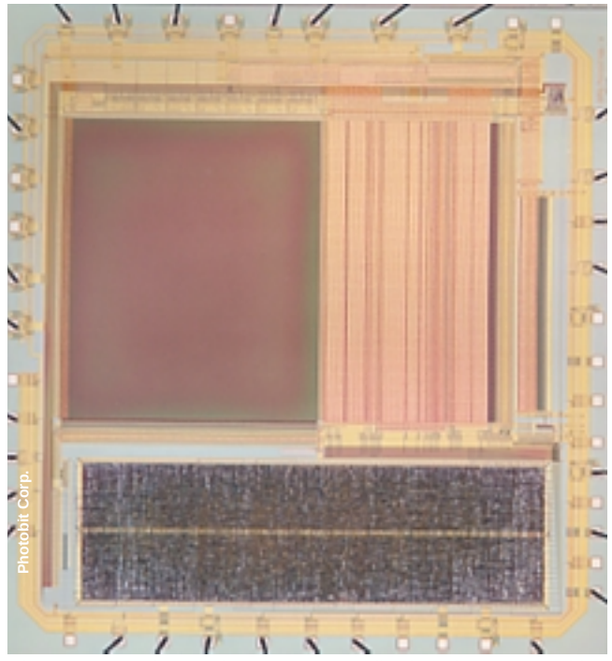

Figure 1A An imager for consumer applications features on-chip signal processing and ADC.

advantages and drawbacks

Theoretically, the imaging performance of CMOS active pixel sensors can be competitive with that of CCD detectors. Both devices are made from silicon, which primarily determines the quantum efficiency response curve. The readout amplifier for both technologies is usually a floating-diffusion device sensed by a source-follower; the capacitance of the device determines the conversion gain. In addition, CMOS APS devices feature antiblooming capability and negligible smear.

Because the standard foundry techniques typically used to fabricate CMOS image sensors limit device performance, CCD detectors hold some advantages over the competing technology, including lower dark current and readout noise, and higher dynamic range. At a given temperature, the best CMOS image sensors suffer higher dark current than optimized CCD detectors, making the technology less appealing for high-end (low-light, scientific, and digital-still camera) applications. Although dark-current performance will improve somewhat, industry experts don't anticipate any large breakthroughs in sensors fabricated using almost-standard CMOS processes.

device architecture

One design issue that impacts performance is the readout signal chain, which includes the analog signal processor (ASP), the analog-to-digital converter (ADC), and the digital signal processor (DSP). The ASP performs functions such as sample-and-hold, correlated-double-sampling (CDS) for temporal noise suppression, delta-difference sampling (DDS) for fixed-pattern noise (FPN) suppression, analog image processing, and programmable-gain amplification. These functions can be globally implemented or implemented in a column-parallel architecture in which each column of the pixel array contains its own ASP. The pros and cons of each approach primarily concern power dissipation, image quality, and chip size.

On-chip ADC is a major advantage for CMOS image sensors in many applications. Since the ADC is typically a major

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age

Once the undisputed kings of electronic imaging, charge-coupled-device (CCD) detectors now face increasingly strong competition from complementary-metal-oxide semiconductor (CMOS) image sensors. As the consumer market begins to open up for CMOS imagers, manufacturers are eyeing the scientific market, traditionally a stronghold of high-performance CCD detectors. This month's ***oe****magazine* puts the spotlight on CMOS imagers in the following two perspectives by industry experts Eric Fossum and Albert Theuwissen, which examine the state of the technology and fabrication methods used to further enhance performance.

Building a Better Mousetrap

Modified CMOS processes improve image sensor performance.

By Albert Theuwissen and Edwin Roks, Philips Semiconductors Image Sensors

When charge-coupled device (CCD) detectors entered the consumer camcorder market two decades ago, they faced a challenge from metal-oxide semiconductor (MOS) image sensors, which were based on the same principle as today's complementary-metal-oxide-semiconductor (CMOS) imagers. Excessive image nonuniformity, or fixed-pattern noise (FPN), blocked MOS detectors from commercial success, however.

By leveraging improved architecture and fabrication technology, CMOS image sensors have returned to challenge CCD detectors. Enhanced technology has provided new options to the designer, and today's low-end CMOS products can compete with the more traditional technology.

design and operation

CMOS imagers transport their information toward the outside world through many different output stages, more or less in parallel. A CMOS *xy*-addressable imager consists of a matrix of photodiodes, each of which is provided with a MOS transistor that acts as a switch.

Passive-pixel CMOS imagers—simple photodiodes with addressing transistors in every pixel—suffer from high levels of noise and FPN. By integrating amplifier circuitry with each pixel to create an active pixel sensor (APS), designers can boost the signal-to-noise ratio (SNR) of the device, achieving FPN and overall noise performance that is an order of magnitude better than passive designs. The pixel itself only includes the driver transistor; the load of the source-follower is common for all pixels belonging to the same column.

To convert two-dimensional spatial information into the serial stream of electrical signals, electronic scan circuits read out each pixel sequentially. At the beginning of a new field, the vertical scan circuit selects a row of pixels by setting a high DC voltage on all gates of the MOS switches of the row. Next, the horizontal scan circuit selects the pixels in one particular column using the same technique. As a result, only one pixel in the two-dimensional matrix has a high DC voltage on both the row and the column switch, which electronically selects it for readout. After the pixel dumps its information into the output stage, it is reset to begin a new integration, and the readout process progresses to the next pixel in the row.

The most common pixel architectures for APSs are photogate conversion and photodiode conversion (see figure 2). In the photogate design, once the scan circuitry has selected a pixel, a pulse on the transfer gate triggers the transport of data from the photosensitive area toward a floating-diffusion amplifier. The photodiode pixel looks very similar to the photogate pixel, except for the additional transport of data from the converting site toward the output diffusion.

enhancing performance

Manufacturers initially fabricated CMOS image sensors using DRAM processes, which are characterized by 0.6-µm minimum feature sizes, a single level of polysilicon, and triple layers of metal. Though economical, DRAM processes yield devices with sensitivity and noise problems.

The first step in overcoming these performance drawbacks is to switch from a DRAM process to an analog CMOS process. Although it is more complex, the approach offers enhanced fabrication capabilities for capacitors, accurate resistors, and well-matched transistors, yielding devices with improved FPN and imaging performance. The resultant image sensors are still not up to the level of CCD detectors, however.

To improve the imaging quality of a device, manufacturers must alter an existing CMOS process to optimize the spectral response and/or noise performance. SeeMOS (Philips Semiconductors Image Sensors; Eindhoven, Netherlands), for example, is an optimized 0.35-µm CMOS process designed to manufacture high-quality CMOS image sensors.

Improving sensitivity

In theory, a photodiode-based APS pixel can show great light sensitivity, but devices fabricated via standard CMOS processes are hampered by shallow photodiode junctions and limited fill factors. Process adjustments can compensate for these drawbacks, however.

Standard CMOS processes yield photodiode junctions that are only about 0.25 µm deep, providing sensitivity to blue and green light, but almost no response to red wavelengths. Red photons penetrate up to 3 µm into the silicon before absorption and are lost if the depletion layer around the metallurgical junction does

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source of power dissipation, however, it must be implemented carefully. Column-parallel ADCs offer the lowest power dissipation and the highest throughput.

DSP, which includes sensor control, color processing, image compression, and image processing, can be performed on-chip or off-chip. Although not necessarily cost-effective, on-chip DSP minimizes form factor and simplifies design. The drawbacks are increased power dissipation and cost as well as susceptibility of the ASP to digital clocking noise. Since DSP is implemented using digital logic, use of a more advanced digital fabrication process may reduce system costs.

FPN historically has been a major performance limiter for CMOS APS devices. Pixel-to-pixel lithographic variations that affect both optical collection efficiency and capacitance are the primary causes of random FPN in CMOS imagers. Although the FPN is comparable to that of CCD detectors, the inconsistencies result in an effective photons-to-volts gain variation of 1% to 2% rms over the pixel array.

CMOS APS devices also suffer from pixel-to-pixel offset variations. Random offsets can be removed by the CDS technique. Column-parallel ASP and ADC architectures do reintroduce column-to-column offsets, but those can be removed by the DDS technique or by DSP.[1] The human eye is very sensitive to the vertical stripes produced by noise, however, and residual columnar FPN still can be detected in some CMOS images despite the small value (less than 1%).

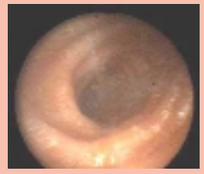
Given, Inc.

Figure 1B Designed to be swallowed, the "pill" camera incorporates a low-power CMOS sensor optical-quality chip-scale package to transmit images from inside the body.

consumer applications

An example of a common consumer CMOS image sensor is the 352 × 288 pixel common intermediate format (CIF) device (see figure 1A on page 28). Incorporating an architecture of three transistors per pixel, the 0.1 Mpix sensor is designed for 5.2 mm optics and hence has a pixel size of 7.9 × 7.9 µm. A red-green-blue filter overlaying the pixel array allows RGB data to be estimated and displayed for each pixel. The device features a column-parallel ASP that includes a PGA with gain from 0.125 to 31.875 in steps of 0.125. It also contains an 8-bit, low-power flash ADC. The output data is either 8-bit parallel-byte mode or 4-bit parallel-nibble mode.

By using a serial interface, the user can program window readout size and location, signal gain, exposure parameters, frame rate, and biasing. The sensor operates up to 40 frames/s with an output date rate of 6 Mb/s and a power dissipation of 100 mW at 3.3 V. At a faceplate illuminance of 1 lux, the sensor has an SNR greater than 20 dB (10:1) at 30 frames/s. The internal (pre-ADC) dynamic range is approximately 75 dB.

high throughput image sensor

CMOS APS devices with on-chip ADC achieve very high throughput image capture. The column-parallel ADC architecture permits simultaneous analog-to-digital conversion of an entire row of pixels. In addition, parallel digital output ports allow efficient output of digital image data, simplifying system implementation and reducing data interference and crosstalk.

To avoid the introduction of FPN, the thousand or more ADCs on the sensor chip must have very similar characteristics. Furthermore, each ADC must have a very low power-per-conversion-rate figure-of-merit to minimize the power consumption of the ADCs as a group.

An example of such a device is a 780 Mpix/s color sensor with an 80 MHz master clock rate and 10 parallel 10-bit output ports. The image sensor features 1280 × 1024 pixels (1.3 Mpix), which is DSC resolution, and an integration time that can be less than 1.6 µs. Each 12 × 12 µm pixel contains an in-pixel memory for simultaneous integration of all pixels, also known as a freeze-frame shutter.

One of the key parameters for a freeze-frame shutter is its efficiency because the use of fast shutters implies a large photon flux. Excess signal must not contaminate the desired signal in the in-pixel memory and hence must be efficiently discarded. The shutter efficiency for the above sensor is better than 99.95%.

The sensor also contains 1280 self-calibrating ADCs operating in parallel. Each ADC performs its conversion in under 2 µs to a resolution of 10 bits and dissipates approximately 120 pJ/conversion. FPN between ADCs is less than 2 bits rms. Total sensor power dissipation is less than 500 mW at 600 frames/s.

"pill" camera sensor

Battery-powered portable applications require devices with very low power dissipation. This performance can be achieved by using low supply voltages (e.g. 2.7 V) and through the use of power-efficient circuit design; for example, a QCIF format sensor (176 × 144 pixels) with on-chip ADC and serial digital output dissipates only 48 mW when operating at 1.2 V and 20 frames/s, or 95 pJ/output-pixel.[2] This can be compared to the 33 × 103 pJ/output-pixel of the CIF sensor described above, which in turn is more power-efficient than a functionally equivalent CCD chip set.

Photobit Corp. (Pasadena, CA) has developed a custom sensor designed for a specialized medical device that combines the imager, a pulsed light source, optics, a radio frequency (RF) transmitter, and a battery, all encapsulated in a small pill that can be swallowed by a patient (see figure 1B). The "pill" camera captures an image on an interval basis and transmits it out of the body. The color sensor is a 256 × 256 pixel array with 10 µm pixel pitch and 8-bit on-chip ADC. Total sensor power dissipation is less than 2 mW at 2 frames/s with 2.8 V supply voltage (see *OE Reports*, August 2000).

CMOS APS technology is finding other unique applications in areas such as security, automotive systems, document scanning, and high-speed inspection. The technology lends itself to radiation-hardened sensors for space applications and

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not reach these depths. Designers can compensate for this effect by introducing extra boron or phosphorus implantations into the standard CMOS process, providing a deeper depletion layer to capture the generated electrons.

Low fill factor (the ratio of active region to total pixel area) also reduces device sensitivity. Each pixel in the detector array incorporates at least three transistors, which occupy the same area as the photosensitive active region. Because the transistors are not light sensitive, their presence drops the per-pixel fill factor to as low as 25%.

Microlenses can counteract this effect by focusing the photons that would normally impinge on the transistors onto the active area, improving sensitivity by a factor of 2.5. Unfortunately, microlensed image sensors show a strong dependency of sensitivity as a function of the incident angle of the incoming rays. This effect can limit the benefits of the microlenses to larger *f*-numbers.

reducing noise

The noise in the video signal delivered by a CMOS image sensor consists of photon shot noise, dark-current shot noise, reset noise, and thermal noise. Photon shot noise is the uncertainty of the amount of photons falling on a pixel. In video applications, the human eye filters out this noise component, but in digital still images, the presence of photon shot noise can seriously hamper sensor performance.

Dark-current shot noise is the noise component generated by pixels in the absence of illumination. Dark current itself can be canceled out and dark-current nonuniformities can be corrected by means of an additional frame store, which is extra memory that can contain a complete frame or picture. Most of today's CMOS imagers focus on low-end applications, however, so an additional frame store is not always affordable.

Although dark-current shot noise is impossible to eliminate, designers can reduce the effect of the shot noise, as well as that of FPN, by minimizing overall dark-current generation. One technique involves the use of pinned photodiodes, in which a shallow p^+ layer on top of the photodiode fills the interface states by means of holes, preventing them from generating dark current.

Another noise source, pixel-reset noise, can be the limiting factor on the SNR of the imager. After every reset action, the capacitance of the floating diffusion is recharged through the reset resistor, which generates noise. Reset noise can be canceled out by means of correlated-double sampling (CDS), in which reset noise is measured alone, then subtracted from the measurement of video signal plus the reset noise.

CDS also cancels the major part of the 1/*f* noise. To perform CDS, the device must include an electron collection site and a separate measuring site on each pixel. Pixels with a single photodiode architecture are not compatible with CDS, but photogate architecture is well-suited to the technique. As always, there are tradeoffs. Although the photogate design is compatible with CDS, it requires an extra transistor within every pixel, further reducing fill factor.

The final noise source is the thermal noise generated by the electronic circuitry present in every pixel. The CMOS pixel readout sequence minimizes thermal noise. The readout speed of every pixel is relatively low (one read cycle for every frame), so the bandwidth of the amplifier within every pixel is very small.

optimizing architecture

CMOS imager performance depends on the architecture of the individual pixel as well as that of the overall image sensor. Unlike CCD detectors, basic CMOS imagers use a rolling integration cycle in which the beginning and end of the integration period differs for each pixel. This approach can yield poor results when integration times are short, or when the device is operated with flash lamp, strobe, or fluorescent light.

To achieve simultaneous pixel integration—freeze-frame shutter—the device requires in-pixel storage capability, which can be realized at the cost of an extra transistor and extra capacitor within every pixel. In some cases this architecture can provide both extra storage and CDS capability, though not simultaneously. Such devices operate in one of two modes: synchronous integration or CDS.

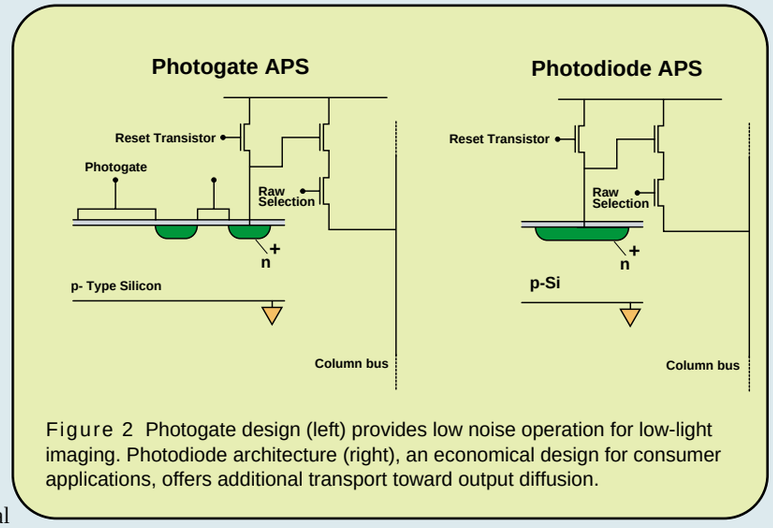

Figure 2 Photogate design (left) provides low noise operation for low-light imaging. Photodiode architecture (right), an economical design for consumer applications, offers additional transport toward output diffusion.

CMOS designers have the option of performing on-chip analog-to-digital (A/D) conversion. Conversion can be implemented with a single A/D converter (ADC), but the converter must operate at the speed dictated by the application. A VGA imager (640 × 480) operating at 60 frames/s, for example, forces a 20 MHz conversion rate. To implement a low-power ADC with these characteristics on-chip is a challenge.

The speed issue can be overcome by introducing an ADC on every column, which, in this example, would lower the operating rate required of each circuit by a factor of 640. The main drawback of the per-column approach is the reduction in fill factor. For a VGA image sensor with 5-µm pixels that is fabricated with a 0.5-µm process, the ADC would occupy 50% of the area of the focal plane. This ultimately is a very high price for this type of architecture. Not surprisingly, most commercial products still use a single-ADC solution.

looking to the future

CMOS imagers benefit from improvements to semiconduc-

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x-ray-sensitive systems that are deployed in dental and osteoporosis diagnostic equipment.

Over the next five years, the industry will see an increasing trend toward on-chip integration of camera functions as well as many embedded imaging applications. Power levels will continue to drop. A new window of opportunity will open as standard CMOS plunges into the deep submicron range with feature sizes in the 0.13 to 0.15 µm range, allowing increasing in-pixel functionality. The lower cost of CMOS-based image sensor systems will permit the widespread use of imaging in automotive applications, toys, and consumer appliances. **oe**

Eric Fossum is chief technology officer at Photobit Corp., 135 N. Los Robles Ave. 7th Floor, Pasadena, CA 91101, USA. Phone: 626-683-2200; e-mail: fossum@photobit.com

Acknowledgments

This article summarizes the achievements of the engineers of Photobit Corp. Their contributions are greatly appreciated, as are the contributions of Photobit's foundry partners, Tower Semiconductor, UMC, and TSMC.

References

1. R.H. Nixon et al., IEEE J. Solid-State Circuits, **31***[12], pp. 2046-2050 (1996).*

2. K-B Cho, A. Krymski, and E.R. Fossum, Proc. 2000 IEEE International Solid-State Circuits Conference, pp. 114–115, San Francisco, California (2000).

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tor fabrication technology. Although the external optics for the imager determine the focal plane area, both the on-chip electronics and the in-pixel circuitry can become much smaller as manufacturers develop more aggressive technologies.

Unfortunately, although the new technologies shrink circuitry dimensions, they also severely limit the imaging function in the following ways: Metallurgical junctions become shallower, which degrades light sensitivity and increases dark current; salicidation of the junctions minimizes resistivity but renders the junctions opaque to incoming photons; increasing numbers of metallic layers raise the physical height of the overall stack, hampering the light sensitivity, even in the case of microlenses; and shrinking power supplies limit the dynamic range of the imagers.

Clearly it will be a challenge to fabricate high-performance CMOS image sensors using standard processes designed for critical dimensions smaller than 0.18 µm. To overcome the issues mentioned above, new processes will be needed to bring CMOS image sensors up to the performance level of CCD imagers. **oe**

Albert Theuwissen is R&D manager and Edwin Roks is project manager of SeeMOS Philips Semiconductors Image Sensors, Prof. Holstlaan, 4, 5656AA Eindhoven, The Netherlands. Phone: +31-40-274-2734; fax +31-40-274-4090; e-mail: albert.theuwissen@philips.com or edwin.roks@philips.com