CHAPTER 5

CHARGE-PACKET DIFFERENCER CIRCUIT

5.1 Introduction

The charge-coupled differencer circuit discussed in this chapter is a novel implementation of the functional block discussed in chapter 2. This circuit creates an output charge packet equal in magnitude to the difference in magnitudes of two input charge packets. The advantage of the implementation of the differencer presented in this chapter is that the physics of the device predict inherently linear transfer characteristics with exactly unity gain. In principle, the circuit can be fabricated using a minimal amount of real-estate, which makes it particularly attractive for charge-coupled computer array applications. A third important feature of this invention is that the origin of the input charge and the differencer electrodes can be separated by structures in the silicon yet connected by a wire passing over those structures, an advantage not normally enjoyed by charge-coupled devices.

In cooperation with the Hughes Aircraft Company's Corporate Patents Office, a novelty search was initiated revealing several circuits which perform a charge packet differencing operation. The prior art which was found to be the closest to the circuit disclosed in this chapter was invented by Fagan (1978). The primary differences between the two circuits are that first Fagan generates two voltages which are proportional (possibly with two different proportionality constants) to two reference charge packets. Fagan then uses two sequential fill and spill cycles utilizing one of these voltages on each cycle to generate the output charge packet. Such a technique produces an inherently non-linear relationship between input charge packet and requires more real
estate and more complicated timing than the circuit presented in this work.

There are two drawbacks to the new charge-packet differencer circuit. The first is that the input charge packets are destructively sensed. This nuisance can be circumvented in the charge-coupled computer by cloning the input charge packets prior to the sense operation through the utilization of the differencer's replicator mode. The second drawback is that the inherent unity gain is affected by stray capacitance. Since the stray capacitance is often a function of voltage, the change in gain appears as a distortion in the transfer characteristic. The stray capacitance can be minimized by proper layout and advanced fabrication technologies.

In the Yale 8205 implementation of the charge packet differencer, much larger geometries than what would be used in a true charge-coupled computer array were employed, due to the limitations imposed by fabricating the devices at Yale. The consequences of these oversized geometries were that charge transfer inefficiency, dark current and PN junction leakage current were all in excess of what they might be were a better facility available. These consequences are compounded due to interplay among the non-optimized characteristics. For example, to improve charge transfer efficiency, clocking rates were kept relatively slow. Such increased time intervals amplified the detrimental aspects of both dark current and leakage currents.

Even with the limitations imposed by the processing facility, the charge packet differencer implemented on the Yale 8205 chip demonstrated the validity of the performance predictions made based on initial analysis of the proposed structure. The device performs charge packet differencing in a linear and accurate way and has a large dynamic range.
In the sections which follow, the operation of the device will be discussed and the predicted performance analyzed. The device layout and the rationale for the chosen geometry will be covered, including a proposed layout for improved performance. Experimental results obtained from measurement of the fabricated devices will be examined and analyzed, including calibration of the output amplifier. This chapter will end with a summary of the results obtained by this work and conclusions regarding future directions.

5.2 Theory of Operation

Basic Operation

To assist in the discussion of the basic operation of the charge packet differencer circuit, a schematic series of drawings is shown in Fig. 5.2-1. In Fig. 5.2-1a, a cross-section showing two input charge packets $Q_{SA}$ and $Q_{SB}$ in storage wells $V_{WA}$ and $V_{WB}$ isolated from floating $p^+$ diffusions by output transfer gates $V_{XA}$ and $V_{XB}$ is displayed. The floating diffusions are wired to two electrodes labelled A and B, which are also connected via a MOSFET switch to the precharge potential $V_0$. Next to electrode A is an isolation gate $V_{X2}$ and an input diode reverse biased by $V_{D2}$. Adjacent to electrode B is an output transfer gate $V_{XO}$. These latter four gates, input diode and precharge MOSFET switches comprise the charge packet differencer. In Fig. 5.2-1a, the precharge switches have been momentarily closed by pulsing $V_{PCS}$ to some negative bias larger than $V_0 + V_T$, where $V_T$ is the (negative) MOS threshold voltage. When this negative bias is removed and the switches open the circuit, the two differencer electrodes A and B remain precharged at a floating voltage $V_0$. The negative charge on each gate is $Q_A$ and $Q_B$ respectively.

In Fig. 5.2-1b, the output transfer gates $V_{XA}$ and $V_{XB}$ have been biased to a negative voltage larger than $V_{WA}$ and $V_{WB}$ respectively,
5.2-1 Schematic drawings of charge packet differencer circuit showing the three major phases of operation.

a. Precharge phase. Electrodes A and B are precharged to potential $V_o$ by pulsing $V_{PCS}$. 
b. Gate charge subtraction phase. Signal charge recombines with a portion of the negative gate charge altering the potential wells under electrodes A and B.
causing the positive minority carrier charges $Q_{SA}$ and $Q_{SB}$ to be collected by the floating diffusions. The positive minority carrier charge recombines with a portion of the negative charge on electrodes A and B, resulting in a reduced charge on each electrode. To ensure complete charge transfer, the precharge voltage must be large enough to ensure that the floating diffusion bias $V_0$ after recombination is still larger than $V_{WA} + V_T$, and $V_{WB} + V_T$. The new negative charges on each differencer electrode $Q_A$ and $Q_B$ are given by

$$Q_A = Q_A + Q_{SA}$$  \hspace{1cm} 5.2-1a
$$Q_B = Q_B + Q_{SB}$$  \hspace{1cm} 5.2-1b

This gate charge subtraction process is very similar to the operation of the output charge packet sense amplifier discussed in appendix D.

In Fig. 5.2-1c, the input diode ($V_{D2}$) has been momentarily forward biased with respect to the semiconductor surface under electrodes A and B, filling the potential wells under those gates with minority carrier charge. When the diode is returned to a reverse bias condition, a portion of the injected carriers spill out from the potential wells back to the diode and the rest are trapped in the potential well under electrode B. This process is wholly analogous to the Tompsett surface potential equilibration method of creating a charge packet (as discussed in chapter 2) except in this device the gate charge is fixed rather than the gate voltage.

The charge trapped under electrode B can be determined using Gauss' Law in the following manner. Since the spill process described above terminates when the surface potential under the two electrodes are equal, Eq. 2.3-10a is used to argue that the depletion layer charge areal densities under the two electrodes are equal. This assumes that there is a negligible potential drop across the minority carrier
inversion layer under electrode B, which is reasonable for gate oxides zero in the 500 Å thickness range under moderate bias conditions. It is also necessary to assume identical doping profiles under each electrode, though the doping profile need not be constant. The charge on the gate electrode, charge in the oxide, interface trapped charge, depletion layer charge and in the case of electrode B, the charge in the potential well is summed, and assuming zero electric field outside the MOS sandwich, one obtains from Gauss' Law:

\[
\frac{Q_A}{A_A} + Q_{OA} + Q_{ITA} + Q_{DA} = 0
\]

\[
\frac{Q_B}{A_B} + Q_{OB} + Q_{ITB} + Q_{DB} + \frac{Q_O}{A_B} = 0
\]

where \(A_A\) and \(A_B\) are the areas of electrodes A and B, \(Q_{OA}, Q_{OB}, Q_{ITA}\), and \(Q_{ITB}\) are the fixed oxide charge and interface trapped charge areal densities on electrodes A and B, \(Q_{DA}\) and \(Q_{DB}\) are the depletion layer charge areal densities under electrodes A and B, and \(Q_O\) is the minority carrier charge trapped in the potential well under electrode B.

The depletion layer charge densities in Eqs. 5.2-2 and 5.2-3 are evaluated and the charge packet \(Q_O\) solved for. It is assumed (as is reasonable) that the oxide and interface trapped charge in the two MOS capacitors are identical. This yields

\[
Q_O = \frac{A_B}{A_A} \cdot \frac{Q_A}{Q_B} - \frac{Q_A}{Q_B}
\]

which relates the magnitude of the captured charge packet to the charge on the two electrodes. This latter charge can be rewritten using Eq. 5.2-1, and by recognizing that in the precharged state, the areal gate charge densities must be equal (i.e. \(Q_A/A_A = Q_B/A_B\)). Thus,

\[
Q_O = \frac{A_B}{A_A} \cdot Q_{SA} - Q_{SB}
\]
Noting that a negative number of minority carriers cannot be captured, the chapter 2 notation is adopted so that

\[
\frac{Q}{\text{A}} = \begin{bmatrix}
\frac{A_B}{A_A} & Q_{SA} - Q_{SB}
\end{bmatrix}
\]

This is the basic equation of operation of the charge packet differencer.

If the differencer electrodes are of equal area, the most useful differencer operation is obtained, that of unity gain. Such a characteristic is desired for the charge-coupled computer. Note that if the B channel input charge packet is zero, the differencer acts as a charge packet replicator. Such a replicator might be designed with unity gain (equal electrode areas), as an attenuator \((A_B < A_A)\) or as an amplifier \((A_B > A_A)\). The latter situation is particularly intriguing since it may be well suited for low noise amplification of small charge packets, however this possibility is not pursued here.

In a final phase not illustrated in Fig. 5.2-1, the newly formed output charge packet \(Q\) may be transferred from the differencer in the usual CCD fashion. At this stage, the differencer may be reset by pulsing the MOSFET precharge switches. Another option is to pulse the diode instead, to fill the potential well under electrode B a second time. In this multiple cycle mode of operation, the differencer (or replicator) acts as a charge packet copying machine. This feature is particularly useful if subsequent circuits utilizing the created charge packet are destructive in nature. The re-generated charge packets may
5.2-2 Timing diagram for charge packet differencer operation. Basic cycle is

1. Precharge phase and prepare input charge packets.
2. Gate charge subtraction phase and differencer fill.
3. Differencer spill.
4. Transfer output charge packet.

Copy cycle is:

1. Reset output amplifier (optional) and differencer fill.
2. Differencer spill.
3. Transfer output charge packet.
also be summed to form a larger charge packet which is a discrete multiple of the original. Note also that more than one input operation can take place, with the differencer electrode acting as a summation node during the gate charge subtraction process.

A timing diagram for the basic operation of the differencer circuit is shown in Fig. 5.2-2. Although more difficult to conceptually visualize, the gate charge subtraction phase (pulsing \( V_{XA} \), \( V_{XB} \)) can be coincident with the differencer's fill phase (pulsing \( V_{D2} \)). This timing reduces the total time required to complete the differencing operation.

**Charge Handling Capability**

The maximum charge which can be input into the differencer depends upon the precharge bias \( V_0 \), and the area of the electrodes. The A electrode is more critical than the B electrode. If too much charge is subtracted from the B electrode during the input phase, the output charge packet will be zero. However, if too much charge is subtracted from the A electrode, the output will saturate, or even be reduced, depending upon the timing. The device saturates when the effective voltage on the A electrode becomes comparable to the MOS threshold voltage \( V_T \). Once the A electrode is less than \( V_T \), the fill and spill operation is hampered.

The maximum precharge voltage which can be applied to electrode A is determined by the breakdown strength of the deep depleted silicon under the electrode. If the breakdown field strength is \( \mathcal{E}_{BR} \), the maximum precharge voltage is given by (assuming no interface trapped charge)

\[
V_o^{MAX} - V_{FB} = \frac{\varepsilon_s \varepsilon_0}{C_{OX}} \mathcal{E}_{BR} + \frac{\varepsilon_s \varepsilon_0}{2qN_D} \mathcal{E}_{BR}^2 \tag{5.2-7}
\]

For \( N_D = 1 \times 10^{16}/\text{cm}^3 \), the silicon breakdown strength is approximately
2.5 \times 10^5 \text{ V/cm} \ [\text{Goetzberger and Nicollian, 1967}]. \text{ For } d_{\text{ox}} = 550 \ \AA, \text{ the maximum precharge voltage is 24 volts. The maximum gate charge is then given by Gauss' Law as}

\begin{equation}
\frac{q_{\text{A}}}{A_{\text{A}}} + s_{\text{s}} e_{\text{o}} \varepsilon_{\text{BR}} = 0
\end{equation} \tag{5.2-8}

After the maximum input charge has been subtracted from the gate, the effective voltage is \( V_T \). The new gate charge is given according to

\begin{equation}
\frac{q_{\text{A}}}{A_{\text{A}}} + q_{\text{DA}} = 0
\end{equation} \tag{5.2-9}

where \( q_{\text{DA}} \), the minimum depletion layer charge density is obtained by setting the surface potential equal to \( 2\phi_n \) such that

\begin{equation}
q_{\text{DA}} = (4\phi_n q_{\text{s}} e_{\text{o}} N_D)^{1/2}
\end{equation} \tag{5.2-10}

The maximum input charge packet is the difference between \( q_{\text{A}} \) and \( q_{\text{A}} \) and is

\begin{equation}
q_{\text{SA}}^{\text{MAX}} = A_{\text{A}} (e_{\text{o}} \varepsilon_{\text{BR}} - 4\phi_n q_{\text{s}} e_{\text{o}} N_D)
\end{equation} \tag{5.2-11}

Evaluating this quantity gives a value of \( q_{\text{SA}}^{\text{MAX}} / A_{\text{A}} \) of 0.21 \( \mu \text{C/cm}^2 \). The maximum output charge packet is determined by Eq. 5.2-6 and is

\begin{equation}
q_{\text{O}}^{\text{MAX}} = A_{\text{B}} (e_{\text{o}} \varepsilon_{\text{BR}} - 4\phi_n q_{\text{s}} e_{\text{o}} N_D)
\end{equation} \tag{5.2-12}

and has the same value \( q_{\text{O}}^{\text{MAX}} / A_{\text{B}} = 0.21 \ \mu \text{C/cm}^2 \).

If the differencer is not operated at full capacity, the maximum input signal charge is given by

\begin{equation}
q_{\text{SA}}^{\text{MAX}} = A_{\text{A}} (e_{\text{o}} \varepsilon_{\text{BR}} - 4\phi_n q_{\text{s}} e_{\text{o}} N_D)
\end{equation} \tag{5.2-13}
where

\[ \xi = \left[ \left( \frac{qN_D}{C_{ox}} \right)^2 - \frac{2qN_D(V_o-V_{FB})}{\varepsilon_S\varepsilon_o} \right]^{1/2} - \frac{qN_D}{C_{ox}} \]  

5.2-14

The maximum output charge packet is also given by Eq. 5.2-13 with \( A_B \) replacing \( A_A \).

**Effect of Stray Capacitance**

The effect of stray capacitance is primarily to attenuate the output of the charge packet differencer. Because the stray capacitance is a function of effective differencer electrode voltage, the associated change in attenuation factor introduces non-linearity into the transfer characteristic. The stray capacitance can be divided into three major components. The first is the stray capacitance due to the floating p⁺ diffusions. The second is due to the underlap capacitance between the floating p⁺ diffusions and adjacent transfer electrodes. The third component is due to stray wiring capacitances. Because the wiring can be done over thick oxide, it can be quite small. The underlap capacitance can be reduced by using a self-aligned implanted diffusion process. The floating p⁺ diffusion can be minimized by reducing the area of these regions.

To quantitatively calculate the effect of stray capacitance one begins by writing a statement of charge conservation on the differencer electrodes:

\[ Q_A + Q_{SCA} = Q_A + Q_{SCA} + Q_{SA} \]  

5.2-15a

\[ Q_B + Q_{SCB} = Q_B + Q_{SCB} + Q_{SB} \]  

5.2-15b

where \( Q_{SCA} \) and \( Q_{SCB} \) are the negative charges stored on the stray capacitance. Substituting these relationships into Eq. 5.2-4 yields
\[ Q_0 = \frac{A_B}{A_A} Q_{SA} - Q_{SB} - \Delta Q_0 \]  

where

\[ \Delta Q_0 = \frac{A_B}{A_A} (Q_{SCA} - Q_{SCA}) - (Q_{SCB} - Q_{SCB}) \]  

5.2-17

The difference in charge stored on the stray capacitance can be expressed approximately by the product of the differential stray capacitance \((C_{SCA}, C_{SCB})\) and the change in interelectrode effective voltage.

\[ Q_{SCA} - Q_{SCA} = C_{SCA} (V_A' - V_A) \]  

5.2-18a

\[ Q_{SCB} - Q_{SCB} = C_{SCB} (V_B' - V_B) \]  

5.2-18b

Substituting these relationships into 5.2-17 yields

\[ \Delta Q_0 = \frac{A_B}{A_A} C_{SCA} (V_A' - V_A) - C_{SCB} (V_B' - V_B) \]  

5.2-19

If the electrode areas are equal, and if the differential stray capacitances are equal \((C_{SC})\), Eq. 5.2-19 can be simplified to

\[ \Delta Q_0 = C_{SC} (V_A' - V_B') \]  

5.2-20

since \(V_A\) and \(V_B\) are equal.

Finally, recognizing that

\[ -Q_0 = C_{OX} (V_B' - V_A') \]  

5.2-21

one obtains

\[ \Delta Q_0 = \frac{C_{SC}}{C_{OX}} Q_0 \]  

5.2-22

and Eq. 5.2-16 becomes

\[ Q_0 = \sigma_{SC} \left[ Q_{SA} - Q_{SB} \right] \]  

5.2-23

where the stray capacitance attenuation factor \(\sigma_{SC}\) is defined as

\[ \sigma_{SC} \Delta (1 + C_{SC}/C_{OX})^{-1} \]  

5.2-24
Although, in general, the stray capacitance attenuation effect is undesirable, it is possible to convert this to a feature. If the stray capacitance can be controlled by a bias voltage, or more ideally, by a charge packet (perhaps under floating gate capacitor), it may be possible to construct a device which does charge packet differencing and multiplication (division). This possibility is not pursued further here, but it may be worthy of future investigation.

**Effect of PN Junction Leakage Current**

The floating $p^+$ diffusions in the charge packet differencer are, of course, reverse biased PN junctions in which a non-zero reverse 'leakage' current flows. This current discharges the differencer electrodes in the same manner discussed in appendix D regarding amplifier droop. The discharge rate is simply

\[
-Q_A = J_{LA} \cdot A_{DA} \quad 5.2-25a
\]

\[
-Q_B = J_{LB} \cdot A_{DB} \quad 5.2-25b
\]

where $J_{LA}$ and $J_{LB}$ are the current densities through the floating diffusions with areas $A_{DA}$ and $A_{DB}$ respectively. These currents depend upon the quality of the diffusions and the effective differencer electrode bias. The higher the bias, the larger the current. For poor quality diffusions, soft breakdown of the junction may occur for large precharge biases leading to large and unpredictable current levels.

If an interval $\Delta t$ elapses between the time the electrodes are precharged and the time the output charge packet is formed, the total discharge is given by

\[
AQ_A = - J_{LA} A_{DA} \Delta t \quad 5.2-26a
\]

\[
AQ_B = - J_{LB} A_{DB} \Delta t \quad 5.2-26b
\]

assuming a constant discharge current during the interval. The output
charge packet, assuming equal floating diffusion areas, is determined by

\[ Q_0 = q_{sc} \left[ Q_{sa} - Q_{sb} - A_B \Delta t (J_{la} - J_{lb}) \right] \]

It is interesting to note that if the discharge currents are equal, there is a net null effect on the output charge packet except that the saturation level will be reduced. However, in most cases of interest the B electrode will have a larger effective voltage than the A electrode, and \( J_{lb} \) will be larger than \( J_{la} \). The consequence will be increased attenuation for increased output charge packets, and increased attenuation for longer intervals. The latter effect will be particularly pronounced for poor junctions when the differencer is operating in a multiple cycle copier mode.

**Effect of Dark Current**

The differencer circuit is virtually immune to bucket dark current in the same way as the Tompsett surface potential equilibration method is immune. Dark current collected in either the spill bucket or the metering well will either result in premature formation of the charge packet, or be spilled toward the input diode if the metering well is already full. The exception to this immunity occurs during the output transfer phase when dark current integrated over the output transfer phase interval may be included in the output packet.

5.3 Device Layout and Fabrication

**Yale 8205 Layout**

The layout of the charge packet differencing experiment fabricated on the Yale 8205 test chip is shown in Fig. 5.3-1, and a photograph of an actual device is shown in Fig. 5.3-2. There are three major stages to this layout; the input charge packet formation stage, the differencer
5.3-1 Layout of fabricated experimental device showing input stage (A and B channels) and charge packet differencer. Interelectrode gap size exaggerated.
Photograph of fabricated device (7B20).
circuit, and the output stage. The latter is discussed in detail in appendix D.

The input stage consists of two parallel but isolated fill and spill charge packet formation channels, A and B. Each channel has an input diode which are connected in parallel and biased by $V_{D1}$. The input diodes are gated by spill electrodes which are also connected in parallel and biased by $V_{X1}$. Each channel has an independent metering well biased by $V_{WA}$ and $V_{WB}$. The metering well sizes are 101 mils$^2$ each. Using these two electrodes and input diode, each channel can produce signal charges $Q_{SA}$ and $Q_{SB}$ for input into the charge packet differencer. Each input structure terminates with an output transfer gate controlled by $V_{XAB}$ followed by a floating $p^+$ diffusion. The area of the floating diffusion is 20 mils$^2$ which includes a 4 mils$^2$ underlap with the output transfer gate. As will be discussed in section 5.5, this underlap constitutes a major portion of the differencer electrodes' stray capacitance.

The floating $p^+$ diffusion is connected via a 1 mil wide wire over an isolation channel stop to the charge packet differencer electrode. The area of each differencer electrode is 138 mils$^2$. Each differencer electrode is also connected to a floating diffusion of the precharge MOSFET (also isolated by the channel stop diffusion). The area of this diffusion is 18 mils$^2$. The A differencer electrode is adjacent to an input gate ($V_{X2}$) and input diode ($V_{D2}$). The B differencer electrode is juxtaposed an output gate ($V_{X0}$) and a floating diffusion wired to the output sense amplifier MOSFET gate (as described in appendix D).

The circuit shown in Fig. 5.3-1 was designed to be compact, reduce bonding sites, and incorporate as much symmetry as possible. The latter was chosen for balance so that parasitic effects might tend to cancel.
In fact, although the bonding pad count was an issue, as was compaction, these self-imposed constraints led to a design which, with hindsight, was not optimized. The circuit performs as designed and certainly demonstrates the basic principles of its operation. However, the author feels it might be instructive for future investigators if a few words are devoted to a critique of this layout.

The most serious error committed in this layout was that the A and B input channels, and A and B precharge switches were tied in parallel. Although this reduces the bonding pad count, experimentally it makes it impossible to independently bias each differencer electrode. This type of operation is important when testing of the chip is underway and faults are being traced. For example, with the present layout there is no way to test for a short between the two differencer gates.

A second oversight was that the W/L ratio of the differencer electrodes was made less than unity. This was convenient from a compaction point of view, but the effect this layout has on charge transfer rates was underestimated. As a consequence, the differencer operates much slower than it might were the layout optimized.

Finally, the stray capacitance effects were not fully analyzed at the time of layout so that floating p+ diffusion capacitance, underlap capacitance and wiring capacitance were not reduced to their minimum values. Optimizing these parameters would have led to a greater demonstrable accuracy in the Yale 8205 experimental device.

Although the above issues are glaringly obvious in the course of retrospection, the reader should take note that when the Yale 8205 chip was laid out, primary concern was concerned with broader questions, such as if the channel stop isolation technique would work, or if the submicron gap technology would work, or even if the predicted operation of
the differencer was indeed correct. Lesser details such as minimizing stray capacitance escaped attention at the time.

**Proposed Improved Layout**

In light of the observations made in the preceding paragraphs, an improved layout suitable for fabrication at Yale without process modification is presented in Fig. 5.3-3. The changes include stretching out the differencer electrodes to achieve a greater W/L ratio without changing the area. There is no reason not to continue to stretch the geometry other than that the sub-micron gap yield is reduced for longer gaps. In the improved layout, the W/L ratio has been increased from its previous value of approximately 2/3 to 17/2, an improvement factor of over an order of magnitude. The layout could probably be stretched another factor of two. As proposed, the charge transfer time will be improved by more than an order of magnitude since the transfer time for diffusion limited transfer scales as $L^2$ [Carnes et al. 1972].

Another change is that the stray capacitance has been reduced as much as possible. In the improved layout, the channel stop diffusion (whose width has been cut in half) is covered with thick oxide, reducing wiring capacitance. The floating $p^+$ diffusion area has been reduced by using the same diffusion for both the precharge switch and input charge collector. The underlap capacitance has been significantly reduced by eliminating the underlap for input charge transfer which was unnecessary, and decreasing the size of the precharge MOSFET switch, which was overdesigned in the Yale 8205 layout.

The third improvement (which may be unnecessary) was to change the precharge MOSFET into a dual gate device. In this new design, the gate closest to the floating $p^+$ diffusion acts as a screen gate which is d.c. biased, and the second gate performs the MOSFET switch function as
5.3-3 Proposed improved layout of charge packet differencer.
before. The purpose of the screen gate is to reduce 'reset noise' when the differencer electrodes are precharged to potential $V_o$. This is analogous to the output amplifier screen gate function described in Beynon and Lamb (1980, pg. 192). The cost of the screen gate is an added bias in the circuit and increased effective floating diffusion area. The utility of such a screen gate may not be apparent in a large geometry device when there are a billion or so electrons in the bucket, but for scaled geometries, the number of electrons decreases as $L^2$. In these cases, the screen gate may perform a necessary noise reduction function.

5.4 Experimental Results and Analysis

Output Amplifier Calibration

In appendix D, a simple theory describing the operation of the source-follower charge packet output sense amplifier was developed. The change in output voltage of the source-follower configured MOSFET was found to be related to a charge packet $Q_{SIG}$ according to

$$\Delta V_{OUT} = \frac{Q_{SIG}}{C_{OUT}}$$  \hspace{1cm} 5.4-1

where $C_{OUT}$ is the transcapacitance of the output MOSFET. The transcapacitance can be written in terms of the lumped output MOSFET gate capacitance $C_{AG}$ and the amplifier gain $g_A$ such that

$$C_{OUT} = g_A C_{AG}$$  \hspace{1cm} 5.4-2

By measuring the amplifier gain $g_A$ and transcapacitance $C_{OUT}$, the physical MOSFET gate capacitance can be ascertained.

To calculate the gain of the source-follower configuration, the precharge MOSFET switch was maintained in the closed or on condition and the voltage $V_{OA}$ was used to control the output MOSFET gate voltage. The output voltage $V_{OUT}$ was measured as a function of $V_{OA}$ for several values
of load resistance. This measurement for device 7B6 is shown in Fig. 5.4-1. The gain of the source-follower amplifier is experimentally determined from the slope of the transfer characteristic using

\[ a_A = \frac{dV_{OUT}}{dV_{OA}} \]  \hspace{1cm} 5.4-3

It is seen from the displayed measurement that the gain improves for increasing load resistances. From appendix D, note that

\[ a_A = 1 - \left[ \frac{2R_L \mu C_{OX} W}{L} (V_{OA} - V_T) + 1 \right]^{-1/2} \]  \hspace{1cm} 5.4-4

so that this dependence is expected. In order to cause the observed transfer characteristic to agree with Eq. 5.4-4, an effective value of \( W/L = 3-5 \) must be used, which gives good agreement over the range of load resistances examined. This same effective \( W/L \) value was observed when the normal (grounded source) I-V characteristics of the output MOSFET were analyzed. However, from the layout shown in appendix D, the design value of \( W/L \) was 33. Such a discrepancy can be explained in terms of high impedance inter-digitated source and drain fingers in the output MOSFET. The ohmic voltage generated in these fingers would be sufficient to cause most of the device current to flow at the base of the fingers. Indeed, the measured sheet resistance of the diffused \( p^+ \) layer for wafer 7B was 2.1 kΩ/□ due to a defective dopant source. (This problem was corrected and in lot 9 and the sheet resistance was reduced to 0.015 kΩ/□). For wafer 7B, the consequence of such a high diffused layer sheet resistance was to increase the minimum load resistance required to achieve near unity gain of the output amplifier. For wafer 7B devices, a load resistance of 1 MΩ in parallel with an oscilloscope impedance of 1 MΩ was chosen. From the slope of the 500 kΩ transfer characteristic, a gain \( a_A \) of 0.81 is observed.

To determine the output sense amplifier transcapacitance, a
DEVICE 7B6
SOURCE-FOLLOWER CONFIGURATION
$V_{PC A} = -25\text{VOLTS}$
$V_{DA} = -12\text{VOLTS}$

**Graph:**
- Y-axis: OUTPUT SIGNAL (VOLTS)
- X-axis: GATE VOLTAGE ($-V_{OA}$)
- Lines for different load resistances: 100MΩ, 500kΩ, 100kΩ, 10kΩ

5.4-1 Measurements of source-follower configured output MOSFET for various load resistance.
measurement of output voltage versus input charge packet was performed. For this measurement, the parallel channel of the charge packet initiated MOSFET junction switching experiment was utilized. A charge packet was formed using only the fill phase of the normal fill and spill technique. In this mode, the input diode is connected to ground (substrate) through an electrometer operating as an ammeter and the input gate is biased just above threshold so that a small current can flow between the diode and the metering well bucket. This current flows until the metering well bucket is filled and then ceases as the equivalent MOSFET source-drain voltage goes to zero. When the output transfer gate is pulsed, the charge transferred to the output sense amplifier \(Q_{\text{SIG}}\) consists of three components: the charge in the metering well bucket (proportional to the metering well voltage minus \(V_T\)), the charge under the input transfer gate (likewise proportional to the input transfer gate bias minus \(V_T\)), and the integrated current which flows from the input diode during the transfer interval. The input transfer gate bias is adjusted so that this latter component is small yet the current sufficient to fill the bucket in between output transfer cycles.

The total charge transferred during each cycle, when averaged over the cycle period \(T\), appears as a d.c. current through the input diode as measured by the ammeter. The current sensed by the ammeter is

\[ I = Q_{\text{SIG}}/T \]  

This current as a function of metering well voltage \((V_{\text{MW}})\) is shown in Fig. 5.4-2. The current over the metering well voltage range -5 to -10 volts is reasonably linear and has an equivalent slope \(dQ_{\text{SIG}}/dV_{\text{MW}}\) of approximately 34.0 pC/volt with a cycle period of one millisecond. This is close to what is predicted from the oxide capacitance.
5.4-2 Calibration of output charge packet sense amplifier by injection of charge packet from parallel channel. Measured current is ratio of injected charge packet to cycle period (one millisecond). Output signal of amplifier referenced to reset level.
Also shown in Fig. 5.4-2 is the change in output voltage (referenced from the reset level and hereafter referred to as the output signal) of the charge packet sense amplifier as a function of metering well voltage. The slope of this transfer characteristic \( \frac{dV_{\text{OUT}}}{dV_{\text{MW}}} \) is 0.90. The transcapacitance is simply calculated from the ratio of the two above slopes as

\[
C_{\text{OUT}} = \frac{dQ_{\text{SIG}}/dV_{\text{MW}}}{dV_{\text{OUT}}/dV_{\text{MW}}} \tag{5.4-6}
\]

and has a value of 37.7 pC/volt for device 7B6.

Combining the amplifier gain measurement and transcapacitance measurement yields an inferred lumped output MOSFET gate capacitance (using Eq. 5.4-2) of 46.5 pF. This can be compared to a predicted value of 43 pF as computed in appendix D using the fabricated characteristics of wafer 7B. The results are reassuringly close.

Charge Packet Replicator

The charge-packet initiated MTOS junction switching experiments' parallel channel was again utilized to test the charge packet replicator mode of operation of the charge packet differencer experiment. The parallel channel was clocked to perform charge packet formation using the fill and spill technique with the input transfer gate biased at -4.00 volts. The output signal was measured as a function of metering well voltage \( V_{\text{MW}} \) as shown for device 7B6 in Fig. 5.4-3. The non-zero value of the output signal for no charge packet \( (V_{\text{MW}} \) smaller than -4.0 volts) is due to a combination of non-ideal behavior including amplifier droop and dark current collected during the output transfer phase. The slope of the transfer characteristic is 0.87, which when multiplied by the output transcapacitance indicates that input charge packet size is 33 pC per metering well volt.

The charge packet differencer operating in a replicator mode was also
Device 7B6

\[ R_L = 500k\Omega \]

\[ \delta t = 50\mu \text{sec} \]

\[ V_{X1} = -4.0\text{VOLTS} \]

**Parallel Channel**

**\[ V_{WB} = -4.0\text{volts} \]**

**\[ V_{WB} = -6.0\text{volts} \]**

5.4-3 Charge packet replicator operation compared to parallel channel input as discussed in text.
measured on device 7B6. In this mode, \( V_{WB} \) was set equal to the input transfer gate bias which was equal to \(-4.0 \) volts. The A input channel metering well bias was ramped from zero to \(-10.0 \) volts and the created charge packet was fed into the differenter. The output signal from the differenter was measured as a function of \( V_{WA} \) as shown in Fig. 5.4-3. Again, a similar non-zero output signal is seen for \( V_{WA} \) smaller than \(-4.0 \) volts, which is attributed to the non-ideal behavior discussed previously but amplified due to the longer overall cycle time of the differencing operation. The slope of the transfer characteristic indicates that the differenter is producing 27 pC per A channel metering well volt. From the previous measurement, the replicator ideally would be producing 33 pC per metering well volt so that differenter has a gain (i.e. attenuation factor) of 0.82.

This attenuation factor can be explained by invoking the stray capacitance effect discussed in section 5.2, as exemplified by Eq. 5.2-23. To estimate the stray capacitance we add the three major components. First, the underlap capacitance between the floating \( p^+ \) diffusions and adjacent electrodes contributes a capacitance of 0.38 pF/mils\(^2\) multiplied by 7 mils\(^2\) or 2.7 pF. The floating \( p^+ \) diffusion capacitance (to substrate) was calculated in appendix D and estimated to be approximately 60 fF/mils\(^2\) yielding 2.2 pF. Finally, the stray wiring capacitance is dominated by where the wire crosses the channel stop diffusion over gate oxide which has a capacitance of 0.38 pF/mils\(^2\) multiplied by 4 mils\(^2\) or 1.5 pF. The total stray capacitance is 6.4 pF.

The effective oxide capacitance of the differenter electrode is 45 pF. Using Eq. 5.3-9, the predicted attenuation factor is 0.87. The agreement between the experimentally observed attenuation factor and this predicted value is reasonable, but the difference indicates that the stray capacitance may be larger than actually calculated.
When the B input channel is used, the device is no longer operating in the replicator mode, but it is convenient to discuss the effect briefly. Applying $V_{WB} = -6.00$ volt results in the formation of a two volt bucket and charge packet of 66 pC. Using Eq. 5.2-23 and the output transcapacitance, the output signal should be reduced by 1.45 volts. In Fig. 5.4-3, the results of this measurement are shown and it can be seen that indeed the transfer characteristic is shifted down by the predicted amount indicating proper operation of the differencer circuit. Note that the knee of the transfer characteristic is shifted two volts to the right but the 'zero' level is unaffected. Finally, as a preview to an upcoming sub-section, observe that the output saturates for approximately a four volt A channel input bucket independently of the B channel input bucket size.

**Charge Packet Differencer Diagnostic Procedure**

Prior to discussing the results of testing a fully functional charge packet differencer, it is useful to discuss the techniques developed to diagnose modes of differencer failure. The procedure outlined below can also serve as a vehicle for fine tuning the circuit. The overall plan is to work backwards beginning from the output amplifier and heading towards the input circuits.

1. **Amplifier source-follower test**
   a. Apply -20 volt bias to $V_{DA}$
   b. Apply -25 volt bias to $V_{PCA}$
   c. Apply -20 volt bias to $V_{OA}$

In the course of applying this latter bias, the output voltage $V_{OUT}$ (measured across a suitable resistor) should follow and track $V_{OA}$ once $V_{OA}$ exceeds $V_T$ (see Fig. 5.4-1).

   d. Operate $V_{PCA}$ in a pulse mode (0, -25 volts)

Output amplifier should exhibit reset clock feedthrough effects and perhaps droop. Droop should not exceed 10-20 mV/µsec.

   e. Turn off $V_{PCA}$ (zero volts)
Output voltage should gradually return to zero, depending upon droop rate.

f. Return V_{PCA} to normal pulse mode operation

2. Differencer potential well test

a. Apply $-25$ volt bias to $V_{PCS}$
b. Apply $-20$ volt bias to $V_0$
c. Apply $-4$ volt bias to $V_{X2}$
d. Apply pulse to $V_{X0}$ ($0, -25$ volts)
e. Apply pulse to $V_{D2}$ ($0, -25$ volts)

Output amplifier should display large (possibly saturated) response. Reducing $V_0$ should reduce output signal which should go to zero when $V_0$ is smaller than $V_{X2}$.

f. Apply $-20$ volt bias to $V_0$
g. Apply pulse to $V_{PCS}$ ($0, -25$ volts)

Output amplifier should display large (possibly saturated) response, but not as large as when $V_{PCS}$ was held 'on'. Reducing $V_0$ should reduce output signal which should go to zero when $V_0$ is smaller than $V_{X2}$.

h. Apply $-20$ volt bias to $V_0$

Check that increasing $V_{X2}$ decreases the output signal which should go to zero when $V_{X2}$ is increased to $-20$ volts.

i. Apply $-20$ volt bias to $V_{X2}$

3. Replicator mode test

a. Apply $-4$ volt bias to $V_{X1}$
b. Apply $-7$ volt bias to $V_{WA}$
c. Apply pulse to $V_{XAB}$ ($0, -25$ volts)
d. Apply pulse to $V_{D1}$ ($0, -25$ volts)

Output amplifier should display an output signal. Increasing $V_{WA}$ should increase output signal. Decreasing $V_{WA}$ below $V_{X1}$ should result in output signal decreasing to zero.

e. Apply $-6$ volt bias to $V_{XA}$

Increasing $V_{X1}$ should cause output signal to decrease which should go to zero when $V_{X1}$ is equal to $V_{WA}$.

f. Apply $-4$ volt bias to $V_{X1}$

4. Differencer Test
Increasing $V_{WB}$ from $-4$ volts to $-6$ volts should cause decreasing output signal which should go to zero when $V_{WB}$ is equal to $-6$ volts. Increasing $V_{WA}$ should increase output signal which should be cancelled by an equal increase in $V_{WB}$.

5. Fine Tuning

a. Apply $-4$ volt bias to $V_{WB}$
b. Apply low frequency triangular wave to $V_{WA}$
   ($-4$ to $-8$ volts)

Oscilloscope display of output synchronized by triangular wave should show a reasonably linear transfer characteristic. Increasing $V_{WB}$ should uniformly decrease envelope (see Fig. 5.4–3). Adjust cycle time, all dc biases, clocked biases' high and low levels, and transition rates until performance is optimized with respect to linearity, dynamic range, zero standoff, clock feedthrough and transfer efficiency.

This last instruction is deliberately vague. Tuning a CCD circuit is an acquired skill which appears to be a black magic art to the inexperienced. This simple differencer experiment can be considered to be a black box with 14 control inputs and one output, the latter of which must be optimized through the 36 parameters which characterize the 14 inputs. The challenge of tuning the circuit is compounded because there are many local optima in parameter space. Only by considering the device physics of the internal workings of the black box (grey box), can one hope to achieve the global optimum in a finite period of time.

Charge Packet Differencer Performance Verification

The charge packet differencer creates a charge packet $Q_O$ equal to the difference of two input charge packets $Q_{SA}$ and $Q_{SB}$ according to

$$Q_O = [Q_{SA} - Q_{SB}]$$  \hspace{1cm} 5.4-7

For the Yale 8205 experimental structure, the input charge packets are proportional to the input channel metering well voltages $V_{WA}$ and $V_{WB}$ such that
\[-g_{SA} = C_{OX} (V_{WA} - V_{X1}) \hspace{1cm} 5.4-8a\]
\[-g_{SB} = C_{OX} (V_{WB} - V_{X1}) \hspace{1cm} 5.4-8b\]

The output transconductance relates the output charge packet to the output signal according to

\[\Delta V_{OUT} = g_{O}/C_{OUT} \hspace{1cm} 5.4-9\]

Combining these equations and including the stray capacitance yields the relationship between input channel metering well voltages and output signal,

\[\Delta V_{OUT} = g_{SC} \frac{C_{OX}}{C_{OUT}} (V_{WA} - V_{WB}) \hspace{1cm} 5.4-10\]

where the effect of stray capacitance has been included. This last equation is valid for \(V_{WA}\) and \(V_{WB}\) larger than \(V_{X1}\), and \(V_{WA}\) larger than \(V_{WB}\). The output signal should be zero otherwise. A plot of the predicted performance of the device using the parameter values determined previously is shown in Fig. 5.4-4. The plot shows a planar surface which intersects the ordinate axes plane along the line \(V_{WA} = V_{WB}\).

The semi-empirical predicted performance may be compared to a plot showing the measured transfer characteristics of device 7B20, which is shown in Fig. 5.4-5. The applied biases are summarized in Table 5.4-1. In Fig. 5.4-5, the output signal is referenced to the case when \(V_{X1}\), \(V_{WA}\) and \(V_{WB}\) are biased at -4.0 volts. The output signal appears to be negative when \(V_{WB}\) is biased above \(V_{WA}\). This is because increasing \(V_{WB}\) helps suppress dark current collected under the B channel differencer electrode through \(g_{SB}\) and the reduced effective electrode bias.

In the active region of the transfer characteristic we can define the
5.4-4 Ideal performance transfer characteristics of differencer circuit. Output gain calculated using experimentally observed values.
5.4-5 Transfer characteristic surface of experimental charge packet differenter circuit. Output signal referenced to reset level shifted by 0.8 volts.
<table>
<thead>
<tr>
<th>Device</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental clock period ( \delta t )</td>
<td>50 ( \mu \text{sec} )</td>
</tr>
<tr>
<td>Output MOSFET load resistance ( R_L )</td>
<td>500 k( \Omega )</td>
</tr>
<tr>
<td>Output MOSFET drain bias ( V_{DA} )</td>
<td>-20 volts</td>
</tr>
<tr>
<td>Output MOSFET precharged gate bias ( V_{OA} )</td>
<td>-20 volts</td>
</tr>
<tr>
<td>Precharge MOSFET pulse (amplifier) ( V_{PCA} )</td>
<td>0, -25 volts</td>
</tr>
<tr>
<td>Differencer precharge bias ( V_O )</td>
<td>-20 volts</td>
</tr>
<tr>
<td>Precharge MOSFET pulse (differencer) ( V_{PCS} )</td>
<td>0, -25 volts</td>
</tr>
<tr>
<td>Input isolation gate bias ( V_{X2} )</td>
<td>-20 volts</td>
</tr>
<tr>
<td>Input diode pulse (differencer) ( V_{D2} )</td>
<td>-25, 0 volts</td>
</tr>
<tr>
<td>Output transfer gate pulse (differencer) ( V_{XO} )</td>
<td>0, -25 volts</td>
</tr>
<tr>
<td>Input diode pulse (input stage) ( V_{D1} )</td>
<td>-25, 0 volts</td>
</tr>
<tr>
<td>Input transfer gate bias ( V_{X1} )</td>
<td>-4 volts</td>
</tr>
<tr>
<td>Output transfer gate pulse (input stage) ( V_{XAB} )</td>
<td>0, -25 volts</td>
</tr>
</tbody>
</table>
differencer output gains $a_{DA}$ and $a_{DB}$ as

$$a_{DA} = \frac{\partial V_{OUT}}{\partial V_{WA}} \bigg|_{V_{WB}}$$  \hspace{1cm} 5.4-11a

and

$$a_{DB} = \frac{\partial V_{OUT}}{\partial V_{WB}} \bigg|_{V_{WA}}$$  \hspace{1cm} 5.4-11b

which according to Eq. 5.4-10 should be equal to each other and

$$a_{DA} = a_{DB} = a_{SC} \frac{C_{OX}}{C_{OUT}}$$  \hspace{1cm} 5.4-12

which is equal to 0.91 using the parameters evaluated for device 7B6. For device 7B20, the gains are $a_{DA} = 0.89$ and $a_{DB} = 0.86$ depending slightly on the operating region in which they are evaluated. The difference between the 7B6 predicted gains and the 7B20 observed gains is insignificant and it is concluded that the device is operating properly.

The transfer characteristic indicates that the differencer saturates for an A channel bucket larger than approximately 5 volts. From device 7B6, this corresponds to 165 pC. Using Eq. 5.2-13, the maximum charge packet prior to saturation is 162 pC so that the agreement, although somewhat fortuitous, validates the understanding of the saturation mechanism.

The transfer characteristic of Fig. 5.4-5 demonstrates the successful implementation of the charge packet differencing concept introduced in this chapter. This transfer characteristic will be revisited in the discussion of device linearity in the next subsection.

In Figs. 5.4-6a and 5.4-6b, multiple exposure photographs showing the raw output signal from the differencer are displayed. In the first
5.4-6 Multiple exposure photographs showing actual output of charge packet differencer circuit as sensed by output amplifier.

a. Output as a function of channel A input charge packet. $V_{WA}$ ramped from $-8.5$ volts to $-3.5$ volts left to right. $V_{WB}$ stepped from $-5.0$ volts to $-8.0$ volts in $-0.5$ volt increments beginning from maximum response.

b. Output as a function of channel B input charge packet. $V_{WB}$ ramped from $-3.5$ volts to $-8.5$ volts left to right. $V_{WA}$ stepped from $-8.0$ volts to $-5.0$ volts in $0.5$ volt increments beginning from maximum response.
(a) DEVICE 7B20 $R_L=500\,\text{k}\Omega$

$V_{X1}= -4.0\text{VOLTS}$

$V_{OUT} 0.5\text{V/DIV}$

$V_{WA} 0.5\text{V/DIV}$

$V_{WB} 0.5\text{V/STEP}$

2msec/DIV →

(b) DEVICE 7B20 $R_L=500\,\text{k}\Omega$

$V_{X1}= -4.0\text{VOLTS}$

$V_{OUT} 0.5\text{V/DIV}$

$V_{WA} 0.5\text{V/DIV}$

$V_{WB} 0.5\text{V/STEP}$

2msec/DIV →
5.4-7 Transfer characteristic surface of experimental charge packet differencer. Output signal referenced to reset level shifted by 0.6 volts.
photograph, $V_{WA}$ (solid trace) is slowly increased from $-3.5$ volts to $-8.5$ volts from left to right while $V_{WB}$ is kept at constant value. The output signal (which appears as a short dash in these photographs) increases as $V_{WA}$ increases, and decreases as $V_{WB}$ is stepped from $-5.0$ volts to $-8.0$ volts in $0.5$ increments.

In the second photograph, $V_{WB}$ (solid trace) is slowly increased from $-3.5$ volts to $-8.5$ volts from left to right as $V_{WA}$ is kept constant. The output signal decreases with increasing $V_{WB}$ and increases as $V_{WA}$ is stepped from $-5.0$ volts to $-8.0$ volts. This second photo is quite similar to Fig. 5.4–5 except that the viewing angle is perpendicular to the $V_{WB}$ axis.

In Fig. 5.4–7, the successful operation of part 9A11 is shown. As expected, this device shows many of the same features as device 7B20 (Fig. 5.4–5) and its behavior is not analyzed here. Since it was fabricated using a slightly different process from that employed during the manufacturing of device 7B20, its operating characteristics are expected to be somewhat different. This is partially exhibited by the lower gain observed in the transfer characteristic of part 9A11.

**Linearity**

The linearity of the transfer characteristic shown in Fig. 5.4–5 is quite good except close to the bias conditions $V_{WA} = V_{X1}$, $V_{WB} = V_{X1}$, and $V_{WA} = V_{WB}$, where the transfer characteristic is slightly rounded. This distortion is introduced by the fill and spill operation for shallow capture wells. For example, a similar distortion is observed in Fig. 5.4–3 where the MTOS experiments' parallel channel was used to create a charge packet using the fill and spill technique. Ideally, the fill and spill technique should result in a sharp slope discontinuity at $V_{MW} = V_{X1}$. Instead, the large geometry circuit implemented on the Yale 8205
chip produces a rounded knee transfer characteristic. The rounding is probably due to charge transfer inefficiency during the spill phase. A small charge packet is effectively captured due to the slow spill process even though it is energetically favorable for that charge to be spilled out the input diode. Such rounding effects are expected to be reduced for smaller geometry devices.

Charge transfer inefficiency during the spill phase of the input circuit is responsible for the distortion near $V_{WB} = V_{XI}$ and $V_{WA} = V_{XI}$ in the 7B20 transfer characteristics. Charge transfer inefficiency during the spill phase of the differencer circuit is responsible for linearity distortion near $V_{WB} = V_{WA}$.

In characterizing the differencer linearity, four cases are considered. The linearity is measured over two different operating ranges. One is the full operating range which includes the rounding effects discussed above. The second is a reduced range which does not include the rounding effects. The linearity is thus measured for a constant value of $V_{WA}$ over two operating ranges of $V_{WB}$, and for a constant value of $V_{WB}$ over two operating ranges of $V_{WA}$.

To quantify the non-linearity, a method introduced by Epsley (1933) as described by Millman and Kalkias (1972) is used. The technique is to partition the operating range into four equal sections in the input parameter ($V_{WA}$ or $V_{WB}$). The four sections are defined by five metering well voltages which are labelled $X_L$, $X_{LM}$, $X_M$, $X_{MH}$ and $X_H$ in order from lowest to highest. Each input voltage is associated with an output voltage ($Y_L$, $Y_{LM}$, $Y_M$, $Y_{MH}$, $Y_H$). For the constant $V_{WA}$ case (-8.0 volts), the partitioned transfer characteristic is displayed in Fig. 5.4-8. Partitioning for both the full interval and the sub interval is shown.

In the method of Epsley, it is assumed that an input sine wave is
5.4-8 Partitioning of actual transfer characteristic for non-linearity characterization. See text.
applied to the circuit and a distorted sine wave is output. The
distorted output signal is assumed to contain the five Fourier
components $B_0$, $B_1$, $B_2$, $B_3$ and $B_4$ in order of increasing frequency.
These five component amplitudes are determined from the transfer
characteristic in terms of the five output voltages according to the
following relationships:

\[
\begin{align*}
B_0 &= \frac{1}{6} (Y_H + 2Y_{MH} + 2Y_{LM} + Y_L) - Y_M \\
B_1 &= \frac{1}{3} (Y_H + Y_{MH} - Y_{LM} - Y_L) \\
B_2 &= \frac{1}{4} (Y_H - 2Y_M + Y_L) \\
B_3 &= \frac{1}{6} (Y_H - 2Y_{MH} + 2Y_{LM} - Y_L) \\
B_4 &= \frac{1}{12} (Y_H - 4Y_{MH} + 6Y_M - 4Y_{LM} + Y_L)
\end{align*}
\]

The harmonic distortion is defined for each component as

\[
\begin{align*}
D_2 &= \left| \frac{B_2}{B_1} \right| \\
D_3 &= \left| \frac{B_3}{B_1} \right| \\
D_4 &= \left| \frac{B_4}{B_1} \right|
\end{align*}
\]

The total distortion is defined as

\[
D_T = (D_2^2 + D_3^2 + D_4^2)^{1/2}
\]

For device 7B20, the four cases considered were

1. $V_{WA} = -8.0$ volts, $V_{WB} = -4.0$ to $-8.0$ volts
2. $V_{WA} = -8.0$ volts, $V_{WB} = -5.0$ to $-7.0$ volts
3. $V_{WB} = -5.0$ volts, $V_{WA} = -4.0$ to $-8.0$ volts
4. $V_{WB} = -5.0$ volts, $V_{WA} = -6.0$ to $-8.0$ volts

In case 1, distortion is expected due to the rounding effects
discussed above. In case 3, the same distortion is expected with
additional distortion due to saturation effects. The results of these
Table 5.4-2
Linearity Distortion

<table>
<thead>
<tr>
<th>Case</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y_H</td>
<td>6.70</td>
<td>5.35</td>
<td>6.38</td>
<td>5.37</td>
</tr>
<tr>
<td>Y_{MH}</td>
<td>5.35</td>
<td>4.50</td>
<td>5.37</td>
<td>4.52</td>
</tr>
<tr>
<td>Y_H</td>
<td>3.63</td>
<td>3.63</td>
<td>3.68</td>
<td>3.68</td>
</tr>
<tr>
<td>Y_{LM}</td>
<td>1.85</td>
<td>2.75</td>
<td>1.93</td>
<td>2.81</td>
</tr>
<tr>
<td>Y_L</td>
<td>0.20</td>
<td>1.85</td>
<td>0.19</td>
<td>1.93</td>
</tr>
<tr>
<td>B_0</td>
<td>-0.08</td>
<td>-0.013</td>
<td>-0.15</td>
<td>-0.02</td>
</tr>
<tr>
<td>B_1</td>
<td>3.33</td>
<td>1.75</td>
<td>3.21</td>
<td>1.71</td>
</tr>
<tr>
<td>B_2</td>
<td>0.09</td>
<td>0.015</td>
<td>-0.02</td>
<td>-0.015</td>
</tr>
<tr>
<td>B_3</td>
<td>0.08</td>
<td>0.000</td>
<td>-0.115</td>
<td>0.0033</td>
</tr>
<tr>
<td>B_4</td>
<td>-0.01</td>
<td>-0.0016</td>
<td>-0.05</td>
<td>0.005</td>
</tr>
<tr>
<td>D_2</td>
<td>0.027</td>
<td>0.0085</td>
<td>0.062</td>
<td>0.0087</td>
</tr>
<tr>
<td>D_2 (dB)</td>
<td>-31dB</td>
<td>-41dB</td>
<td>-24dB</td>
<td>-41dB</td>
</tr>
<tr>
<td>D_3</td>
<td>0.025</td>
<td>0.0000</td>
<td>0.036</td>
<td>0.0019</td>
</tr>
<tr>
<td>D_3 (dB)</td>
<td>-32dB</td>
<td>-</td>
<td>-29dB</td>
<td>-54dB</td>
</tr>
<tr>
<td>D_4</td>
<td>0.003</td>
<td>0.0009</td>
<td>0.015</td>
<td>0.0029</td>
</tr>
<tr>
<td>D_4 (dB)</td>
<td>-50dB</td>
<td>-61dB</td>
<td>-36dB</td>
<td>-51dB</td>
</tr>
<tr>
<td>D_T</td>
<td>0.037</td>
<td>0.0086</td>
<td>0.073</td>
<td>0.0094</td>
</tr>
<tr>
<td>D_T (dB)</td>
<td>-29dB</td>
<td>-41dB</td>
<td>-23dB</td>
<td>-41dB</td>
</tr>
</tbody>
</table>
measurements and calculations are displayed in Table 5.4-2. For the first case, the total distortion is $-28 \text{ dB (} 20 \log_{10} D_{T} \text{)}$ and for the third case, the distortion level was increased to $-23 \text{ dB}$. However, in the sub internal operating ranges, the distortion was much less and measured to be $-41 \text{ dB}$ for each case.

**Noise and Dynamic Range**

The noise of part 7B20 was examined by displaying the output signal during actual operation on an oscilloscope. Although such a method does not reveal the spectral properties of the noise nor does it provide an accurate determination of the RMS noise value, it does yield an upper bound on the magnitude of the noise. From such an examination, the noise envelope was found to have a maximum value of 1 millivolt in width, with a 60 Hz envelope of 2 mV.

The observed noise level is most likely due to the experimental set-up which was designed to reduce noise levels to the millivolt range. For measuring noise levels in the microvolt range in such a complex test station, special elaborate precautions must be taken which were not observed in this work since noise levels were not a fundamental issue. The noise was examined to place a lower bound on the dynamic range of the fabricated devices.

A millivolt noise signal corresponds to a 37 fC equivalent noise charge packet. The observed saturation level was 165 pC so that the dynamic range, which is the ratio of these charge packets is over 4400, corresponding to 73 dB for a signal to noise ratio (SNR) of unity. The practical dynamic range might be defined for an SNR of 10, or 53 dB.

To compare this figure to the range expected were test station noise removed, various noise sources are estimated following Carnes and Kosonocky (1972) and Barbe (1975). The noise is calculated in terms of
an RMS number of carriers and converted to output signal by multiplying by \( q / C_{\text{OUT}} \). First, at the input, the noise introduced by the A and B input channels is given by

\[
\overline{v}_{\text{IN}} = (kT C_{\text{MW}})^{1/2} / C_{\text{OUT}}
\]

which is of the order of 10 \( \mu \)V each. The differencer itself also has a fill and spill noise of the same size. Dark current (which is zero-standoff signal) contributes a noise which is approximately equal to the square root of the zero-standoff voltage equivalent number of carriers (assuming a Poisson distributed generation rate). For part 7B20, which has a zero-standoff signal of 0.8 volts, this yields approximately 60 \( \mu \)V.

Interface trapping noise is given by

\[
\overline{v}_{\text{IT}} = q(1.4 k T D_{\text{it}} A_E)^{1/2} / C_{\text{OUT}}
\]

where \( A_E \) is the total electrode area in the circuit and \( D_{\text{it}} \) is the active interface trap density. Assuming \( D_{\text{it}} = 1 \times 10^{10} \text{ (cm}^2 \text{- eV)}^{-1} \), the noise is 5 \( \mu \)V. Another source of noise during charge transfer is charge transfer inefficiency noise. This noise is given by

\[
\overline{v}_{\text{CTI}} = q \left[ \frac{2 e n_T \bar{N}}{N} \right]^{1/2} / C_{\text{OUT}}
\]

where \( s \) is the fractional loss per transfer, \( n_T \) is the number of transfers, and \( \bar{N} \) is the average number of carriers. Using a modest value of \( s = 0.05 \) yields approximately 60 \( \mu \)V.

The output amplifier reset noise during the precharge phase is

\begin{equation}
\bar{v}_R = \left(\frac{kT}{C_{\text{OUT}}}\right)^{1/2}
\end{equation}

which is of the order of 10 \(\mu\text{V}\). The Johnson noise from the large load resistance is

\begin{equation}
\bar{v}_J = \left(4kT R_{\text{LAB}}\right)^{1/2}
\end{equation}

The bandwidth is determined by the 25 pF oscilloscope input capacitance yielding a noise level of 25 \(\mu\text{V}\).

The total noise expected for this CCD circuit is therefore

\begin{equation}
\bar{v}_T = \left(3\bar{v}_{\text{IN}}^2 + \bar{v}_{\text{TH}}^2 + \bar{v}_{\text{IT}}^2 + \bar{v}_{\text{CTI}}^2 + \bar{v}_R^2 + \bar{v}_J^2\right)^{1/2}
\end{equation}

which is approximately 90 \(\mu\text{V}\), or a noise equivalent charge packet of 3.4 fC. The projected maximum dynamic range for an SNR of 1 for this device is given by the ratio of the maximum saturation charge packet of 186 pC to the noise equivalent charge packet which is \(5.5 \times 10^4\) or 81 dB.

**Operating Speed**

The effect of varying the fundamental clock period \(\delta t\) from 1000 \(\mu\text{sec}\) down to 5 \(\mu\text{sec}\) is shown in Fig. 5.4-9. In this experiment, the A channel input charge packet is kept constant \((V_{\text{WA}} = -8.0 \text{ volts})\) and the B channel charge packet size is slowly ramped \((V_{\text{WB}} = 0 \text{ to } -10 \text{ volts})\). The input transfer gate \(V_{X1}\) was biased at -4.0 volts and the other d.c. and clocked biases were as in Table 5.4-1.

The effect of varying the operating speed can be divided into two major consequences. For slow speeds (fundamental clock periods longer than 100 \(\mu\text{sec}\)), the consequence is increased dark current and amplifier droop resulting in a significant zero-standoff signal. However, the slope of the transfer characteristic is not affected. For clock periods shorter than 50 \(\mu\text{sec}\), charge transfer inefficiency degrades the gain of
Output of charge packet difference circuit as a function of B channel input for various values of fundamental clock period $\delta t$. 

DEVICE 7B20
$R_L=500k\Omega$
$V_X1=-4.0VOLTS$
$V_{WA}=-8.0VOLTS$
the transfer characteristic. At a clock period of 5 \( \mu \)sec, the transfer characteristic is nearly flat. Using a fundamental clock period of 50 \( \mu \)sec, it takes 300 \( \mu \)sec to complete one full differencing operation and to transfer the output charge packet into subsequent circuitry.

**Multiple Cycle Operation**

If the timing of the circuit is appended (see Fig. 5.2-2), it is possible to re-generate the output charge packet several times without repeating the gate charge subtraction operation. In this multiple cycle mode, a fill and spill operation is performed subsequent to the transfer of the output charge packet, and a copy of the output charge packet is re-generated.

To measure the effectiveness of this multiple cycle mode, the 7B20 device was biased for replicator mode operation with the re-generation timing cycles appended. The fundamental clock period was 62 \( \mu \)sec and the interval between each charge packet formation was one millisecond. During each cycle, the output amplifier was reset to its precharged state. The output signal is shown as a function of input charge packet size \( (V_{\text{WA}}) \) for six copy cycles in Fig. 5.4-10.

The overall behavior indicates that the differencer is indeed capable of re-generating output charge packets over multiple cycles. The slope of the transfer characteristic changes slightly from the initial cycle to the copy cycles, but remains nearly constant during the latter. The linearity appears to improve during the re-generation cycles, though the absolute size of the output signal progressively decreases. Most of these effects can be interpreted in terms of PN junction leakage current discussed in section 5.2, and exemplified by Eq. 5.2-27. During the replicator mode operation, the B electrode effective voltage may be significantly larger than the A electrode effective voltage, leading to
5.4-10 Output of charge packet differencer circuit as a function of
A channel input for sequential regeneration cycles.
Re-generation cycle time was one millisecond.
decreased output charge packets with increasing time.

When $V_{WA}$ is larger than $-7.0$ volts, the effective A electrode voltage is small enough to result in charge transfer inefficiency during the fill phase. As a result, the output charge packet size dramatically drops. To explain why it does not drop to the zero-standoff voltage level is more troublesome, but a plausible explanation is that soft silicon breakdown in the B channel well is occurring, which tends to fill that potential well independently of the input diode. Such a soft breakdown hypothesis is consistent with the large zero-standoff charge packets observed during the output transfer phase.

5.5 Discussion

Accuracy Error

In chapter two the desired features of the charge packet differencer circuit were discussed. The key feature in an analog processing system is that accuracy be maintained. Within that context, it was proposed that an analog computational building block should have an eight bit equivalent accuracy, i.e., that the error be no larger than one part in 256, or $-48$ dB.

In the previous section, the fabricated devices were characterized in terms of linearity, gain, noise, and offset dynamic range. Each of these characteristics contributes to the total error accrued in one operation. For the fabricated devices, the equivalent observed noise in these circuits (0.04 pC) might suggest that a minimum resolvable charge packet (MCRP) size of 0.50 pC for an SNR of 12.5 be chosen. For a dynamic range of 256:1, the maximum charge packet which the differencer must need to handle is 128 pC, well below the experimentally observed saturation level of 165 pC.
The linearity distortion contributes to the accuracy error. For example, if the best fitting straight line is chosen through the five measured points of the first case listed in Table 5.4-2, the slope is 0.825. At the point where the actual transfer characteristic deviates the most from this best fitting line, the corresponding error is 6.5 pC. For the second case of Table 5.4-2, the slope is 0.88 and the maximum error in this subinterval corresponds to 0.68 pC. These non-linearity errors should be compared to the MRCP size of 0.50 pC. Thus, the subinterval non-linearity error is almost tolerable in these large geometry devices.

The non-linearity error is calculated assuming that the slope itself is acceptable. However, non-unity gain caused by stray capacitance is the largest contributor to absolute computational error in the circuit. The maximum error occurs during the replication of a large charge packet. For example, with a stray capacitance attenuation factor of 0.89, replicating a 128 pC charge packet results in an error of 14 pC. To achieve a maximum error smaller than the MRCP, the stray capacitance attenuation factor must be better than 1-1/256 or 0.996. This implies that the stray capacitance must be less than 0.40 percent of the differencer oxide capacitance.

As observed at the output of the charge packet sense amplifier, the zero-standoff voltage also appears as a fixed large offset error. However, most of this error is generated in the course of transferring the charge packet out of the differencer and amplifying it. Therefore, it is not considered as an error in the differencer itself, even though it represents a nuisance.

The improved layout proposed in Fig. 5.3-3 will assist in decreasing the non-linearity error due to charge transfer inefficiency rounding.
effects, and partially reduce stray capacitance, especially if the
gate is omitted. However, even with the gate omitted, the
stray capacitance will be two percent of the electrode oxide capacitance
which is five times too large. The major effect of the improved layout
will be to increase the speed of the circuit, which in turn will
alleviate the detractive effects of the dark current and PN junction
leakage current.

Operating Speed

As was just discussed, the proposed improved layout will increase the
speed of the circuit from its present value of 300 μsec/operation (3.3
kops) by perhaps one or two orders of magnitude (∼0.1 mops). This is
due to the present speed limitation being diffusion limited charge
transfer which scales as $L^2$.

For a charge-coupled computer, the operating speed should be of the
order of one million operations per second (1 mop). A major increase in
speed comes about if the charge transfer in the channel is due to
fringing fields rather diffusion. Such effects dominate in channel
lengths under 10 μm which are not practically obtainable at the present
time in the Yale facility.

Effects of Scaling and Process Improvement

It is expected that if a suitable processing facility were available,
devices meeting the charge-coupled computer's requirements could be
realistically manufactured. By decreasing the CCD device geometry to
levels comparable to present day commercial devices (for example: $W =
50 \mu m, L = 10 \mu m$) the device speed could easily reach the 1 mops range.
The area of such a scaled device is 200 times smaller than the improved
layout of Fig. 5.4-3. Thus the noise level in the circuit becomes much
more critical, even though the noise equivalent charge packet size
scales with the saturation level charge packet. However, the author's experience is that the charge-coupled computer's noise requirement (3000 RMS noise carriers) is comparable to present day CCD noise levels.

With the transfer efficiencies expected for such a small geometry device (better than 0.999), the linearity error associated with charge transfer inefficiency is expected to be minimal. The attenuating effects of stray capacitance can be improved by using a self-aligned polysilicon gate technology, though wiring capacitance may become more pronounced in system configurations. Any error though could be kept below the MRPC by careful layout and process design.

5.6 Summary and Conclusions

This chapter began with a discussion of the basic theory of operation of the charge packet differencer circuit. To the best knowledge of the author, and confirmed by a patent novelty search, the differencer circuit is unique in its operation and compactness, and offers distinct advantages over present charge packet differencing techniques. Aside from compactness, the advantages of the circuit are inherent linearity and communication over structures in the silicon substrate. The speed of this new circuit is projected to be comparable to present CCD differencing circuits with accuracy unsurpassed by devices occupying significantly more real estate.

In addition to the basic theory, non-ideal behavior was also discussed such as the attenuating effects of stray capacitance. Also covered was the detractive effects of PN junction leakage current and bucket dark current.

The layout of an experimental realization of the proposed differencer circuit which was fabricated at Yale was presented. The layout was critiqued using hindsight and an improved layout suitable for
fabrication without process alteration was described.

The experimental devices fabricated at Yale were measured and characterized. Although the relatively large geometries employed in the Yale process due to the limited facilities were a priori acknowledged to yield less than optimal performance, the fabricated devices functioned well. The major source of accuracy error was due to stray capacitance, though the effects of charge transfer inefficiency, dark current and PN junction leakage current also contributed to the total error. By applying the theory presented early in the chapter, the inaccuracies described above were quantitatively analyzed and found to conform to expectations in a self-consistent way.

Finally, the actual device performance and projected performance in consideration of scaling and process improvement were compared to the requirements of the charge-coupled computer as discussed in chapter two. The experimental devices have well demonstrated the feasibility of performing charge packet differencing using the proposed CCD circuit.