CHAPTER 3

FABRICATION OF PROTOTYPE CIRCUITS

3.1 Introduction

The fabrication of charge-coupled devices requires stringent control over semiconductor processing quality. Semiconductor defects, impurities, and surface traps can dramatically alter the performance characteristics of CCDs. Dark current, originating from bulk and surface traps shortens the storage time of deep depleted MOS capacitors. Bulk traps also contribute to the reverse leakage current of PN junctions. Surface traps can lead to charge transfer inefficiency and reduced dynamic range.

The processing of semiconductor devices at Yale has historically been limited to MOS capacitors and occasionally MOSFETs with the primary emphasis on (tunnel) oxide and interface properties rather than on semiconductor quality. [Low temperature, long channel MOSFET research excepted]. There has also been no work on the charge-coupling of MOS devices. To successfully couple two deep depleted MOS capacitors, the capacitor electrode spacing must be less than a few microns, depending upon the oxide thickness. The charge transfer efficiency degrades rapidly with increasing spacing. Thus the fabrication challenge was to improve the standard Yale MOSFET process [Ma, 1984] to reduce dark current and make sub-micron structures in a mil-scale facility.

The major reason why the Yale facility is presently limited to design rules in the one mil range is not because of photolithographic limits (5 microns) or particulate contamination (class 100 air), rather it is due to the inability to make multiple level mask sets which register to an accuracy much better than ± 0.5 mils over the die width. This
registration error source is the rotational error during the frame mounting of 10x reticles.

During the process development, a literature search revealed a particularly elegant method for making sub-micron gaps in the Yale environment. This process worked well and was found to be reliable. It is discussed in detail in the next section. The dark current remained enigmatic for some time primarily because of our own inexperience in dealing with this processing aspect, though it continues to commercially be a topical issue for dynamic memory circuits. The dark current was reduced in the Yale 8205 process through the use of a lower wet oxidation temperature and through the gettering properties of heavily (phosphorous) doped silicon. The tunnel oxide growth process developed by Dressendorfer (1978) and Lai (1979), and employed by Teng (1983) was retained without significant modification. However, due to a plumbing problem in the dry oxidation furnace, the first bistable MTJUS junction grown in air (800 C) may have been inadvertently fabricated. Once corrected, the tunnel oxidation process worked well. A defective dopant source (Borosilica film) which has a short shelf life led to some initially false conclusions regarding the optimization of PN junction leakage current. This too was corrected by changing the dopant source (Borofilm) and the process was brought under control.

On the same die, charge-coupled devices with inter-electrode spacings less than one micron and low dark current, low leakage current PN junctions, and high quality bistable tunnel oxide junctions have been successfully fabricated. As it was once remarked, "It's amazing what one can make with equipment industry discarded ten years ago; imagine what one could do with state-of-the-art equipment ..." [P. Santhanam, private communication].
3.2 Sub-Micron Gap Fabrication

The coupling of MOS capacitors to effect minority carrier charge transfer requires that the electrode spacing be quite small, typically less than a few microns [Amelio, 1972; Suzuki and Yanai, 1974]. As described in a review article by Kosonocky (1974), there have been several fabricated structures which satisfy this requirement. Single level metal electrodes [Amelio et al. 1970] are attractive from a structural simplicity point of view, but have suffered from two problems. First, creation of the gap requires micron scale photolithography followed by etching. Although the former is possible in a modern facility, etching of the gap remains difficult due to wetting problems with wet etches, and oxide/interface damage problems associated with ion milling or reactive ion etching process. Such difficulties were overcome using a shadow evaporation technique [Browne and Perkins, 1976]. However, a stability problem remains for the exposed oxide surface in between the two electrodes. For commercial devices, this latter effect has lead to the development of sealed structures.

For example, a single-level polysilicon gate technology can replace the metal described above [Kim and Snow, 1972]. The polysilicon gates have the advantage of being defined by a subsequent implant process and being passivated by an upper level of oxide. Unfortunately the gap size is still limited by photolithography and the implant process.

The use of two levels of electrodes can reduce the effective gap width to zero if they overlap. The first level might be polysilicon and the second aluminum [Kosonocky and Carnes, 1973; Patrin, 1973]. The drawbacks of this technique are that alternating electrodes have a different oxide capacitance requiring higher clocking voltages so that shorts between overlapping electrodes can completely shut off a channel.
An improved overlapping gate technology employing three levels of polysilicon [Sequin, et al. 1973]. In this technology the primary polysilicon levels are isoplanar, with one electrode built up on one side to be able to overlap the adjacent electrode. An anodized aluminum structure can be used in a similar fashion [Collins, et al. 1974]. The advantage of the aluminum structure is the improved conductivity of the metallic gate, though $\text{Al}_2\text{O}_3$ is not as good an insulator as $\text{SiO}_2$. Other metal–insulator systems have also been investigated [Engeler, et al. 1970].

It was elected to use the Browne and Perkins (1976) method at Yale for several reasons. First, the charge-coupled differencer is best implemented using an isoplanar electrode structure (see chapter 5). Second, the Yale facility does not include a polysilicon deposition system. Third, the photolithographic resolution is limited to the five micron range on a wafer wide basis. Thus, the Browne and Perkins method was ideally suited for our requirements and capabilities.

The basic fabrication technique is illustrated in Figs. 3.2-1 (a–e). In Fig. 3.2-1a, a 3500 Å layer of aluminum has been coated with photoresist. The photoresist has been subsequently patterned by exposure and development in the usual way (see section 3.5). In Fig. 3.2-1b, the aluminum has been overetched resulting in a photoresist overhang. Following the overetch, a second layer of aluminum (2000 Å) is deposited without prior removal of the photoresist as shown in Fig. 3.2-1c. Note that the photoresist overhang shadows the aluminum evaporation resulting in a cavern. In Fig. 3.2-1d, the aluminum which was deposited on the photoresist has been removed using a liftoff process. The liftoff is effected by soaking the wafer in acetone for an hour. Although the liftoff is facilitated through the simultaneous use of ultrasonic agitation, such agitation causes degradation of tunnel
3.2-1 Sub-micron inter-electrode gap formation process.

a. Photoresist patterned
b. Overetch of aluminum results in undercut
c. Second metallization
d. Lift-off removes photoresist and metal cap
e. Final metal patterning complete
oxide durability and was not used in the Yale 8205 process. Following liftoff, the aluminum is patterned to its final form as shown in Fig. 3.2-1e.

In Figs. 3.2-2 (a-c) a series of scanning electron microscope (SEM) pictures are displayed which illustrate the gap formation process. In Fig. 3.2-2a, the photoresist overhang can be seen. Note the one micron size bar at the base of the picture. In Fig. 3.2-2b, the structure has been coated with 2000 Å of aluminum. The cavern formed by the photoresist overhang can be discerned. Finally, in Fig. 3.2-2c, the liftoff process has yielded a clean gap between the two metal electrodes. The gap size is slightly under one micron in this photograph.

The size of the gap depends upon the thickness of the first layer of aluminum and the overetch time. To simplistically model the wet chemical aluminum etch process, it is assumed that the etching proceeds at a fixed rate normal to the aluminum surface. A series of contours depicting this model is sketched in Fig. 3.2-3. To calculate the gap width using Fig. 3.2-3, let $t_d$ be the time it takes to etch the aluminum down to the SiO$_2$ (which is experimentally straight-forward to observe) and let $t_w$ be the total etch time. As measured from the corner of the photoresist, a right triangle is formed by the vertical drop $d$ and the horizontal gap $w$ (assuming the subsequent shadowing process is clean and leaves a sharp shadow under only the photoresist). The hypotenuse $h$ assuming a constant etch rate is

$$h = d^2 + w^2 \quad \text{3.2-1}$$

or

$$h = \left(\frac{d}{t_d}\right) t_w \quad \text{3.2-2}$$

Solving for the total etch time yields
3.2-2 SEM photographs showing gap formation process

a. Photoresist overhang/aluminum undercut
b. Second metallization leaves cavern structure
c. Lift-off leaves clean gap structure (= 1 μm)

(Photographs by R. Wisnieff)
Simple model of etch process profiles
\[ t_w = t_d \left[(w/d)^2 + 1\right]^{1/2} \quad 3.2-3 \]

This equation is a useful experimental predictor if the etch rate is unknown (due to etch temperature fluctuations, for example). If the aluminum thickness \( d \) is measured during the evaporation process, then the total etch time according to the simple model may be determined. For example, suppose \( d = 3500 \) Å and \( w \) was to be one micron. From Eq. 3.2-3 it follows that the total etch time should be three times as long as the time required to etch down to the \( \text{SiO}_2 \).

Unfortunately, this simple model fails to accurately determine the size of the gap. In Fig. 3.2-4, several experimental data points measuring the ratio \( w/d \) as a function of \( t_w/t_d \) are plotted. By rewriting Eqs. 3.2-3,

\[ w/d = [(t_w/t_d)^2 - 1]^{1/2} \quad 3.2-4 \]

This theoretical curve is also plotted in Fig. 3.2-4, indicating the failure of the model to predict the gap size. Indeed, the theory underestimates the gap size by a factor of two, though it seems to describe the shape of the experimental curve reasonably well. The discrepancy cannot be explained in terms of an aluminum oxide layer initially delaying the etch process. Although the principle is reasonable, the delay time must be nearly equal to the entire time it takes to etch down to the \( \text{SiO}_2 \) in order to cause the data to match such a hypothesis. Neither can the discrepancy be explained in terms of a broader than expected shadow. Such an effect should yield a nearly constant offset between the two curves of Fig. 3.2-4 since the aluminum thickness was nearly always 3500 Å.

Although there is no strong a priori reason to support this explanation, the experimental evidence suggests an etch anisotropy such that the horizontal etch rate exceeds the vertical etch rate. Such
3.2-4 Measured gap width as a function of overetch time.
anisotropy may be due to an interaction between the photoresist and etching solution, or due to polycrystalline aluminum grain boundaries facilitating horizontal etching. In partial support of the anisotropy hypothesis, two scanning electron microscope photographs taken early in the sub-micron gap process development are displayed in Figs. 3.2-5 (a,b). In the first photograph, the basic profile illustrated in Fig. 3.2-3 can be readily discerned, though it appears to be elongated in the horizontal direction. In Fig. 3.2-5b, the gap is shown from an angled viewpoint following photoresist removal. The irregularity of the undercut edge (since improved, see Fig. 3.2-2c) is of roughly the same size as the observed grain size, supporting the suggested effect of grain boundaries on the etch process.

This latter concept was put to work in subsequent processing runs. From the preceding statement, it follows that the smaller the grain size, the less irregular the gap will be. To achieve a smaller aluminum grain size, the evaporation rate was increased to a higher level. Of course a very large grain size should also yield improved gaps (as well as establish the role of grain boundaries in the observed anisotropy) but this will have to wait for future investigation. It appears that the worst grain size is one which is the same size as the gap itself.

Mask design for the gaps is straightforward if done properly. There is a subtle pitfall though, which is associated with slight mask misalignment. Such a pitfall resulted in the redesign of the first metal level mask. There are two ground rules which are useful for the design of the metal level masks. First, one should try to leave as much of the initially evaporated metal on the wafer as possible. This metal can be used to protect tunnel oxide devices and the gate oxide from contamination and physical damage. Second, the dimensions of the first metal mask in the direction parallel to the gap should be exaggerated to
3.2-5 SEM photographs showing (early) gaps

a. Undercut profile suggesting etch anisotropy
b. Top view showing enhanced etching along grain boundaries

(Photographs by A. Pooley)
prevent misalignment shorts subsequent to the second level metal definition.

In Fig. 3.2–6a, an example of first and second level masking patterns is shown for making three electrodes and two gaps. The dashed line shows the border of the first level metal etch pattern. The metal within the border will be removed during the course of the overetch process. Following evaporation and lift off, all metal outside of the border defined by the solid line will be removed. The dashed line within this border will be an inter-electrode gap as shown in Fig. 3.2–6b. Slight misalignment of two patterns will still result in the electrode pattern of Fig. 3.2–6b except that the relative areas of electrodes 1 and 3 will be altered (though electrode 2 will not be affected. Note that this layout represents the reverse pattern of that illustrated in Fig. 3.2–1.

The inter-electrode gap formation process has been found to work reliably. Perhaps its only drawback is that the topology of the process makes gap intersections (such as a 'T' intersection) nearly impossible to fabricate.

3.3 Dark Current Reduction

Causes and Effects

A charge-coupled device is a non-equilibrium device and its key to success is in the length of time it takes to re-equilibrate. For the MOS structure in deep depletion, re-equilibration involves the generation of a minority carrier inversion layer. As discussed in chapter 2, this rate of change of inversion layer charge \( \dot{Q}_{\text{INV}} \) due to minority carrier generation at the oxide-silicon interface, generation in the depleted silicon, and minority carrier extraction from the bulk is referred to as dark current. The bulk extraction current is usually
3.2-6

(a) First level (dashed border) and second level (solid border) mask patterns for metal electrodes

(b) Resultant electrode pattern (gap size exaggerated)
negligible so that interface generation and depletion region generation constitute the dark current, and depending upon processing conditions, can exchange dominating roles.

Dark current due to interface traps and dark current due to depletion region generation are nearly independently determined by the processing conditions, but the physical mechanisms describing the generation processes are similar. Generation/recombination is most easily described statistically in terms of rates and concentrations. In this work, the generation rate is of primary concern. According to the Shockley–Read–Hall recombination process, the local generation rate is proportional to the local trap density (see chapter 2). This is true at the interface and in the depletion region so that the key to dark current reduction in charge-coupled devices operating at room temperature is to reduce the number of active traps.

The interface contributes dark current in two ways. First, the interface traps act as stepping stones for the excitation of electrons into the conduction band. The ability of these interface traps to act as stepping stones depends upon their occupancy. It works out that the type of trap and its energy distribution results in a decreased number of active stepping stones for increased inversion layer charge during the re-equilibration cycle. This is the reason for using the so-called 'fat-zero' [Carnes and Kesonocky, 1972] signal charge in surface channel CCDs to reduce the number of active interface traps and reduce dark current effects, as well as improve charge transfer efficiency.

The second type of dark current arises from minority carrier emission from interface traps, as opposed to the electron-hole pair generation mediated by a trap. In a CCD, the MOS capacitor is repeatedly pulsed from deep depletion to flat-band with varying amounts of charge in the
bucket. Suppose a large signal charge resident in the potential well filled all the trap states with minority carriers. When that charge packet is transferred out and an empty well left behind, those filled interface traps will tend to emit those captured carriers.

Quantitatively, the mean number of carriers emitted in time $t$ per unit area from a set of traps initially full at time $t = 0$, $N(t)$, is given by [Tompsett, 1973]

$$N(t) = \int_{0}^{E_{C}/2} D_{it}(E) \cdot \left\{ 1 - \exp \left[ -\sigma_{it}(E)v_{th}N_{c} \exp \left( -\frac{E}{kT} \right) \right] \right\} dE$$  \hspace{1cm} (3.3-1)

where $D_{it}$ is the interface trap areal density and $\sigma_{it}$ the trap cross-section. Assuming $D_{it}$ and $\sigma_{it}$ are constant, this can be simplified to

$$N(t) = kT D_{it} \ln (\sigma_{it} v_{th} N_{C} t)$$  \hspace{1cm} (3.3-2)

where $(\sigma_{it} v_{th} N_{C})^{-1} < t < \tau_{mb}$ and $\tau_{mb}$ is the midband interface trap time constant. The time derivative of this latter expression is the dark current due to interface trap emission. If the emission time constant is close to the clocking period of the CCD, this dark current has the worst effect on charge transfer efficiency.

The salient point of the preceding discussion is two-fold. First, the elimination or passivation of interface traps is quintessential to the suppression of dark current. Although in MOS capacitor analysis, order of magnitude changes in interface trap densities are routinely observed, even a factor of two can dramatically affect the viability of a CCD device. The second point is that the interface trap contribution is history dependent with a memory dictated by the interface trap time constants.
The reduction of interface traps has been a major part of research and development in the semiconductor industry and the processing techniques used to reduce interface traps has become imbedded in the normal MOS process at Yale. The problem, as will be discussed in section 3.5, is that these techniques may be incompatible with other constraints in the process.

Dark current originating in the deep depleted silicon is bulk trap dependent. From the Shockley–Read–Hall equation, it is clear that the local trap density and local carrier concentration both control the local thermal generation rate. Bulk traps can be physically realized in many ways. Metallic impurities such as gold provide efficient mid-gap traps for carrier generation [Bullis, 1966]. Silicon crystal defects also provide traps for carrier generation [Tanikawa, et al. 1976; Unter, et al. 1977]. In this manner, unpaired silicon bonds in the defect probably behave similarly to unpaired silicon bonds at the surface. These defects may be present in off-the-shelf wafers but they are usually introduced by the fabrication process. One of the more serious defects is the oxidation induced stacking fault [Ravi and Varker, 1974]. This defect is nucleated during the oxidation process by local excess oxygen diffusing into regions of excess vacancy concentration in the crystal. These planar defects usually extend from the silicon surface to several microns in the bulk and are 1–2 microns in diameter. The elastic strain field surrounding these defects can lead to a precipitation of metallic and other impurities around the defect, contributing a double punch to the dark current. The elastic strain field plus impurity decoration can result in a locally enhanced generation zone 20 microns in diameter [Varker and Ravi, 1974].

The gettering effect associated with silicon defects has recently been exploited by creating silicon defects deep in the substrate by
intentional processing. This intrinsic gettering process aids in the
removal of impurities from active regions of the semiconductor [Nelson,
et al. 1983; Swaroop, 1984].

The key to dark current suppression in the deep depleted silicon is
to first avoid the introduction of both metallic impurities and silicon
defects into the substrate, and second, to getter any impurities which
are introduced. This discussion will be continued following the next
sub-section.

Experimental Characterization of Dark Current

Determination of the dark current is closely related to the
determination of minority carrier lifetime, but simpler. The minority
carrier lifetime is a local parameter describing the local
generation/recombination zone, and if the zones are related to silicon
defects in a nearly defect free substrate, it is inappropriate to
describe the semiconductor by a single lifetime parameter. The dark
current is a lumped parameter which includes surface trap generation as
well as bulk trap generation and is the natural parameter to describe a
CCD. The problem with using the dark current is that the dark current
is history dependent and voltage dependent. To a lesser extent, the
dark current is also a local parameter and will vary from capacitor to
capacitor, but will only vary dramatically in a few pathological
capacitors. Such dark current 'spikes' have long plagued the CCD
industry and are accepted as a matter of course as long as the density
is low.

To measure the dark current, a pulsed capacitance measurement (C-t)
is used. The capacitor is biased at −5.0 volts (inversion) through a
Boonton model 72B capacitance meter. The capacitor is exposed to light
momentarily to guarantee that the surface is inverted. For devices with
low dark currents (long 'lifetime') it was observed that when illumination is removed, the capacitance decreases rapidly at first, but would then decrease slowly to its steady state value in the 10-30 second range. Such a decrease must be due to an increase in depletion layer depth corresponding in this constant bias condition to a decrease in surface charge, suggesting slow surface recombination or diffusion of the optically generated super-inversion layer.

Once the device has returned to equilibrium (as determined by a constant capacitance), the capacitor bias is stepped to -10.0 volts, resulting in deep depletion. The capacitance decreases immediately, and then slowly returns to nearly its initial value as the semiconductor re-equilibrates. The time it takes for the semiconductor to return to equilibrium is referred to as the capacitor relaxation time as shown in Fig. 3.3-1.

The dark current may be determined using the Zerbst relation [Zerbst, 1966] as described by Nicollian and Brews (1982, pg. 411). The oxide voltage is written as

\[ V_G - V_{FB} - \psi_s(t) = (Q_{INV} + Q_D)/C_{ox} \]  \hspace{1cm} (3.3-3)

Differentiating with respect to time yields

\[ - \dot{\psi}_s = (\dot{Q}_{INV} + \dot{Q}_D)/C_{ox} \]  \hspace{1cm} (3.3-4)

Rearranging gives

\[- \dot{Q}_{INV} = C_{ox} \dot{\psi}_s - \dot{Q}_D \]  \hspace{1cm} (3.3-5)

For an arbitrary doping profile, it is true that

\[ \dot{Q}_D = qN_D x_D \]  \hspace{1cm} (3.3-6)

and that if the voltage drop across the inversion layer is ignored,
3.3-1 Experimental capacitance as a function of time in response to a five volt step bias.
\[-\dot{\psi}_s = \left(\frac{qN_D}{\varepsilon_s \varepsilon_o}\right) x_D^2\]

Substituting these latter equations into Eq. 3.3-5 results in

\[-\dot{Q}_{\text{INV}} = qN_D \left(x_D^0 \varepsilon_{ox}/\varepsilon_s \varepsilon_o + 1\right) \dot{x}_D\]

The inversion layer depth \(x_D\) is accurately probed by the high frequency capacitance according to

\[x_D = \varepsilon_s \varepsilon_o \left(1/C - 1/C_{ox}\right)\]

so that Eq. 3.3-8 becomes

\[-\dot{Q}_{\text{INV}} = \left(q\varepsilon_s \varepsilon_o N_{D,ox}/C\right) \frac{d}{dt} \left(\frac{1}{C}\right)\]

or finally,

\[\dot{Q}_{\text{INV}} = \left(q\varepsilon_s \varepsilon_o N_{D,ox}/C^3\right) \left(dC/dt\right)\]

In this work, the Zerbst relation (Eq. 3.3-11) is evaluated just after the step voltage is applied. Thus, the dark current is consistently defined for a five volt bucket.

The capacitor relaxation time \(\Delta t\) can also be used to obtain an average value of the dark current during the re-equilibration process. The incremental charge collected in a re-equilibrated CCD bucket \(\Delta Q_{\text{INV}}\) is proportional to the step voltage \(\Delta V_G\) such that

\[\Delta Q_{\text{INV}} = C_{ox} \Delta V_G\]

The average dark current over the interval \(\Delta t\) is

\[Q_{\text{INV}} = C_{ox} \Delta V_G/\Delta t\]

If the dark current decreased at a constant rate to zero during the re-equilibration period, one would expect that the average dark current (Eq. 3.3-13) would be half the initial instantaneous dark current (Eq.
If desired, an average minority carrier lifetime $\bar{\tau}_p$ may be determined by assuming that the thermal generation rate in the incremental depletion region is given by the Shockley–Read–Hall expression (chapter 2) using $p,n < n_i$. Such an assumption is specious both in terms of the actual Shockley–Read–Hall rate as determined by the actual carrier concentrations [Collins and Churchill, 1975] and in terms of the local variations in generation centers [Varker and Ravi, 1974], but nevertheless gives a reasonable lumped estimate. The dark current is therefore

$$\dot{Q}_{\text{INV}} = \frac{q n_i}{2 \pi \bar{\tau}_p} \left[ x_D^o - x_D^\infty \right]$$ \hspace{1cm} 3.3-14

Employing Eq. 3.3-9 and solving for $\bar{\tau}_p$ gives

$$\bar{\tau}_p = \frac{q C_o n_i}{2 \dot{Q}_{\text{INV}}} \begin{bmatrix} (1/C) \bigg|_{t=0^+} - (1/C) \bigg|_{t=\infty} \end{bmatrix}$$ \hspace{1cm} 3.3-15

Figure 3.3-1 shows an actual C-t plot as measured for the active and parallel channel metering wells of device 9A13 (see Fig. 4.3-2). The device area is 203 mils$^2$ with a stray capacitance estimated to be 3 pF. The effective oxide capacitance is 81 pF. At $t = 0^+$, the capacitance drops from 27 pF to 12 pF, and then increases at the initial rate of 0.11 pF/second. The capacitor relaxation time $\Delta t$ is 87 seconds.

Using Eq. 3.3-11 with $N_D$ equal to $1.0 \times 10^{16}/\text{cm}^3$, the five volt bucket instantaneous dark current is 11 nA/cm$^2$. The average dark current using Eq. 3.3-13 is 3.8 nA/cm$^2$. Using the approximate calculation of Eq. 3.3-15, the lifetime appears to be 6.6 $\mu$s. Using a
more sophisticated approach\(^1\), lifetime analysis yields a value of 8.1 
\(\mu\)sec.

**Dark Current Reduction Experiments**

The device dark current was not initially thought to be a major 
fabrication problem. However, following the fabrication of the second 
test lot of 8205 wafers (which were nearly structurally identical to the 
final lot of wafers) it was discovered that the dark current exceeded 
3000 nA/cm\(^2\). To estimate the acceptable dark current level, assume that 
no more than a fraction \(\eta\) of a maximum signal charge can be generated by 
dark current in a maximum integration period \(T_I\). The dark current 
should therefore not exceed

\[
Q_{\text{INV MAX}} \leq \eta \cdot C_{\text{ox}} \cdot \left(V_G - V_T\right)/T_I
\]

3.3-16

Setting \(\eta\) to one part in \(2^9\), and using a maximum integration period of 
50 milliseconds, the dark current in a five volt bucket should be less 
than 12 nA/cm\(^2\). Thus the challenge was to reduce the dark current 
introduced by the basic Yale MOSFET process [Ma, 1954], channel stop 
diffusion, tunnel oxidation and sub-micron gap formation by three 
hundred fold.

The first experiment was to resolve the issue of why other 
researchers in our group obtained long capacitor relaxation times (\(\sim 60\) 
seconds) yet wafer 2A had a relaxation time measured in tenths of 
seconds. In collaboration with V. Zekeriya, three wafers were cleaned 
by the standard process [Dressendorfer, 1978] and simultaneously given a 
dry oxidation at 1000 C for 60 min. Two wafers were \(p\)-type and one was 
\(n\)-type. One of the two \(p\)-type wafers had been wet oxidized at 1100 C

\(^1\)A more sophisticated approach assumes the entire depletion region 
initially contributes to the dark current.
for 60 min. and then stripped of the SiO₂ prior to dry oxidation. As summarized in Table 3.3-1 (expt. 1), the wafer which had undergone prior steam oxidation had a dark current greater than 2000 nA/cm² whereas the two wafers which had only had the subsequent dry oxidation had currents of 120 nA/cm² (n) and 18 nA/cm² (p). Clearly, something happened to the silicon during the steam oxidation which it 'remembered' even after the wet oxide had been stripped.

The second experiment attempted to resolve a contamination problem in the steam oxidation furnace. Two wafers were scribed in half and cleaned. One half of each wafer was dry oxidized in the steam furnace tube, and the other half was dry oxidized in the dry oxidation furnace tube. Each was oxidized at 1050 °C for 60 min. followed by an in-situ N₂ anneal for 30 min. as summarized in Table 3.3-1 (expt. 2). The wafers were given a 15 minute post metallization N₂ anneal (PMNA) at 420 °C. The dark currents ranged from 1 to 30 nA/cm², and failed to indicate that either furnace was contaminated, except that a bias-temperature stress capacitance check revealed the presence of mobile ions (perhaps sodium) through a half volt C-V shift.

The furnaces were cleaned and the experiment retried (Table 3.3-1, expt. 3). The results were nearly identical (including sodium contamination) except that the wafer half closest to the furnace mouth in the dry oxidation tube showed an order of magnitude higher dark current than the other three wafer halves. The wafer in the same position in expt. 2 was similarly afflicted, even though the wafer brand had been subsequently swapped. The only difference between the two furnaces after cleaning was the presence of a platinum-rhodium thermocouple in the dry oxide furnace. The thermocouple was installed inside a hollow quartz tube and in principle should not have been a problem. However, it is possible for heavy metals to diffuse through
quartz [Schmidt, 1983] so that the thermocouple was removed to observe any effect it may have.

In the fourth experiment, the same procedure was used except the wafer cleaning process was slightly modified to try to improve the heavy metal gettering of the cleaning process (see section 3.5). Also, the dry oxidation temperature was reduced to 1000 °C. The effect was to improve the device and wafer to wafer consistency, and the overall dark current. Because three 'parameters' were changed between experiments 3 and 4, only the lumped effect was observed and the role each individual change played not firmly established. It was decided to retain all three changes since the overall effect was beneficial.

The fifth experiment was designed to examine the effect of wet oxidation and post-metallization forming gas annealing (PMFGA; forming gas is a 95% N₂ + 5% H₂ mixture) since the dry oxidation MOS capacitor relaxation times had been successfully extended to the ten minute range for a five volt bucket. Four wafers were fabricated as summarized in Table 3.3-1 (expt. 5). All four were cleaned using the improved technique. Wafer T4 received a 45 min. wet oxidation at 1000 °C which was then stripped. Then, T3 and T4 underwent a 45 min. wet oxidation at 1000 °C which was also stripped. Finally, all four wafers were dry oxidized at 1000 °C for 60 min. followed by an in-situ N₂ anneal. The devices were characterized immediately following metallization. Wafer T4 had a dark current of 10 nA/cm², wafer T3 had 480 nA/cm², and wafer T4 more than 8000 nA/cm². Wet oxidation clearly has an influential effect on dark current and the silicon truly remembers its processing history. Following a 10 minute PMFGA, the wafers' dark current improved to 3.4, 94 and 828 nA/cm² respectively. Adding an additional 30 minutes of PMFGA further improved the dark current to 0.6, 20 and 100 nA/cm² respectively.
The forming gas anneal significantly reduced the dark current. Wafer T4 recovered in a dramatic fashion from 8000 nA/cm² after 40 minutes of PMFGA at 420 C. Varker and Ravi (1974) saw similar effects in PN junction reverse currents following low temperature heat treatments (400 C), which they suggest are due to thermal relaxation of the elastic strain field associated with an oxidation induced stacking fault. They speculate that the strain field itself results in a locally enhanced generation rate, in addition to the contribution made by impurity precipitates and silicon defect.

Wafer T4 may have recovered in a different manner than Ravi-Varker strain field relaxation model. Forming gas decreases the number of interface traps [Deal, et al. 1969], so that one might speculate that wafer T4 originally had an excessive number of interface traps due to surface termination of oxidation induced stacking faults perhaps resulting in excess surface strain fields or excess dangling bonds. The long forming gas anneal may have reduced this interface trap generation source, and decreased the dark current. Such a hypothesis might be easily tested by comparative annealing in an inert atmosphere (e.g. PHNA) with a non-aluminum gate. Careful measurement of (near mid-gap) interface states should also be performed. Although the circumstances were not controlled as indicated above, long PHNA cycles in expt. 11 (Table 3.3-1) resulted in increased dark current rather than decreased dark current which, in the least, does not contradict the oxidation-induced stacking fault induced interface trap generation hypothesis. Support for this hypothesis is also obtained with wafer 02B of expt. 7. The wafer was tested after POFGA and after PMFGA. The POFGA decreased the dark current by a factor of 10, whereas the PMFGA improved it by a factor of 40. The presence of a metal gate should only affect the interface, not bulk strain fields. A careful study should be made of this phenomenon to make any substantial conclusions.
The seemingly miraculous healing powers of post-metallization forming gas annealing is unfortunately not a panacea for dark current. For some devices, PMFGA has virtually no effect on the capacitor relaxation time indicating that the dark current is most likely dominated by lattice defects and impurities in the depleted bulk. More significantly, extended PMFGA may be incompatible with the fabrication of tunnel oxide devices. Dressendorfer (1978) indicates that high quality tunnel oxides may survive a ten minute PMFGA. However, Teng (1983) found that a PMFGA of more than three minutes degrades the MTJS junction performance. In the present work it was found that MTJS junctions can tolerate at least 60 minutes of PWMA (400 C) and at least 10 minutes of PMFGA with only improved device performance. This will be elaborated upon later in this chapter.

In the sixth experiment, the effect of using a dry-wet-dry oxidation process was investigated following a suggestion from T-P. Ma. Three wafers were tested as summarized in Table 3.3-1 (expt. 6). Wafer W4 was dry oxidized at 1000 C for 90 minutes. Wafer W5 was oxidized and annealed at 1000 C in a dry(25 min.), wet (45 min.), dry (25 min.) and N₂ (20 min.) sequence. Wafer W6 was given a 45 min. wet oxidation. All three wafers were stripped of their oxide and then dry oxidized at 1000 C for 90 min. followed by an in-situ N₂ anneal for 30 min. The three wafers were given a 60 min. PMFGA. The dark currents for wafers W4, W5 and W6 were 90, 300, and 20 mA/cm² respectively. The conclusion was that the dry-wet-dry process did not improve dark current, and if it had any effect, it was to make the dark current worse.

It is suggested by Nicollian and Brews (1982, pg. 721) that among many techniques to decrease oxidation induced stacking faults, high temperature wet oxidation works well. In the seventh experiment, the effect of wet oxidation temperature was investigated. As indicated in
Table 3.3-1 (expt. 7), four wafers were wet oxidized at three different periods and temperatures yielding roughly equal oxide thicknesses. The oxide was subsequently stripped and a dry oxide grown at 1100 C for 35 min. One of the wafers was given a low temperature post-oxidation (pre-metallization) FGA for 60 min. The dark current densities following a PMFGA clearly indicate that the low temperature (900 C) wet oxidation is preferable, but also that 1100 C is better than 1050 C. Also indicated is that post oxidation FGA improves the dark current.

In a quick experiment in collaboration with C-C. Wei, an RF plasma anneal [Ma and Ma, 1978; Chin 1981] was attempted at 500 watts for 20 min. The high power level was chosen due to previous success with RIE damaged wafers. Unfortunately, the RF plasma anneal annihilated any observable capacitor relaxation time and distorted the C-V characteristic, suggesting the plasma caused the creation of an enormous number of interface trap generation centers. Following these disastrous results, no further investigation into RF plasma annealing was performed. Perhaps a lower power setting might yield more satisfactory effects.

In the eighth experiment, four different oxides which might be suitable for diffusion masking and a field oxide were tested. In collaboration with T-C. Chen, a plasma enhanced chemical vapor deposition (PECVD) process was used to form a 4700 Å thick oxide. This oxide was densified at 1000 C for 90 min. in N₂. A spin-on SiO₂ film was applied to the second wafer and similarly densified. A dry oxide grown at 1000 C for 120 min. was used on the third wafer, and a wet oxide grown at 900 C for 120 min. was used on the fourth wafer. The oxide mask layer was stripped on all four wafers and a dry oxide was grown at 1000 C for 120 min. The devices were characterized following a 60 min. PMFGA. The PECVD wafer showed a wide range of dark currents
from 35 nA/cm² (very best) to well over 2000 nA/cm². These devices also
exhibited poor C-V characteristics indicating bulk damage or
contamination by the plasma. The spin-on wafer yielded consistently
poor results at over 2000 nA/cm² indicating probable bulk contamination
during the densification process. The dry oxide wafer gave an almost
reasonable dark current level of 23 nA/cm² but the low temperature
(900 C) wet oxide wafer gave the best results at about 10 nA/cm².

Having established a promising wet oxidation process, the effect of
dopant diffusion was examined in the ninth experiment. The basic MOSFET
process was employed and for two wafers, the channel stop diffusion was
included. The first wafer (X1) was subjected to all masking oxidations
and gate oxidations but the actual spin-on/drive-in process was omitted.
The second wafer (X2) was processed as was X1, but a borosilicate film
was spun-on and driven-in. The third and fourth (X3 and X4) wafers,
like X2, were subjected to the p⁺ drive-in but were also given the n⁺
channel stop diffusion. The first three wafers were stripped of their
oxide layers and a new field oxide grown at 900 C for 120 min. Gate
oxidation windows were opened in all four wafers and dry oxidation at
1000 C for 95 min. and in-situ N₂ annealing cycles were carried out.
All four wafers were given a 60 min. pre-metallization FGA at 420 C,
and a 10 min. PMNA. The results summarized in Table 3.3-1 (expt. 9)
show that following the p⁺ diffusion, the dark current increased
significantly, but was reduced after the channel stop n⁺ diffusion.
However, regrowing the field oxide resulted in increased dark current.

A probable explanation involves the temperature dependent solid
solubility of impurity contaminants in heavily doped silicon, moderately
doped silicon, and in silicon defect elastic strain fields. The
gettering property of heavily phosphorous doped silicon was noted by
Goetzberger and Shockley (1960) and studied by Lambert and Reese (1968).
Impurities were probably introduced into the silicon by the borosilicate and phosphorosilicate spin-on films. Due to the differentially higher solid solubility of the n⁺ regions, the impurities were gettered during the n⁺ diffusion process. During the 120 min. wet oxidation subsequent to the n⁺ drive-in, the impurities were drawn out of the n⁺ diffused regions and perhaps collected by higher solid solubility elastic strain field zones caused by the wet oxidation, and could not be re-gettered during the gate oxidation process. Thus, avoiding subsequent wet oxidation after the n⁺ drive-in yields significantly lower dark current. This practice was adopted in the Yale 8205 process.

A satisfactory lot of wafers was fabricated (lot 7) and as indicated by the tenth experiment of Table 3.3-1, a wafer which underwent the MOSFET portion of the Yale 8205 process and channel stop diffusion had excellent characteristics. The MOS dark current was 1.4 nA corresponding to a seven minute capacitor relaxation time (5.0 volt bucket) and the PN junction reverse current density (at -5.0 volts) was 15 nA/cm².

The PN junction reverse current is another measure of semiconductor quality, though it also includes the quality of the diffusion itself. Following an exasperating series of experiments which showed that the borosilicate film spin-on process was unreliable, a boronil dopant source was employed. In the final lot of devices made (lot 9), the PN junction reverse current density (measured at -5.0 volts) was 1.5 nA/cm² following the p⁺ drive-in. After n⁺ diffusion and gate oxidation it increased to 7.7 nA/cm², and following tunnel oxidation, it rose to 37 nA/cm².

The MOS dark current in wafer 9A was 11 nA/cm² following a 10 min. PHNA. For increased PHNA cycle times, the dark current increased.
However, when a 10 min. PMFQA was subsequently performed, the dark current improved to its initial low level or better. For the lot 9 packaged devices, only the initial 10 min. PMNA was performed to insure the integrity of the MTOS junctions.

Summary of Dark Current Reduction Findings

It was observed that the reduction of wet oxidation temperature had a major impact on the dark current. Such an effect is ascribed to the reduction of oxidation rate and subsequent reduction of oxidation induced stacking fault nucleation due to precipitation of local excess of diffused oxygen [Ravi and Varker, 1974].

Forming gas atmosphere low temperature (420 C) heat treatments also contributed to the reduction of dark current. Besides the normal effect of PMFQA [Deal, et al. 1969], the heat treatment may also relax elastic strain in the silicon lattice due to defects and shrink strain field induced excess generation zones in the silicon [Varker and Ravi, 1974]. Post-gate oxidation/pre-metallization forming gas annealing (420 C) was also found to reduce dark current, and is more compatible with tunnel oxide device fabrication.

Phosphorous doped silicon channel stop n+ diffusions also significantly enhanced dark current reduction. This effect is due to the impurity gettering properties of heavily doped silicon through enhanced contaminant solid solubility [Lambert and Reese, 1968]. The gettering effect was observed to depend on the processing sequence, and seemed to work best when the n+ diffusion was the final high temperature (> 800 C) processing step. It is expected that heavily doping the wafer’s backside will assist in the gettering action, but two attempts to try this resulted in a severe autodoping problem during subsequent processing.
To a lesser extent, it was observed that a slightly improved wafer cleaning process showed a positive effect on the dark current. Such wafer cleaning helps remove metallic impurities from the wafer surface prior to high temperature processing.

In future studies, it is hoped that the development of an intrinsic gettering process [Swaroop, 1984] might help control dark current. Success might also be achieved with a combination of the techniques referred to by Nicollian and Brews (1982) such as HCl gettering [Young and Osburn, 1983], but it seems that dark current reduction is a processing art which varies from laboratory to laboratory. One commercial manufacturer revealed that dark current in the 10 nA/cm² range was achieved only on good days. Thus, the suppression of dark current from 3000 nA/cm² on wafer 2A to 11 nA/cm² on wafer 9A through process development in the Yale facility can be considered satisfactory.
<table>
<thead>
<tr>
<th>Expt.</th>
<th>ID&lt;sup&gt;Wafer&lt;/sup&gt;</th>
<th>Type&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Process</th>
<th>Typ. Dark Current (nA/cm&lt;sup&gt;2&lt;/sup&gt;)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>MOA</td>
<td>M</td>
<td>Dry 1050-60; N&lt;sub&gt;2&lt;/sub&gt; 1050-30; PHNA 420-15</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>M0B</td>
<td>(p)</td>
<td>Dry 1050-60; N&lt;sub&gt;2&lt;/sub&gt; 1050-30; PHNA 420-15</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>MOC</td>
<td>(p)</td>
<td>Wet 1100; Strip; Dry 1050-60; N&lt;sub&gt;2&lt;/sub&gt; 1050-30; PHNA 420-15</td>
<td>&gt; 2000</td>
</tr>
<tr>
<td>2</td>
<td>M1A</td>
<td>M</td>
<td>Dry 1050-60 (in dry ox tube); N&lt;sub&gt;2&lt;/sub&gt; 1050-30; PHNA 420-15</td>
<td>1.5</td>
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<td>SH</td>
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<td>SH</td>
<td>Dry 1050-60 (in wet ox tube); N&lt;sub&gt;2&lt;/sub&gt; 1050-30; PHNA 420-15</td>
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<tr>
<td>3</td>
<td>M3A</td>
<td>M</td>
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</tr>
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<td>M</td>
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<tr>
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<td>M6B</td>
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<td>Process</td>
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<tr>
<td>5</td>
<td>W1</td>
<td>W</td>
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<tr>
<td></td>
<td>T1</td>
<td>SH</td>
<td>Dry 1000-60; N₂ 1000-30</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>+ PMFGA 420-10 3 + PMFGA 420-30 0.6</td>
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<tr>
<td>T3</td>
<td>SH</td>
<td>Wet 1000-45; Strip; Dry 1000-60; N₂ 1000-30; + PMFGA 420-10 94 + PMFGA 420-30 20</td>
<td>480</td>
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<td></td>
<td>T4</td>
<td>SH</td>
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<td>W</td>
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<td>W</td>
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<td>W</td>
<td></td>
<td>Wet 1000-45; Strip; Dry 1000-60; PMFGA 420-60</td>
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<td>7</td>
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<td>Expt.</td>
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<td>8</td>
<td>W8A</td>
<td>W</td>
<td>PECVD; N₂ 1000-90; Strip; Dry 1000-120; PMFGA 420-60</td>
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<td>W8B</td>
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<td>Dry 1000-120; Strip; Dry 1000-120; PMFGA 420-60</td>
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<tr>
<td></td>
<td>W9B</td>
<td>W</td>
<td>Wet 900-120; Strip; Dry 1000-120; PMFGA 420-60</td>
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</tr>
<tr>
<td>9</td>
<td>X1</td>
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<td>X2</td>
<td>M</td>
<td>MOSFET; Regrow field ox; Dry 1000-95; N₂ 1000-60; POFGA 420-60; PHNA 420-10</td>
<td>&gt; 5000</td>
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<td></td>
<td>X3</td>
<td>M</td>
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<td>X4</td>
<td>M</td>
<td>MOSFET + channel stop; Dry 1000-95; N₂ 1000-60; POFGA 420-60; PHNA 420-10</td>
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</tr>
<tr>
<td>11</td>
<td>9A</td>
<td>H</td>
<td>Yale 8205</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ PHNA 420-15</td>
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<td>+ PHNA 420-35</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ PMFGA 420-10</td>
<td>10</td>
</tr>
</tbody>
</table>

*Wafer Types:  
H = Monsanto C7 (100) 1-2 Ω-cm 2" diam (n-type)  
SH = Semimetal C7 (100) 3-5 Ω-cm 2" diam (n-type)  
W = Wacker F7 (100) 3-5 Ω-cm 2" diam (n-type)*
3.4 Mask Making

Using the present facilities at Yale to manufacture a set of mask plates is an unpleasant process. Computer aided layout of masks with mask fabrication occurring with a modern E-beam or optical pattern generator is the preferred route to take in the future. Perhaps an intermediate solution might be to employ the new SEM to generate 10x reticles by exposing aluminum and photoresist coated glass plates in a manner similar to that recently demonstrated by W. Rooks of Yale University to write ultra-small patterns. In this section, the current recipe for making masks is presented for completeness, since change often comes slowly.

To aid in the mask making (and subsequent fabrication) process, the mask layout should include a border line encompassing the chip. Such a border aids in 10x reticle mounting and mask alignment. Each mask level should also include a series of fine structures (e.g. fine lines) to assist in focusing and determining photoresist exposures. Such a resolution pattern was found to be useful in the Yale 8205 mask set. Level identifications are also suggested. An alignment key or registration mark is required for each level. A simple cross suffices. The best alignment method seems to make a solid cross on the first level. The second level has a translucent cross of slightly larger dimensions (e.g. 0.2 mils on the final plate). Alignment is done by centering the fabricated cross in the slightly larger cross-shaped window. Alignment accuracies of better than $\pm 2 \mu m$ can be achieved with this simple technique if the 10x reticle rotation problem is solved. Note that the cross may be reused for the third level if the second level process doesn't obliterate it, otherwise a new cross must be made in an adjacent location by the second level.

The Yale 8205 process requires eight mask levels. After cutting each
rubylith (100x), they must be photographically reduced by a factor of ten, resulting in a 10x reticle. The rubylith is mounted on a light box and photographed at the highest possible f-number (largest depth of focus) after being focused at the lowest available f-number. Focusing was facilitated when ground glass system was modified during the course of the present work, so that 'what you see is what you get'. The exposed plate is developed as indicated by Table 3.4-1. The developer mixture ratios and development times may be varied depending on the outcome and exposure time.

Once the 10x reticles have been made, they must be mounted on frames for the step and repeat camera. Mounting is secured using Krazy Glue™ with the reticle’s emulsion side facing into the frame. All reticles must be mounted with the same amount of rotation. In the present work, a technique was developed to assist in 'square' mounting. Two glass slides are glued to graph paper at right angles. The frame is snugly pressed against the glass slides. The 10x reticle is mounted on the frame by making the chip border (discussed above) square with the graph paper lines by eyeballing the set-up. To achieve ± 0.5 mil error or less on the final mask plates, the frame border must be parallel to the graph paper line within ± 0.1 mm. This challenge can be met by patience. Should the final result be undesirable, the reticle can be separated from the frame by soaking the pair in acetone for three hours using ultrasonic agitation. The acetone will not affect the reticle.

The correct use of the step and repeat camera requires similar patience and concentration. The utmost care must be taken to reproduce x and y steps between each run to within ±0.5 mils. For the three barrel step and repeat camera at Yale, a minimum of three runs must be made to make the eight master mask plates. Development is as described in Table 3.4-1.
Table 3.4-1

**HRP Development Process**

<table>
<thead>
<tr>
<th>Mixtures</th>
<th>DGR Powder DN-3/DR-5:</th>
<th>H$_2$O : 1:3</th>
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<tr>
<td>Developer:</td>
<td>H$_2$O : 1:16</td>
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<tr>
<td>Fixer:</td>
<td>Kodak Rapid Fixer as is</td>
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<tr>
<td>50% Methanol:</td>
<td>Methanol: H$_2$O : 1:1</td>
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<tr>
<td>75% Methanol:</td>
<td>Methanol: H$_2$O : 3:1</td>
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</tr>
<tr>
<td>100% Methanol:</td>
<td>Methanol</td>
<td></td>
</tr>
</tbody>
</table>

All baths 22°C - 24°C. Gently agitate plate in each bath.

**Process**

1. Clearing bath to remove anti-halation backing  
   30-60 sec
2. Rinse in running water  
   60 sec
3. Developer  
   ~ 300 sec
4. Rinse in running water  
   60 sec
5. Fixer  
   60 sec
6. Rinse in running water  
   300 sec
7. 50% Methanol  
   15 sec
8. 75% Methanol  
   15 sec
9. 100% Methanol  
   15 sec
10. Blow dry with $N_2$
To copy a working mask plate from the master mask plate, an emulsion to emulsion contact exposure is used. Subsequent development results in a negative polarity mirror image of the master plate. To obtain a faithful copy of the master plate, the intermediate copy must be copied. However, to obtain a positive polarity mirror image, a reversal development process is used. The basic process is to develop the emulsion to emulsion exposed plate in a solution which does not dissolve unexposed emulsion, but turns exposed emulsions black. This blackened emulsion is then removed using a bleach bath followed by a clearing bath. The previously unexposed remaining emulsion is then given a blanket exposure and developed turning it black. This emulsion is then fixed and hardened in a fixer bath in the usual way. Thus, the initially unexposed emulsion shadowed by a black master plate emulsion is blackened, resulting in a positive polarity mirror image. The resolution of this process is nearly as good as the negative process and more than adequate for the Yale 8205 plates. The process is described in Table 3.4-2.

A photograph showing the completed (and mounted) 10x reticles is displayed in Fig. 3.4-1.
### Table 3.4-2

**Reversal Process**

<table>
<thead>
<tr>
<th>Mixtures</th>
<th>Description and Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dacomatic Clearing Bath</td>
<td>DN-3/DR-5: ( \text{H}_2\text{O} : 1:3 )</td>
</tr>
<tr>
<td>D-8 Developer (Kodak)</td>
<td>Stock: ( \text{H}_2\text{O} : 1:3 )</td>
</tr>
<tr>
<td>R-9 Bleach Bath</td>
<td>4 liters ( \text{H}_2\text{O} ) + 38 grams Kodak Potassium Dichromate + 48 mL ( \text{H}_2\text{SO}_4 )</td>
</tr>
<tr>
<td>CB-6 Clearing Bath</td>
<td>4 liters ( \text{H}_2\text{O} ) + 60 grams Kodak Sodium Bisulfite + 2 grams Calgon (water softener)</td>
</tr>
<tr>
<td>HRP Developer (Kodak)</td>
<td>HRP Dev.: ( \text{H}_2\text{O} : 1:8 )</td>
</tr>
<tr>
<td>Kodak Rapid Fixer</td>
<td>as is</td>
</tr>
<tr>
<td>50% Methanol</td>
<td>Methanol: ( \text{H}_2\text{O} : 1:1 )</td>
</tr>
<tr>
<td>75% Methanol</td>
<td>Methanol: ( \text{H}_2\text{O} : 3:1 )</td>
</tr>
<tr>
<td>100% Methanol</td>
<td>Methanol</td>
</tr>
</tbody>
</table>

Baths 22°C – 24°C. Gently agitate plates in each bath.

**Process**

1. Clearing bath Dacomatic       30–60 sec
2. Rinse in running water        60 sec
3. Develop in D-8 Developer until black 120 sec
4. Rinse in running water        60 sec
5. Bleach in R-9 bath until transparent 120 sec
6. Rinse in running water        60 sec
7. Clearing bath CB-6            180 sec
8. Rinse in running water        60 sec
9. Presoak in HRP developer      20 sec
10. Rinse in running water       60 sec
11. Blanket exposure             120 sec
12. Develop in HRP developer until black 60–120 sec
<table>
<thead>
<tr>
<th>Step</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>13. Rinse in running water</td>
<td>30 sec</td>
</tr>
<tr>
<td>14. Fix in Rapid Fixer</td>
<td>120 sec</td>
</tr>
<tr>
<td>15. Rinse in running water</td>
<td>300 sec</td>
</tr>
<tr>
<td>16. Dehydrate in 50% Methanol</td>
<td>15 sec</td>
</tr>
<tr>
<td>17. Dehydrate in 75% Methanol</td>
<td>15 sec</td>
</tr>
<tr>
<td>18. Dehydrate in 100% Methanol</td>
<td>15 sec</td>
</tr>
<tr>
<td>19. Blow dry with N₂</td>
<td></td>
</tr>
</tbody>
</table>
3.4-1 10X reticles for Yale 8205 chip. Level IDs in lower right-hand corner are as follows:

R: Registration   C: Contact vias
P: Boron diffusion 1: First level metal
N: Channel stop diffusion 1: Improved first level metal
G: Gate oxide windows 2: Second level metal
T: Tunnel oxide windows

(Note: Polarity reversal from final mask plates)
3.5 Fabrication Process

The Yale 8205 process is quite similar to the processes used by past and present investigators, and only departs significantly by the reduction of wet oxidation temperature to 900 C, the use of post-gate-oxidation forming gas annealing (420 C), the formation of source-drain contacts, and of course in the fabrication of sub-micron inter-electrode gaps. The process is interlocked beyond what is revealed by a casual inspection. Slight changes in parameters or sequences can dramatically affect device behavior and yield. The best advice offered in this thesis is to not 'mess' with the recipe.

A series of device cross-sections illustrating the basic fabrication sequence is shown in Figs. 3.5-1(a-h). The device fabricated in this sequence is the charge packet initiated MTOS junction switching experiment described in detail in chapter 4 and illustrated in Fig. 4.3-3.

The wafers are selected and cleaned. Best results have so far been obtained with Monsanto n-type wafers (100) 2'' in diameter with 2-Ω cm resistivity (CZ). In retrospect, more lightly doped wafers may have been preferable (10-20 Ω·cm). Attempts to use Wacker n-type wafers (100) 2'' in diameter with 5 Ω·cm resistivity (float zone) were disappointing. The dark current was usually worse with these wafers and the MTOS junctions seldom worked. The latter may be related to the quality of surface polishing, which was done for the Wacker wafers by a small business in Massachusetts.

A wet oxidation is used to grow a 1000 Å oxide mask for the silicon etching of registration marks (R-level). Since photoresist does not adhere well to SiO₂ exposed to Si etch, the SiO₂ is stripped and a 2000 Å wet oxide regrown. This oxide serves as the borofilm drive-in mask
3.5-1 Yale 8205 process summary cross-sections

- a. Registration marks
- b. Borofilm diode formation
- c. Phosphorusilicafilm channel stop formation
- d. Gate oxide window and growth
- e. Tunnel oxide window and growth
- f. Contact via etch
- g. First level metal
- h. Final cross-section
(P-level). The borofilm (a boron doped polymer) and oxide mask are stripped using 10% HF.

A final wet oxide is grown to a thickness of 3000 Å to serve as a phosphorosilica film drive-in mask and field oxide (N-level). Gate oxide windows are opened in the sandwich structure and the gate oxide grown. No autodoping was observed during the gate oxide growth from adjacent phosphorosilica film. The gate oxide is given a post-oxidation, low temperature heat treatment (420 C) in a forming gas atmosphere. Although not as effective as a post-metallization forming gas anneal (which is incompatible with tunnel oxides for long periods of time), it does reduce dark current by an order of magnitude.

Tunnel oxidation windows are opened in the gate oxide and the tunnel oxide is grown as described by Dressendorfer (1978), Lai (1979) and Teng (1983). The oxidation is at 800 C for 15 minutes followed by an in-situ anneal of 15 minutes. The final cleaning of the windows prior to tunnel oxide growth was found to have a significant influence on tunnel oxide thickness and quality. A few drops of HF in the final H2O rinse bath (preferably chilled) seems to yield the best results [T-C. Chen, private communication]. It was also observed that wafers which had undergone significant processing prior to tunnel oxide growth had thinner tunnel oxides than near virgin wafers oxidized for the same amount of time. Aluminum is immediately evaporated on the tunnel oxide to a thickness of 2000 Å.

Contact windows are opened to p⁺ and n⁺ regions by a double etch process. First, aluminum etch is used to etch through the 2000 Å metal layer. Then, oxide etchant is used to etch through the gate oxide layer. Unfortunately, BOE attacks aluminum so that unless the process is carefully controlled, the aluminum surrounding the contact window is
bevelled over several microns. Although actually a side benefit assisting step coverage in the Yale 8205 process, it looks ugly and cannot be used in smaller geometries. Other oxide etch techniques (i.e. gas phase) may be more fruitful in constrained layouts. The contact made by this new double-etch technique has relatively low resistance, and for example, allows the fabrication of high quality tunnel oxide MOSFETs.

Once the contact windows have been opened and the photoresist removed, aluminum ($1500 \, \text{Å}$) is evaporated. The first level metal mask is used to form the photoresist overhang for the subsequent aluminum $^0$ (shadow) evaporation. This 2000 Å aluminum layer and the previous 3500 Å of aluminum are patterned following lift-off using the second level metal mask. Backside evaporation of aluminum is followed by a 10 minute post-metallization $N_2$ anneal.

Following tunnel oxidation, it has been found that the use of ultrasonic agitation degrades tunnel oxide durability. Teng (1983) used ultrasonic agitation and observed MTOS junction degradation for annealing periods exceeding a few (i.e. 3) minutes. This was confirmed by more recent experiments in which ultrasonic agitation was inadvertently used [C-C. Wei, private communication]. It was found in this work that without ultrasonic agitation, low temperature ($400 \, \text{°C}$) post-metallization $N_2$ anneals could be performed for at least 60 minutes, and PMFGEA for at least 10 minutes. The MTOS junction performance as measured by OFF state current (ambiguous as discussed in chapter 4) improved steadily (lower current).

To package the chips, they are coated with a protective layer of photoresist and carefully scribed and split apart. The resist is removed in an acetone bath. The chips are mounted in packages using a
conductive epoxy which is cured by an air bake at 150 °C for 60 min.
Bonding is done with 1 mil gold wire and an ultrasonic bonder set at a
low power and time setting. The chip/package is heated to 150 °C as a
ball bond is formed on the chip bonding pad and a wedge bond on the
package. The package leads are trimmed if necessary. The Yale 8205
chips were packaged in both 24 pin dual-in-line packages (DIPs) and in
44 pin leadless carriers. The MTOS packaging yield was 100% as
determined by measuring device characteristics before and after
packaging.

The Yale 8205 process is given in recipe form in Table 3.5-1 and a
photograph of a completed device after packaging in a 44 pin leadless
carrier is shown in Fig. 3.5-2.
Table 5.5-1

Yale 8205 Fabrication Process

1. Wafer Initialization

   A. Select wafers
      - best results have been obtained with Monsanto n-type (100) 2" diam. 1-2 Ω-cm one side polished

   B. Scribe IDs into backside
      - place front side on texwipe and use diamond scribe on backside near edge

   C. Blow off wafer with N₂ to remove particles

2. Wafer Cleaning

   A. Preheat TCE and acetone to ~ 50°C in ultrasonic agitator. Cover to keep from evaporating.

   B. TCE ultrasonic > 5 min

   C. Acetone ultrasonic > 2 min

   D. DI rinse > 1 min

   E. Methanol ultrasonic > 5 min
      - prepare "super-mickey" ingredients
        40 mL H₂O₂ into SM beaker
        120 mL H₂SO₄ into grad. cyl.

   F. DI rinse > 2 min
      - mix SM; pour H₂SO₄ into SM beaker slowly

   G. SM ultrasonic 10 min

   H. DI rinse > 2 min

   I. 10% HF ~ 1 min (49% HF: H₂O :: 1:1)

   J. Blow dry w/N₂ out of 10% HF - should be hydroscopic if clean

   K. Transport to furnace in clean petri dish
Table 3.5-1 (cont.)

3. Initial wet oxidation (900°C, 40 min)
   (This is the standard furnace procedure with a slow pull)
   A. Load wafers into furnace
      i. Pull out hot boat with cool rod
      ii. Blow dust off wafer with N₂
      iii. Load wafers onto boat facing mouth
      iv. Push in 1-2 in/sec
      v. Put on end cap
   B. Oxidize 40 min.
   C. Unload wafers
      i. Pull boat to furnace mouth 1 in/sec
      ii. Replace end cap
      iii. Wait 5 min.
      iv. Pull out boat
      v. Blow wafers cool with N₂
      vi. Place in clean petri dish

4. Photolithography R-level
   (This is the standard photolithography procedure)
   A. Prepare AZ1370 photoresist (room temp.)
   B. Blow dust off pipette and bulb
   C. Mix HF312 developer: H₂O :: 1:1 (room temp.)
   D. Spin on AZ1370 3000 RPM 60 secs
   E. Bake 90°C in clean air 10 min.
   F. Align and expose ~ 65 secs
   G. Develop until developed one-at-a-time ~ 40 secs
   H. DI rinse > 2 min
   I. Spin dry ~ 1 min
   J. Inspect and check alignment
   K. Bake 90°C in clean air 10 min
   L. BOE etch SiO₂ until clear + 1 min ~ 3 min
Table 3.5-1 (cont.)

6. Strip PR
   (This is the standard photoresist strip process)
   A. DI rinse > 2 min
   B. Acetone (ultrasonic) > 3 min
   C. Fresh acetone (ultrasonic) > 2 min
   D. DI rinse > 1 min
   E. Methanol (ultrasonic) > 5 min
   F. Blow dry with N₂

7. Silicon Etch
   A. Mixed etchant ~ 1 sec
      - 70% HNO₃: 49% HF: 99.9% Acetic :: 3:1:1
      - etch individually
   B. DI rinse immediately > 3 min

8. BOE strip SiO₂ 5 min

9. DI rinse > 2 min

10. Methanol (ultrasonic) > 1 min

11. Blow dry with N₂ and transport to furnace

12. Wet oxidation, 900°C 90 min slow pull > 2000 Å

13. Photolithography P-level

14. BOE etch SiO₂ until clear + 1 min ~ 5 min

15. Strip PR

16. Nitric Acid (70% HNO₃) 10 min
    - need hydrophilic surface

17. DI rinse > 2 min

18. Methanol (ultrasonic) > 1 min
Table 3.5-1 (cont.).

19. Blow dry with $N_2$

20. Bake out $90^\circ C$ in clean air  > 5 min

21. Spin on Borofilm 100, 3000 RPM  60 secs

22. Bake $90^\circ C$  > 5 min

23. Bake $150^\circ C - 200^\circ C$  > 5 min

24. Drive in $^+1050^\circ C$, $N_2 @ 1.6$ slpm, $O_2 @ 0.07$ slpm
   A. Load into boat face-to-face, back-to-back
   B. Load boat in furnace mouth, put on end cap
   C. Prebake  10 min
   D. Push into furnace 1 in/sec
   E. Replace end cap, drive-in  75-90 min
   F. Pull to mouth to cool  10 min
   G. Unload

25. Strip oxide and borofilm (10% HF) until clear  ~ 8 min

26. Wet oxidation, $900^\circ C$ 3 hours, slow pull  > 3000 A

27. Photolithography N-level

28. BOE etch $SiO_2$ until clear + 1 min
   - record time  ~ 7 min

29. Strip PR

30. Bakeout $90^\circ C$  > 5 min

31. Spin on Phosphorosilica film 3000 RPM
   - "$C_o = 3 \times 10^{20}/cm^2$"  60 secs

32. Bake $90^\circ C$ in air  > 5 min
### Table 3.5-1 (cont.)

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>33.</td>
<td>Bake 150°C - 200°C in air</td>
<td>&gt; 5 min</td>
</tr>
<tr>
<td>34.</td>
<td>Drive-in n⁺ 1000°C N₂ @ 2.0 slpm, O₂ @ 0.2 slpm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A. Load wafers close packed front-to-back</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B. Proceed as for p⁺ drive-in (step 24)</td>
<td></td>
</tr>
<tr>
<td>35.</td>
<td>Photolithography G-level</td>
<td></td>
</tr>
<tr>
<td>36.</td>
<td>BOE etch SiO₂ until kerf clears + time from step 28 + 1 min</td>
<td></td>
</tr>
<tr>
<td>37.</td>
<td>Strip PR</td>
<td></td>
</tr>
<tr>
<td>38.</td>
<td>Dry O₂ should flow in furnace</td>
<td>&gt; 60 min</td>
</tr>
<tr>
<td>39.</td>
<td>Dry oxidation 1000°C O₂ @ 2.0 slpm</td>
<td>90 min</td>
</tr>
<tr>
<td>40.</td>
<td>N₂ in-situ anneal cool down</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A. Switch to N₂ @ 2.0 slpm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B. Reset furnace temperature to 800°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C. Let cool down</td>
<td>60 min</td>
</tr>
<tr>
<td></td>
<td>D. Slow pull</td>
<td></td>
</tr>
<tr>
<td>41.</td>
<td>Post-oxidation FGA 420°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(5% H₂, 95% N₂)</td>
<td>60 min</td>
</tr>
<tr>
<td>42.</td>
<td>Photolithography T-level</td>
<td></td>
</tr>
<tr>
<td>43.</td>
<td>BOE etch SiO₂ until clear + 1 min record time</td>
<td>~ 3 min</td>
</tr>
<tr>
<td>44.</td>
<td>Strip PR</td>
<td></td>
</tr>
<tr>
<td>45.</td>
<td>Dip etch in chilled H₂O with a drop</td>
<td></td>
</tr>
<tr>
<td></td>
<td>or two of HF</td>
<td>10 sec</td>
</tr>
<tr>
<td>46.</td>
<td>Blow dry with N₂ (or spin dry) and transport to furnace</td>
<td></td>
</tr>
<tr>
<td>47.</td>
<td>Dry oxidation 800°C O₂ @ 2.0 slpm</td>
<td>10-15 min</td>
</tr>
</tbody>
</table>
Table 3.5-1 (cont.)

47. cont.
   A. Pull hot boat to mouth
   B. Load wafer face up at mouth
   C. Push in and replace end cap

48. Switch to N₂ @ 2.0 slpm in-situ anneal 15 min

49. Evaporate 2000 Å Al @ 10 Å/sec

50. Photolithography C-level

51. Al etch until clear + 1 min ~ 5 min

52. DI rinse > 2 min

53. Spin dry

54. BOE etch SiO₂ (use time from step 43) ~ 3 min

55. DI rinse > 2 min

56. Strip PR (no ultrasonic)

57. Evaporate 1500 Å Al @ 10 Å/sec

58. Photolithography Ml-level - align carefully

59. Al etch until clear + 3 min overetch ~ 10 min

60. DI rinse > 2 min

61. Spin dry

62. Evaporate 2000 Å Al @ 10 Å/sec
   -use point-like source

63. Lift-off in acetone (no ultrasonic) 60 min
Table 3.5-1 (cont.)

64. DI rinse > 2 min
65. Spin dry
66. Photolithography M2-level
67. Al etch until clear + 1 min
   - don't stop when 2000 Å Al clears ~ 8 min
68. Strip PR (no ultrasonic)
69. Backside swab etch BOE
70. DI rinse > 2 min
71. Methanol (no ultrasonic) > 1 min
72. Blow dry with N₂
73. Backside Al evaporation ~ 3000 Å
74. PMNA 400°C 10 min
75. Measure and weep
3.6 Process Verification

In this section, the completely fabricated device characteristics are reported as measured using the process verification structures. The data is reported for wafers 7B and 9A which were those diced and packaged and used in the subsequent experimental testing of the prototype circuits.

The \( p^+ \) boron diffusion process can be checked using diffused resistor and contact string and evaluated in terms of the diffused layer sheet resistance and PN junction leakage current. The sheet resistance \( r_D \) and contact via (1 mil x 2 mils) resistance \( r_C \) can be determined from the diffused resistor resistance \( R_D \) and contact string resistance \( R_C \) in combination with the layout geometry. From the layout,

\[
R_D = 172 \times r_D + 2 \times r_C \quad 3.6-1
\]

and

\[
R_C = 9 \times r_D + 18 \times r_C \quad 3.6-2
\]

so that

\[
r_D = \frac{R_D}{171} - \frac{R_C}{1539} \quad 3.6-3
\]

and

\[
r_C = 9.55 \times \frac{R_C}{171} - \frac{R_D}{342} \quad 3.6-4
\]

For wafer 7B, a defective dopant source resulted in \( r_D = 2.1 \, \text{k}\Omega/\square \) and \( r_C = 450 \, \Omega \). In the improved wafer 9A process, the sheet resistance was reduced to 16 \( \Omega/\square \) and \( r_C \) to 4 \( \Omega \). The PN junction leakage current measured at -5.0 volts was approximately 40 nA/cm², though wafer 7B diodes suffered from low voltage soft breakdown above 10 to 12 volts reverse bias, undoubtedly attributable to the defective dopant source. The diodes fabricated show a two to three order of magnitude improvement in leakage current over those fabricated by Teng (1983), attributable to the reduction in bulk traps achieved by the improved process.

The \( n^+ \) phosphorous diffusion yielded sheet resistances well under 1 \( \Omega/\square \). The field oxide sandwich was in the 5000 \( \AA \) to 6000 \( \AA \) thickness
range. This gives a bonding pad stray capacitance close to 1 pF. The
gate oxide was 590 Å thick and 550 Å thick for 7B and 9A devices
respectively as determined using the accumulated gate oxide capacitance
corrected for stray capacitance. The gate oxide interface trap density
measured close to inversion using the high/low frequency capacitance
technique of Wagner and Berglund (1972) was in the 2–3 x 10^{10}/cm^2 eV
range for both wafers. In that method,

\[ D_{it} = \frac{C_{LF} - C_{HF}}{qA} \left( 1 - \frac{C_{LF}}{C_{ox}} \right)^{-1} \left( 1 - \frac{C_{HF}}{C_{ox}} \right) \] 3.6-5

where \( C_{LF} \) is the low frequency capacitance (quasi-static) at some
voltage, and \( C_{HF} \) the high frequency (1 MHz) capacitance at the same
voltage. No hysteresis was observed in the room temperature HF C-V
characteristic, though it is expected that there were unactivated mobile
ions present due to the aluminum evaporation process. Fortunately,
almost all biases used experimentally were negative, thus retaining
positive mobile ions (i.e. \( N_a^+ \)) at the Al-SiO_2 interface.

The typical breakdown strength of the gate oxide for wafer 7B was 7 x
10^6 V/cm). Anomalous low voltage breakdown (1–2 x 10^6 V/cm) of the
wafer 9A gate oxide was observed in many parts, and was the major cause
of low operational yield on this wafer. This breakdown was not
systematically studied but may be related to the PMFGA of wafer 9A
following gate oxidation, metallization and electrode definition prior
to tunnel oxidation, etc. Such an inserted sequence was designed to
preview device behavior prior to investing unwarranted processing time
for tunnel oxidation and sub-micron gap formation. Such a preview
process sequence was not performed on wafer 7B. Post-oxidation FGA
prior to tunnel oxide window definition has not exhibited any problem
(lot X) so that PMFGA in the preview sequence is most likely the
culprit.
The tunnel oxide was determined to be in the 31 Å to 32 Å thickness range on wafer 7B, and in the 33 Å to 34 Å thickness range on wafer 9A as determined using a modified [Dressendorfer, 1978] C-V extrapolation technique [McNutt and Sah, 1975], with $\varepsilon_{ox} = 3.9$. The flat-band voltage was $-0.19$ volts ± 0.02 volts where the uncertainty is due to uncertainties in oxide thickness and stray capacitance values. The OFF state current (for wafer 9A) biased at $-3.5$ volts was typically 3.5 $\mu$A/cm$^2$, although this current can be reduced by extending the PMNA cycle. The ON state current was typically 100 times larger at this bias, and increases exponentially (see chapter 4) with bias voltage up to a breakdown voltage of $-4.1$ volts at a current density of 2.5 mA/cm$^2$. Operating the device in this range is a risky proposition since breakdown is a costly event with only two dozen devices packaged. The ON state holding voltage was $-3.2$ volts so that most devices were operated at $-3.5$ volts.

The MTOS durability test site consists of two adjacent MTOS junctions (40 mils$^2$ each) separated by a sub-micron gap. One junction is formed by etching off the aluminum covering the tunnel oxide during the overetch/undercut process, and then recoating the tunnel oxide with aluminum. The MTOS junction survived the etch/recoat process without significant change in characteristics. For example, the OFF current in the recoated junction was 3.1 $\mu$A/cm$^2$ compared to 2.1 $\mu$A/cm$^2$ in the adjacent junction ($-3.5$ volts). The ON current (also at $-3.5$ volts) was 217 $\mu$A/cm$^2$ in the recoated junction and 201 $\mu$A/cm$^2$ in the adjacent device. The ability to fabricate such closely spaced MTOS junctions leads to intriguing opportunities for future investigation.

The gate oxide MOSFET test site on wafer 9A was measured and showed excellent MOSFET characteristics, as shown in Fig. 3.6-1a. The saturated MOSFET transfer characteristic was carefully measured over the
3.6-1 MOSFET characteristics

a. Gate oxide (550 Å)
b. Tunnel oxide (33 Å)
range zero to 0.5 mA. Plotting the square root of current as a function of gate voltage gave a very straight line indicating a threshold voltage of -2.1 volts. The slope of the line is related to an effective surface mobility \( \mu'_p \) using a simple equation for saturation current \( I_s \) [Streetman, 1972]

\[
I_s = (\mu'_p C_{ox} W/2L) (V_G - V_T)^2
\]

so that

\[
\frac{d \sqrt{I_s}}{d V_G} = (\mu'_p C_{ox} W/2L)^{1/2}
\]

Using \( W = 4 \) mils, \( L = 1 \) mil and \( C_{ox} = 62 \mu F/cm^2 \) yields an effective surface mobility of 146 cm\(^2/V\) sec.

This result can be used for reference in discussing similar measurements performed on the tunnel oxide MOSFET test site with similar geometry. The characteristics of this 33 Å oxide MOSFET can be seen to appear normal in Fig. 3.6-1b. The saturated MOSFET current was carefully measured over the same range of zero to 0.5 mA and the square root of the saturated current as a function of gate voltage plotted. A very straight line was obtained yielding a threshold voltage of -0.8 volts and effective mobility of 75 cm\(^2/V\) sec. This mobility reduction may be due to a higher inversion layer charge density. If the saturated channel charge is written as

\[
Q_C = \frac{2WL}{3} C_{ox} (V_G - V_T)
\]

then the ratio of channel charge for the tunnel oxide MOSFET to channel charge in the gate oxide MOSFET at equal saturation currents is
approximately

\[
\frac{Q_T^G}{Q_G^C} = \left( \frac{d_{ox}^T}{d_{ox}} \right)^{1/2}
\]

3.6-9

assuming equal mobilities and geometries. Thus, the tunnel oxide MOSFET has approximately 20 times higher channel charge. The mobility reduction may also be due to differences in interface trap density or may even be fundamental in nature, such as dimensionally enhanced surface scattering or silicon surface tensile stress reduction. Further studies to understand this phenomenon are presently underway.

The sub-micron gaps were fabricated with excellent yield on wafer 7B and less so on wafer 9A. However, in most cases, any residual short circuits between adjacent electrodes could be burned out by passing a few hundred milliamperes of current through the short, without observable damage to the devices. Typically the resistance between gaps exceeded \(10^{12}\) Ω.

To test the basic functionality of the fabricated CCDs, the parallel channel of the MTOS junction charge packet initiated switching experiment (Fig. 4.3-2) was used to create a charge packet using the surface potential equilibration method, and then dump it to the charge packet output sense amplifier (appendix D). The output of the source-follower is shown as a function of metering well voltage in Fig. 3.6-2. This photograph demonstrates the functionality of the CCD structures fabricated on the Yale 8205 chip.
DEVICE 7B9 PARALLEL CHANNEL

GND
VOUT
1V/DIV

1V/DIV
-VXI
GND

RL=500kΩ  2MSEC/DIV

VOA=-12VOLTS
VDA=-12VOLTS
VMW=-8VOLTS

3.6-2  CCD input/output verification