DEVELOPMENT OF CMOS ACTIVE PIXEL IMAGE SENSORS FOR LOW COST COMMERCIAL APPLICATIONS

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ABSTRACT

The Jet Propulsion Laboratory, under sponsorship from the NASA Office of Advanced Concepts and Technology, has been developing a second-generation solid-state image sensor technology. Charge-coupled devices (CCDs) are a well-established first generation image sensor technology. For both commercial and NASA applications, CCDs have numerous short comings. In response, the active pixel sensor (APS) technology has been under research. The major advantages of APS technology are the ability to integrate on-chip timing, control, signal-processing and analog-to-digital converter functions, reduced sensitivity to radiation effects, low power operation, and random access readout.

JPL has been exploring a complementary metal-oxide-semiconductor (CMOS) APS technology. CMOS is a widely used microelectronics technology for microprocessors, memory devices and application specific integrated circuits (ASICs). Use of CMOS for image sensors can reduce fabrication costs by over a factor of three compared to CCD image sensors. Thus, the JPL-developed technology has widespread appeal for low cost commercial applications such as video phones, computer input devices, surveillance and robotics.

The JPL CMOS APS technology is being successfully transferred to industry. The sensors feature TTL-compatible operation (5 volts or less), random accessibility, 75 dB dynamic range, fixed pattern noise less than 0.1 %, read noise in the 15-25 electron r.m.s. range, and low power.

This paper will discuss the development of CMOS APS technology, its performance characteristics, and its application to low cost commercial products.

1. INTRODUCTION

Imaging system technology has broad applications in commercial, consumer, industrial, medical, defense, and scientific markets. The development of the solid-state charge-coupled device (CCD) in the early 1970's led to relatively low cost, compact imaging systems compared to vidicons and other tube technology. The CCD has advanced as the microelectronics industry has improved silicon material quality and device fabrication technology. Today, in mass production, CCDs are made at the rate of over 10 million imager chips per year in Japan (Sony, Matsushita, and NEC dominate production) mostly for video camcorder applications. At this production rate, a CCD has a manufacturing cost of approximately $10-$15 per chip, or about $50/Mpixel (million pixels). Unfortunately, these large production runs are mostly used in vertically integrated products so that the cost for low volume external purchase of CCDs is typically much higher. Megapixel CCD sensors, desired for low volume applications, are typically made in the U.S. or Europe rather than Japan and cost in the neighborhood of $1,000/Mpixel. Scientific-grade defect-free sensors can cost as much as $10,000/Mpixel. (HDTV format sensors with 2M pixels, will enter production in Japan in a few years and will lower the cost of megapixel sensors significantly.)

The major reason why megapixel CCDs are so expensive is related to the high cost of fabrication equipment that must be amortized over low volume production runs. Furthermore, modern CCD technology is a significant departure from mainstream microelectronics fabrication technology -- complementary metal-oxide-semiconductor or CMOS, which is used for most microprocessor and ASICs. CMOS technology is backed by an enormous worldwide R&D workforce and infusion of capital. In contrast, advancement of CCD technology is limited by a lack of both investment capital and worldwide level of effort.

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CMOS technology advancement has been rapid. This advancement has been following the well-known trend that microelectronic device feature size decreases by approximately a factor of two every five years. In large volume production, six-inch CMOS wafer fabrication costs approximately $1,000 per wafer. Thus, a CMOS image sensor with a 10 micron pixel pitch might have a manufacturing cost of approximately $10/Mpixel, or about five times less than a CCD. For lower volume production, the cost of fabricating a six-inch CMOS wafer is about the same as fabricating a four-inch CCD wafer. A six inch wafer yields about three times the number of large-sized chips as a four-inch wafer so the manufacturing cost of a CMOS image sensor would be approximately three times less than a CCD image sensor.

The use of CMOS presents an additional opportunity for significantly reducing imaging system cost, power and mass as well as improving reliability. A CMOS-based image sensor can be readily integrated with on-chip timing, control, signal chain and analog-to-digital converter (ADC). Unlike a CCD system that requires a large number of power supply voltages, clock drivers that can drive large capacitances, a discrete component signal chain, and an ADC chip, the CMOS sensor can be a single-chip camera system with a full digital interface. The image sensor can communicate directly with a microprocessor or computer, significantly reducing system complexity and concomitant development time. Other advantages of the CMOS APS are: TTL-compatible operation (0-5V), only a single power supply is required, electronic shuttering, readout windowing, variable integration time and pixels in the array can be addressed randomly.

The major hurdle to realizing the economic benefit of utilizing CMOS-based image sensors has been the performance of the sensor. Until recently, CCD imager performance has been vastly better than its CMOS counterpart. In this paper, a high performance CMOS sensor technology competitive with CCDs and suitable for many scientific, commercial, consumer, industrial, medical and defense applications is described.

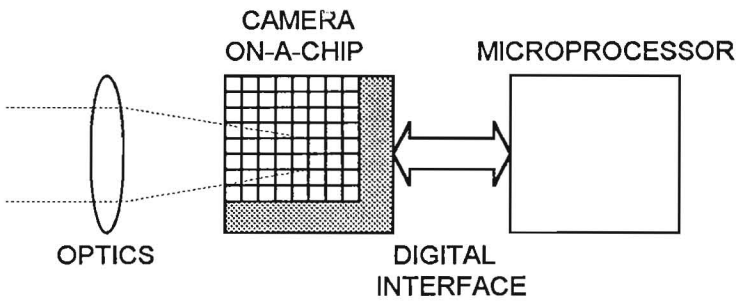

Fig. 1. Block diagram of highly integrated, low mass, low power, compact imaging system

2. CMOS ACTIVE PIXEL SENSOR

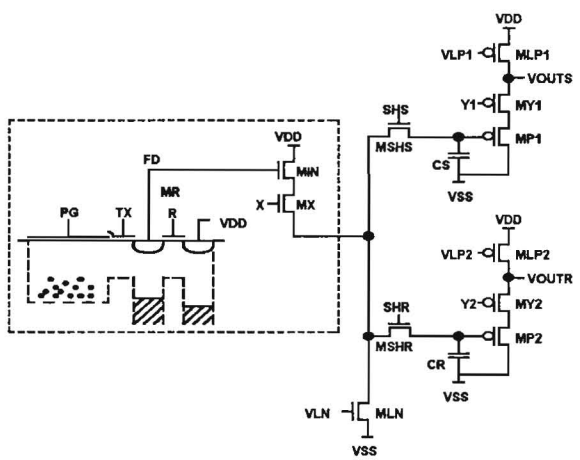

Fig. 2. Circuit diagram of CMOS APS

The Jet Propulsion Laboratory, California Institute of Technology, has recently developed a CMOS active pixel image sensor (APS) technology. This technology is a second generation solid state imager technology that greatly improves the performance of CMOS image sensors to a level comparable to CCDs [1-3]. Each pixel consists of a photoactive region that is a MOS photogate detector, similar to the structure employed in CCDs. The pixel also contains a transfer gate and a floating-diffusion source-follower output amplifier, similar to those employed in the output stage of a CCD. The output transistor is within the pixel, hence the name active pixel sensor. The in-pixel source-follower converts the photogenerated signal into a voltage. The pixel is addressed by a row select switch, and the output of the transistor is fed to a vertical wire running down the column. The voltage on this column bus is sensed by an amplifier located at the bottom of each column.

The signal is sampled onto a holding capacitor for readout. The per-column signal chain has two capacitors, one for sensing the output of the floating diffusion after reset, and the second for sensing the output following intra-pixel transfer of the signal charge. The two capacitors are buffered by a second source-follower stage that is scanned and selected for readout. The differential output permits correlated double sampling (CDS) of the pixel that suppresses pixel kTC noise, 1/f noise, and fixed pattern noise due to threshold voltage offset. The signal chain is shown in figure 2.

A layout of a photogate CMOS APS pixel is shown in figure 3. As seen in figure 3, the optical fill-factor (percentage of pixel area designed for photodetection) of the APS is approximately the same as an interline CCD (25-30%), but lower than for a full frame CCD. On-chip microlenses are used on interline CCDs to boost the effective optical fill-factor to over 60% and could also be used with the CMOS APS by requiring an additional backend processing step (as is the case for on-chip color filter arrays). JPL has performed intra-pixel laser scanning of its CMOS APS devices and has found that for n-well, n-channel implementations, significant response is obtained in regions not designed for photodetection. Photons generating carriers in these regions are not blocked by polysilicon, and the generated carriers diffuse laterally to the collecting potential well. While this introduces a small amount of crosstalk, the resultant per-pixel quantum efficiency is measured to be close to that of a full frame CCD.

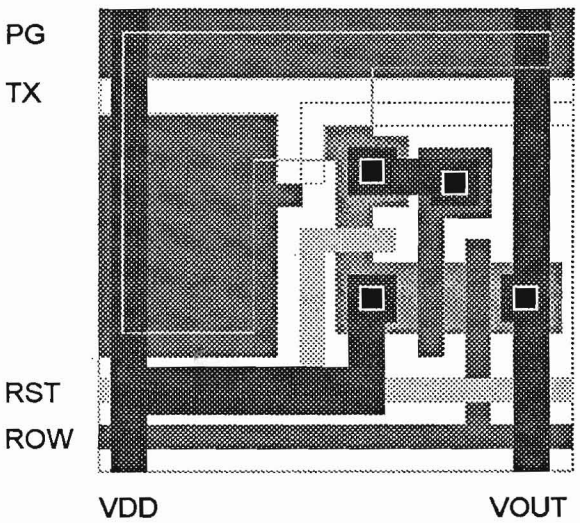

Fig. 3. Typical layout of CMOS APS photogate pixel

An absolute quantum efficiency curve for a CMOS APS implemented with approximately a 25% optical fill factor and no coatings is shown below in figure 4. Note the absence of fringe patterns in the measured quantum efficiency normally associated with CCD overlapping polysilicon gates. Also, the good near infrared (NIR) response of this n-well, n-channel device allows for scientific imaging in this spectral band (0.7-1.0 μm). Improvement in blue/UV response is desired and can be achieved using phosphors (e.g., lumogen) and/or anti-reflection coatings. Improved device design is also expected to boost blue response. The pixel can also be implemented using a photodiode detector structure. The photodiode has the advantage of increased blue response by eliminating the polysilicon overlayer, but has larger capacitance (lower conversion gain, μV/e⁻) and its kTC noise cannot be suppressed on-chip. Thus, the signal-to-noise ratio remains nearly the same as for the photogate implementation, though this structure is simpler to design and operate. A pinned photodiode structure, as that employed in interline CCDs, can be used to suppress kTC noise, but introduces a non-standard CMOS process variation.

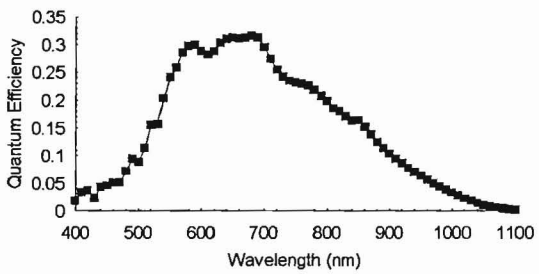

Fig. 4. Measured absolute quantum efficiency in 20 μm CMOS photogate APS pixel (no coatings).

Output-referred conversion gain in the CMOS APS depends on the capacitance of the floating diffusion output node. Typical values are 7 μV/e⁻ (n-well, n-channel), and 3 μV/e⁻ for a photodiode. So-called "full-well" of the APS sensor is determined by the saturation of the signal chain rather than the photogate potential well capacity, and is typically 1.2 V output-referred, or 170,000 electrons for the photogate device. Increasing or decreasing the supply rails results in a change in saturation level of about 0.5 V/V.

Readout noise in the CMOS APS is presently limited by excess noise from the pixel output transistor, though theoretically limited by kTC noise on the sampling capacitors at the bottom of the column. These capacitors are typically 4 pF yielding a theoretical output-referred kTC noise of 45 μV r.m.s. Typical output referred noise levels are 180 μV r.m.s. with 5 V power supply operation, and 100 μV r.m.s. at 3 V power supply operation. Thus, the experimental noise level is typically 25 electrons r.m.s. with 76 dB of dynamic range. Noise as low as 14 electrons r.m.s. has been obtained at 3 V operation. Improvement in these values is expected in the next year.

Room temperature dark current in the CMOS APS is typically 200 mV/sec, or 1 nA/cm^2 -- typical of MOS devices including most CCDs. In the photodiodes, average dark currents an order of magnitude less are typically observed, though the percent fluctuation is greater, as is the incidence of "hot" or white pixels. Cooling is expected to reduce dark current, which is utilized in scientific CCD sensors. The use of non-standard CMOS fabrication steps can be used to reduce dark current to levels comparable to scientific inverted-surface CCDs, but for most commercial applications this is not necessary.

Fixed pattern noise (FPN), often a concern in active pixel image sensors, has been reduced to negligible levels. The D.C. offset variations seen from pixel to pixel has been observed to be comparable to CCDs -- typically 1-2%. The conversion gain/quantum efficiency variations are dominated by column-to-column variations, since threshold offset per pixel is suppressed by the CDS operation. A double-delta sampling (DDS) technique for on-chip suppression of column-to-column variations has been developed at JPL that suppresses column-wise FPN to less than 0.1% sat. -- a nearly unobservable level. Off-chip FPN suppression for removing pixel-to-pixel variations is typically employed in scientific CCD applications (dark frame subtraction) and is readily applicable to CMOS APS sensors.

The voltage-mode, random-access readout of the CMOS APS allows functions not easily implemented using CCDs. The nominal CMOS APS architecture uses row and column decoders for selecting pixels for readout. Window-of-interest readout is easily implemented in the CMOS APS and is useful for star trackers and optical communications. Variable integration periods for different windows can also be achieved -- a function useful for tracking stars of greatly different magnitudes, or for scientific sensors for spectroscopy, where some spectral bands have weak signals. Windowed readout can also be used for electronic panning in large arrays, where a limited instantaneous field of view is desired. Such an approach is useful in surveillance applications.

The voltage mode readout has another large advantage over CCDs. Since CCDs are read out by physically transporting the signal charge to the output amplifier, charge must be transported with nearly perfect charge transfer efficiency (CTE), i.e., no charge can be lost due to traps or spilling en route to the amplifier. For a large number of transfers (e.g. 10,000) the transfer efficiency per transfer must be very high (e.g. 0.999999) so that the net transfer efficiency ($0.999999^{10000} = 0.99$) is reasonable. This high CTE requirement leads to several inherent problems with CCDs. First, CCDs require large clocking voltages (10-15 volts) to maintain high CTE. Secondly, CCD performance degrades with increasing array size unless CTE is increased. Also, CCD performance degrades with increasing readout rate since CTE drops at higher transfer speeds. CCD performance degrades in the presence of trap-inducing radiation (especially protons) and CCD performance degrades at low temperatures due to trapping of signal charge. On the other hand, the CMOS APS technology does not suffer from these limitations.

Power dissipation in the CMOS APS technology is very low. Although column-wise readout requires many source-follower circuits operating in parallel, these circuits are typically biased at 10 μA. These circuits are only activated to sample the data onto the holding capacitors so the duty cycle is low, perhaps 1% or less, depending on array size. Driving analog data off-chip requires a larger bias current to charge cable capacitance at the serial data rate. Only one source-follower is on at a time so that the situation is comparable to a CCD output amplifier. However, in the CMOS APS the amplifier supply voltage is only 3-5 volts (compared to a CCD biased at perhaps 20 volts) so that the CMOS APS dissipates a factor of 4 or more less power. Typical APS power dissipation at serial data rates of 100 kpixels/sec to 1 Mpixels/sec is under 10 mW.

3. ON-CHIP ELECTRONICS

Integration of on-chip electronics leads to an enormous decrease in system power dissipation as well as in system electronics volume and mass. Since radiation shielding of the electronics volume is often required for deep space missions, additional leverage for mass reduction is obtained. CMOS technology has been developed specifically for very large scale integration (VLSI) of microelectronic circuits. Implementation of the image sensor in CMOS enables massive on-chip electronics integration. These electronics include timing and control electronics, and output signal chain. For example, JPL has demonstrated a 128x128 element CMOS APS chip that requires only +5 V power and a master clock to continuously produce video output. The chip has additional digital control input lines for commanding the window of readout (by inputting the addresses of the window boundaries) and for digitally controlling the interframe integration time (by inputting a 32-bit word delay). The chip has integrated per-column CDS circuitry, and integrated DDS circuitry for suppressing column-wise FPN to below 2% sat. The chip was implemented in 1.2 μm CMOS technology through a commercial foundry and has a 19.2 μm photodiode-type pixel pitch.

On-chip analog-to-digital conversion (ADC) can permit a full digital interface, since output data is digital. There are many approaches to on-chip ADC and a full discussion is presented in reference [4]. JPL has demonstrated a small image sensor chip (32x32 elements) with a column-parallel single-slope ADC architecture. The on-chip ADC had 8 bit resolution and operated at 30 frames per second. The ADC was found to have excellent linearity and capable of at least 10 bit resolution (i.e., less than 500 μV noise). Most interesting was the incorporation on-chip ADC reduced on-chip power dissipation from 7 mW to 5 mW. This is ascribed to the power reduction obtained by using digital output amplifiers rather than analog output amplifiers that more than offset the power of the on-chip ADC.

4. FUTURE IMPROVEMENTS

Improved performance through continued R&D is expected in the next few years. Reduction in noise and increased digital resolution through oversampled ADC technology [5] is anticipated. Improved quantum efficiency through the use of optical coatings, backside thinning and smaller CMOS feature sizes is also expected. At the present time, several megapixel-class CMOS APS sensors are being designed for fabrication. Very high speed imaging for large format sensors is also expected to be demonstrated. "Smart sensors" are also expected to be demonstrated through the use of on-chip CMOS signal processing circuits.

5. ACKNOWLEDGMENTS

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6. REFERENCES

1. E.R. Fossum, *Active Pixel Sensors -- Are CCDs Dinosaurs?,* in CCD's and Optical Sensors III, Proc. SPIE vol. 1900, pp. 2-14, (1993).

2. S. Mendis, S.E. Kemeny, R. Gee, B. Pain, and E.R. Fossum, *Progress in CMOS active pixel image sensors,* in Charge-Coupled Devices and Solid State Optical Sensors IV, Proc. SPIE vol. 2172, pp. 19-29 (1994).

3. S.Mendis and E.R. Fossum, *CMOS active pixel image sensor,* IEEE Trans. Electron Devices, vol. 41(3), pp. 452-453 (1994).

4. B. Pain and E.R. Fossum, *Approaches and analysis for on-focal-plane analog-to-digital conversion,* in Infrared Readout Electronics II, Proc. SPIE vol. 2226, paper 24 (1994).

5. S. Mendis, B. Pain, R. Nixon, and E.R. Fossum, *Design of a low-light-level image sensor with an on-chip sigma-delta analog-to-digital conversion,* in CCD's and Optical Sensors III, Proc. SPIE vol. 1900, pp. 31-39 (1993).

Technology 2004, Video/Imaging (1994).