Design of Radiation Hard CMOS APS Image Sensors in 0.35 μm CMOS Standard Process

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ABSTRACT

A CMOS APS image sensor test chip was designed employing the physical design techniques of enclosed geometry and guard ring, and according to the design rules of a 0.35-μm CMOS standard process that has a gate oxide thickness of approximately 7.0 nm. Three sets of radiation tolerant photodiode active pixels were developed employing these design techniques. They are N-type, P-type, and H-type (Hybrid-type) pixels. Each of the pixels is a square pixel with a 16.2 μm pitch. The yielded fill-factor is approximately 50%. Depending on the pixel-type and the layout, the simulated output voltage swing ranges from 300 mV to 1.1 V. The peripheral circuits, which include decoders, row/column drivers, and I/O pads, were also developed. All NMOS transistors in the peripheral circuits were laid out employing the physical design techniques of enclosed geometry and P-type guard ring. Integrating the pixels and the peripheral circuits into the design of radiation hard CMOS APS image sensors has been completed. The size of the pixel array is 256 X 256, constituting an imaging area of approximately 4.1 mm X 4.1 mm. The total size of the die is approximately 5.2 mm X 5.0 mm. The total number of the I/O pads is 42. Plans to irradiate these image sensors using Cobalt-60 to determine the level of their radiation hardness are currently being devised.

1. INTRODUCTION

CMOS Active Pixel Sensor (APS) image sensors are exceptionally well matched to power, mass, and cost constrained applications [1]. A leading and significant set of such applications is space-based applications. However, the CMOS APS image sensor has to be tolerant to radiation to be space qualified. Consequently, it is of foremost importance that CMOS APS image sensors are designed and fabricated to be radiation tolerant. Furthermore, fabricating the radiation tolerant CMOS APS image sensors in standard CMOS processes provides a very valuable cost advantage over other image sensors fabricated in specialized radiation tolerant processes. Image sensors are inherently susceptible to leakage current, which accumulates a charge signal even in the absence of photons (*dark current*). Controlling leakage current, in terms of both background level and uniformity across the array, is fundamental for a standard CMOS foundry to viably fabricate image sensors. Employment of physical design techniques to control a potential source of leakage current has become necessary. Modifications to the CMOS fabrication process to better control leakage current are sometimes required as well.

There has been an increasing interest in radiation hard CMOS APS image sensors. This is evident by the recent publication of research work in this area [2, 3, 4, and 5]. The three major and consequential effects of ionizing radiation on standard CMOS devices are shift of threshold voltages, current leakage in NMOS transistors, and N-channel inter-transistor (isolation field) current leakage. The physical design technique of *enclosed geometry* proved to be very effective for significantly reducing current leakage in NMOS transistors [6 and 7]. The N-channel inter-transistor (isolation field) current leakage was substantially curtailed employing the physical design technique of P-channel guard rings [8].

The magnitude of radiation induced threshold voltage shift is proportional to the number of holes created (and trapped) in the gate oxide due to ionizing radiation. The number of holes created in the gate oxide by ionizing radiation is proportional to its thickness (volume). Therefore, the magnitude of radiation induced threshold voltage shift is smaller for thinner gate oxides.

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For particularly thin oxides (less than 12 nm thick), the radiation induced holes in the gate oxide have a much better chance to tunnel out of the oxide (requiring only 6 nm effective tunneling distance) before their conversion to interface states. Radiation induced threshold voltage shifts for both N- and P-channel transistors was experimentally found to get considerably smaller when the gate oxide is less than 12 nm thick [9], a feature of standard deep sub-micron CMOS technologies such as 0.35-μm technology.

In this paper, the design of a set of radiation hard CMOS APS image sensor test chips is described. This set of test chips was designed employing the physical design techniques of enclosed geometry and guard ring, and according to the design rules of a 0.35-μm CMOS standard process that has a gate oxide thickness of approximately 7.0 nm. The paper has three main sections. In the first one, the design of three sets of radiation tolerant photodiode active pixels is presented. In the second section, the design of radiation tolerant peripheral circuits, which include decoders, row/column drivers, and I/O pads, is described. The integration of the pixels and the peripheral circuits into the design of a set of radiation hard CMOS APS image sensors is presented in the third section, which is followed by conclusions.

2. DESIGN OF RADIATION HARD PIXELS

Three sets of radiation hard photodiode pixels were developed employing the physical design techniques of enclosed geometry and guard rings. They are labeled as N-type, P-type, and H-type (Hybrid-type) pixels. These pixels were designed according to the design rules of a 0.35-μm process that has a gate oxide thickness of approximately 7.0 nm. Each of the pixels is a square pixel with a 16.2 μm pitch.

N-Type Pixels:
The circuit schematic diagram of an N-Type pixel is shown in Fig. 1. Employing the physical design techniques of enclosed geometry and P-channel guard rings yielded a fill factor of approximately 50% for a square pixel with a 16.2 μm pitch. To realize the same fill factor (approximately 50%) without having to use the physical design techniques of enclosed geometry and P-channel guard rings, the pixel pitch would have been approximately 11.0 μm. Thus, the penalty of radiation hardening the N-type pixel was to increase the pixel pitch from 11.0 μm to 16.2 μm, an approximately 2-fold increase in silicon real estate.

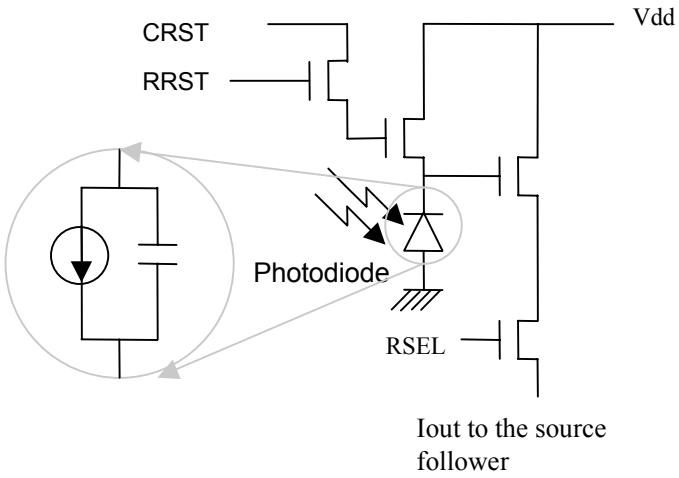

Fig. 1 The circuit schematic diagram of an N-type pixel.

The power supply Vdd is 3.3 V, as opposed to 5.0 V for the first generation radiation hard CMOS APS image sensors that was designed in a 0.50-μm CMOS standard process. Simulation resulted in an output signal voltage swing of 300 mV. A way of improving the output signal voltage swing is to increase the pixel reset level. This was achieved by employing a higher voltage power supply (4.0 V) in the row reset driver, which drives the signal RRST. This resulted in a simulated

output signal voltage swing of approximately 600 mV. Alternatively, a boosting capacitor may be used to provide the higher voltage.

P-Type Pixels:
The circuit schematic diagram of a P-type pixel is shown in Fig. 2. PMOS transistors have the advantage of not having a leakage current path between drain and source, and between transistors. Hence, the design techniques of enclosed geometry and guard ring are not necessary. Consequently, the pixel size can be smaller than that of its NMOS counterpart. However, each pixel needs an additional substrate contact connected to Vdd. The operation of the P-type pixel is similar (but reversed) to that of the N-type pixel. The P-type photodiode has a larger capacitance than that of the N-type one, thus the conversion gain of the P-type pixel is anticipated to be smaller than that of the N-type pixel. Quantum efficiency is also anticipated to be lower than that of the N-type pixel.

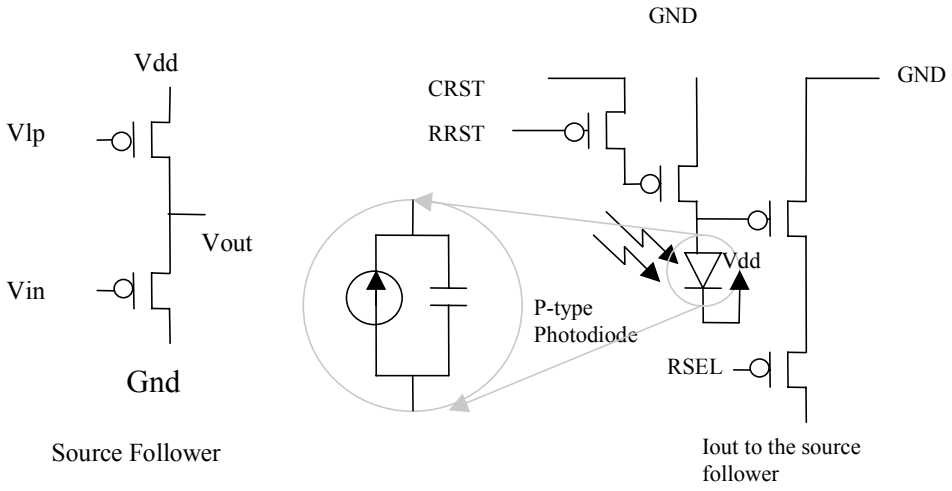

Fig. 2 The circuit schematic diagram of a P-type pixel.

The power supply (Vdd) is 3.3 V. Simulation resulted in an output signal voltage swing of 300 mV. Similar to the N-type pixel, a way of improving the output signal voltage swing of the P-type pixel is to decrease the pixel reset level. This was achieved by employing a lower than ground voltage (-0.5 V) in the row reset driver, which drives the signal RRST. This resulted in a simulated output signal voltage swing of approximately 500 mV. Alternatively, a boosting capacitor may be used to provide the lower than ground voltage. It should be noted that unlike the bodies of NMOS transistors, which are connected together (same substrate), the substrates (bodies) of the PMOS transistors (N-wells) could be of different potential levels. However, this will require the running of additional wire lines across the pixel array, which will adversely affect the photosensitivity of the image sensor by yielding in lower fill factor and quantum efficiency. Also, the breakdown voltage of the diodes in the ESD pads will limit the value of the lower than ground voltage.

H-Type Pixels:
The circuit schematic diagram of an H-type (Hybrid-type) pixel is shown in Fig. 3. The H-type pixel has been conceived in order to realize the combined advantages of the N-type and P-type pixels. The in-pixel transistors are P-type; hence there is no need for enclosed geometry or transistors guard rings. This relaxes the additional requirement on the pixel size imposed by the physical design techniques of enclosed geometry and guard ring. The photodiode is N-type; thus the quantum efficiency and conversion gain can be as high as those of the N-type pixel. The output signal voltage swing of the H-type pixel is anticipated to be larger than that of either the N-type or the P-type pixel. It should be noted that pixels guard rings are still needed to prevent leakage between pixels. The operation of H-type pixel is different from that of the N-type and that of the P-type pixels.

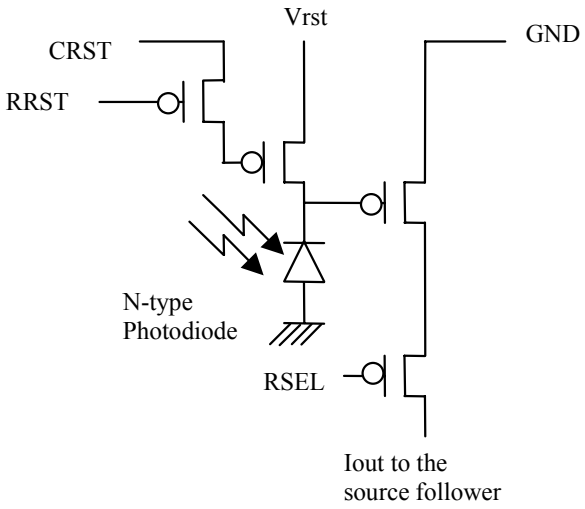

Fig. 3 The circuit schematic diagram of an H-type pixel.

The voltage source Vrst is employed to reset the photodiode to a certain reset level through a PMOS transistor in the saturation region. Consequently, the reset level could be more uniform than that of other type pixels. The voltage source Vrst must be lower than Vdd to avoid the nonlinear region of the P-type source follower output stage at low light levels. As evident from simulation, the output stage for each of the N-type and P-type pixels saturates before the photodiode does. However, the output stage of the H-type pixel saturates after the photodiode does. This translates to a higher output signal voltage swing. A Vdd of 3.3 V and a Vrst of 2.0 V yielded a simulated output signal voltage swing of approximately 1.1 V. This is considerably higher than the corresponding output signal voltage swing for either the N-type or the P-type pixel (600 mV and 500 mV, respectively).

3. DESIGN OF RADIATION HARD PERIPHERAL CIRCUITS

The peripheral circuits include decoder, row/column drivers, and I/O pads. All NMOS transistors were laid out employing the radiation hardening physical design techniques of enclosed geometry and P-type guard rings.

10-Bit Decoder:
The circuit schematic diagram of the 10-bit decoder is shown in Fig. 4, while the layout of one of its cells is shown in Fig. 5. The decoder is 10-bit, anticipating a future expansion of the array format to 1024 X 1024. An enable signal has been designed in to control the output of decoder.

Row Driver:
A different row driver has been developed for each pixel type. As an example, the circuit schematic diagram of the row driver for the P-type pixel is shown in Fig. 6, while its layout is shown in Fig. 7. The row driver provides the row_select and row_reset signals to the pixel array. The row_reset level may be boosted for larger output signal voltage swing as previously described. A reset_all signal has been designed in to simultaneously reset all rows.

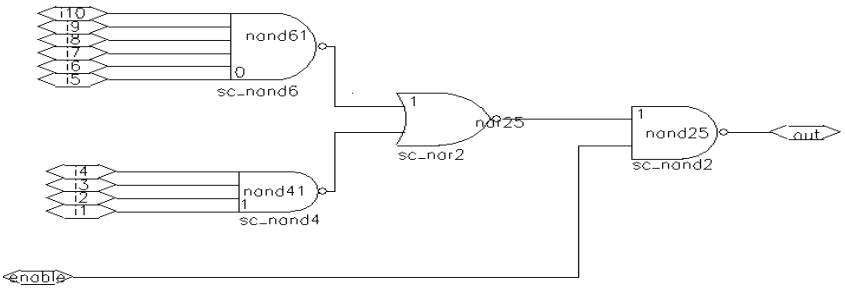

Fig. 4 The circuit schematic diagram of the 10-bit decoder.

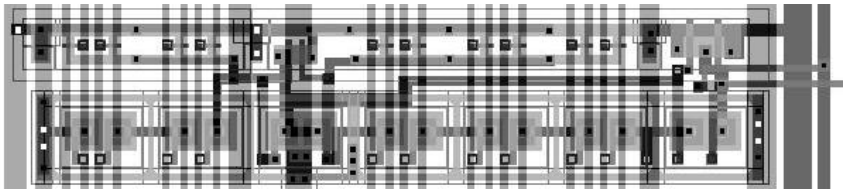

Fig. 5 Layout of one cell of the 10-bit decoder.

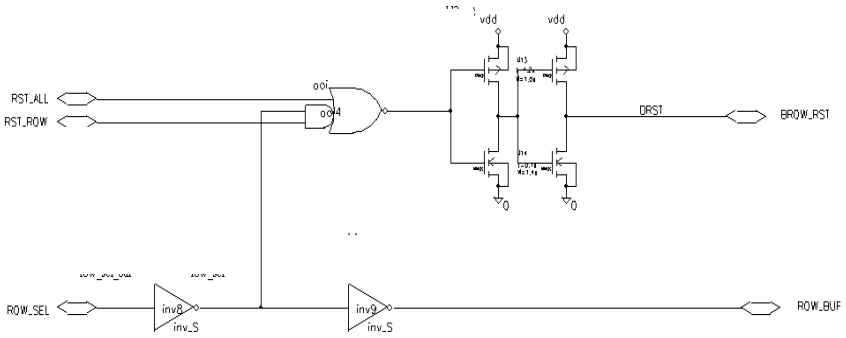

Fig. 6 The circuit schematic diagram of the row driver of the P-type pixel.

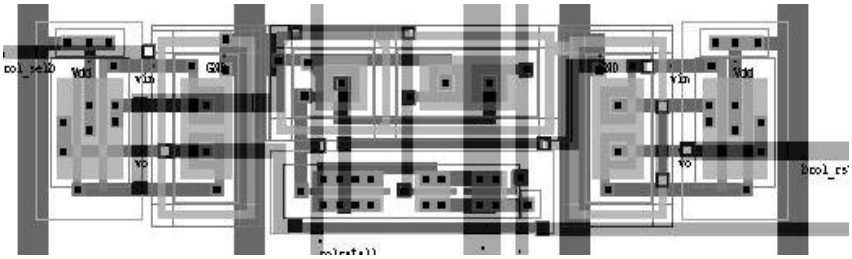

Fig. 7 Layout of the row driver of the P-type pixel.

Column Driver:
A different column driver has been developed for each pixel type. As an example, the circuit schematic diagram of the column driver for the P-type pixel is shown in Fig. 8, while its layout is shown in Fig. 9. The column driver provides the column_reset signal to the pixel array, and multiplexes the output signal out of the pixel array. A reset_all signal is designed in to simultaneously reset all columns.

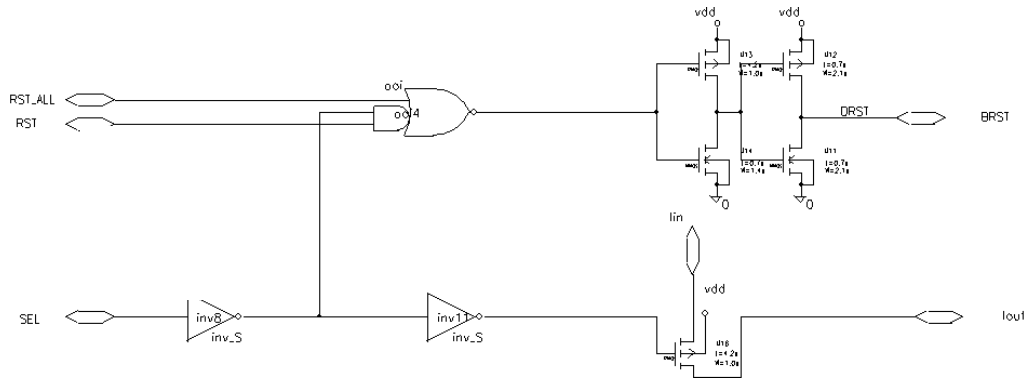

Fig. 8 The circuit schematic diagram of the column driver of the P-type pixel.

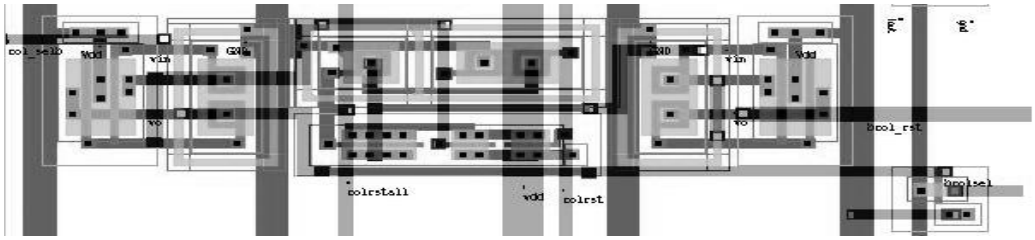

Fig. 9 Layout of the column driver of the P-type pixel.

ESD Power Pad:
The power pads were redesigned to be radiation hard. The ESD protected power pads include digital power supply, digital ground, analog power supply, and analog ground. As an example, the circuit schematic diagram of the digital power supply pad is shown in Fig. 10, while its layout is shown in Fig. 11. It has a large reverse-biased diode that is connected to ground.

ESD Digital Input Pad:
The digital input pads were also redesigned to be radiation hard. A typical ESD protected digital input pad contains a reverse-biased diode that is connected to the power supply, a reverse-biased diode that is connected to ground, and an input buffer. The circuit schematic diagram of the redesigned digital input pad is shown in Fig. 12, while its layout is shown in Fig. 13.

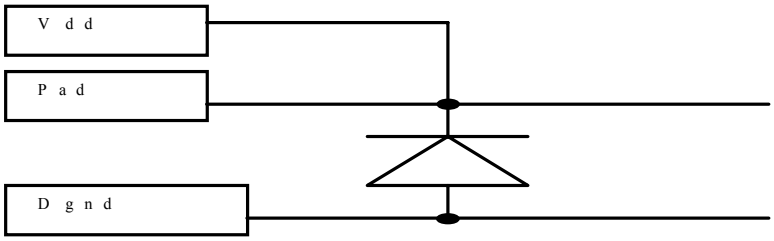

Fig. 10 The circuit schematic diagram of the Vdd pad.

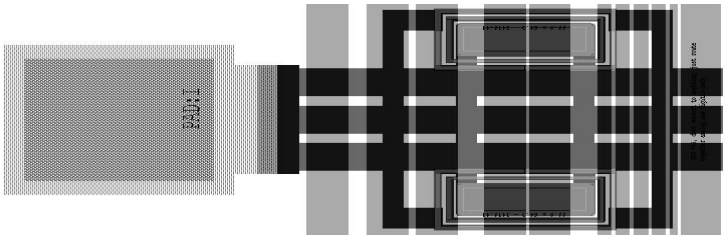

Fig. 11 Layout of the Vdd pad.

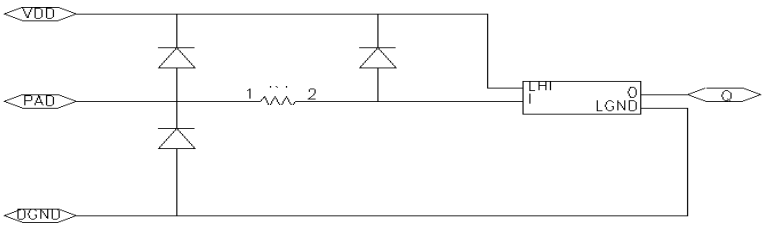

Fig. 12 The circuit schematic diagram of the digital input pad.

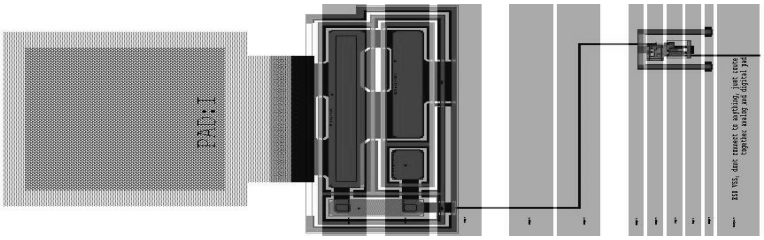

Fig. 13 Layout of the digital input pad.

4. INTEGRATED DESIGN OF RADIATION HARD CMOS APS IMAGE SENSORS

The three different pixel designs described above were compiled into three different pixel arrays. Each of the three arrays contains only one type of pixels: N-type, P-type, or H-type. The size of each of these pixel arrays is 256 X 256, constituting an imaging area of approximately 4.1 mm X 4.1 mm. Each of the three 256 X 256 arrays was divided into 4 sub-arrays, each is 128 X 128. Each of the four sub-arrays has only one of four different pixel layouts, but of the same pixel type. The peripheral circuits were then integrated around each of the pixel arrays. This resulted into three different image sensor test chips that are designed to be radiation hard. The first one employs N-type pixels, the second one employs P-type pixels, while the third and last one employs H-type pixels.

The peripheral circuits were designed to be radiation hard as outlined above. The main peripheral circuits are row and column decoders, row buffers, and an analog circuit processor. The row and column decoders are similar and are used to select the particular row(s) and column(s) of the array that are under consideration at a given time. The windowing function, and the electronic pan and tilt functions can be realized by manipulating the digital inputs of those decoders. The row buffers are used to drive the pixel control signals, such as reset and row select, to the pixels across the array. The analog signal processor is used to drive the output signal voltage level (illuminated level) and the output voltage reset level (dark level) off chip. Pseudo correlated-double-sampling (CDS) is realized on-chip by taking the difference between those two voltage levels.

Each of the three full chips was verified using Design Rule Checking (DRC) and Layout versus Schematic (LVS) techniques. The database was transmitted to a mask house for a mask set generation and then fabrication. The complete physical design of one of the three chips (with the pixel core removed) is shown in Fig. 14. The total size of the die is approximately 5.2 mm X 5.0 mm. The total number of the I/O pads is 42. The bonding diagram of the die pads to the package pads is shown in Fig. 15.

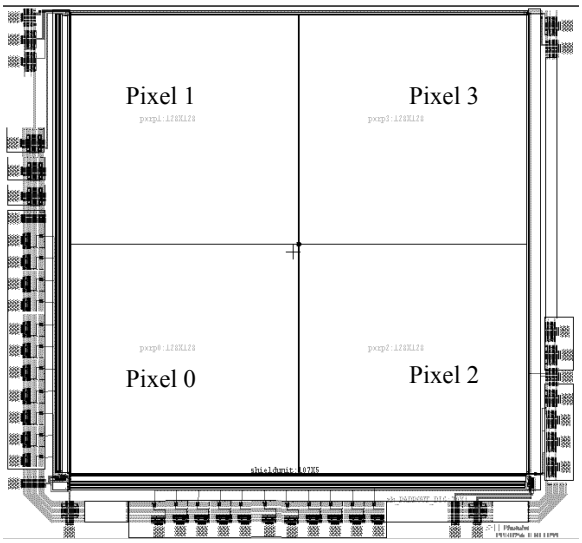

Fig. 14 The physical design of a complete chip (with the pixel core removed) showing the four pixel sub-arrays and the die 42 I/O pads. The total size of the die is approximately 5.2 mm X 5.0 mm.

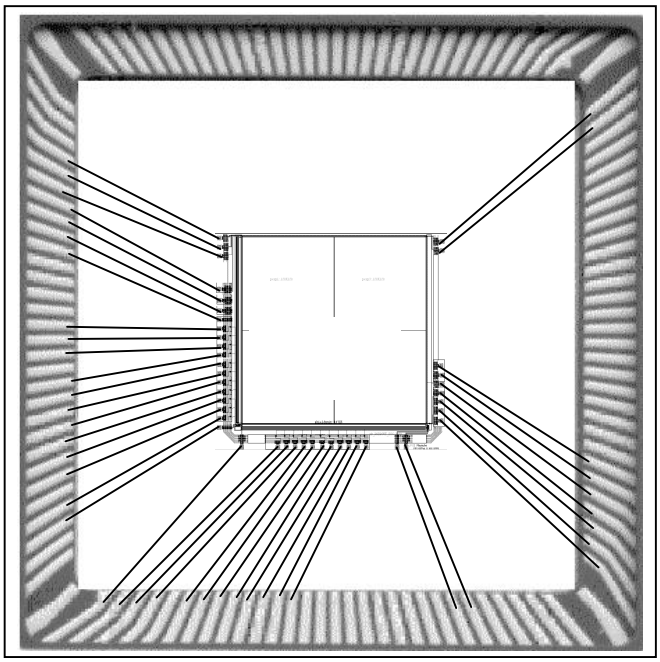

Fig. 15 The bonding diagram of the die I/O pads to the package I/O pads.

5. CONCLUSIONS

A set of three CMOS APS image sensor test chips was designed employing the physical design techniques of enclosed geometry and guard ring, and according to the design rules of a 0.35-μm CMOS standard process that has a gate oxide thickness of approximately 7.0 nm. Three sets of radiation tolerant photodiode active pixels were developed employing these design techniques. They are N-type, P-type, and H-type (Hybrid-type) pixels. Each of the pixels is a square pixel with a 16.2 μm pitch. The yielded fill-factor is approximately 50%. Depending on the pixel-type and the layout, the simulated output voltage swing ranges from 300 mV to 1.1 V. The peripheral circuits, which include decoders, row/column drivers, and I/O pads, were also developed. All NMOS transistors in the peripheral circuits were laid out employing the physical design techniques of enclosed geometry and P-type guard ring. Integrating the pixels and the peripheral circuits into the design of a set of three radiation hard CMOS APS image sensors has been completed. The size of the pixel array is 256 X 256, constituting an imaging area of approximately 4.1 mm X 4.1 mm. The total size of the die is approximately 5.2 mm X 5.0 mm. The total number of the I/O pads is 42. The three test chips are currently being fabricated. Plans to irradiate these CMOS APS image sensor test chips using Cobalt-60 to determine the level of their radiation hardness are currently being devised.

Radiation hard CMOS APS image sensors will be a very favorable and welcome alternative to the inherently radiation soft Charge-Coupled Device (CCD) image sensors for applications in radiation environments. The research work described in this paper concludes that radiation hard CMOS APS image sensors are feasible. The combination of employing the physical design techniques of enclosed geometry and guard ring, and a deep sub-micron standard CMOS fabrication process provides the path to radiation hard CMOS APS image sensors. Utilizing commercial standard CMOS fabrication processes to realize radiation hard image sensors makes every economic sense. The cost element associated with these standard processes is less (by at least a factor of 2) than the cost element associated with specialized radiation hard processes. The completed design of a radiation hard CMOS APS image sensor is the vehicle to test the radiation hard design concepts as they apply to CMOS APS image sensors. The design effort described in this paper proved the feasibility of employing the physical design techniques of enclosed geometry and guard ring in designing a set of radiation hard CMOS APS image sensors.

6. ACKNOWLEDGMENT

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7. REFERENCES

1) E. R. Fossum, "CMOS Image Sensors – Electronic Camera on a Chip," IEEE Trans. on Electronic Devices, Volume 44, Number 10 (1997).

2) G. R. Hopkinson, "Radiation Effects in a CMOS Active Pixel Sensor," IEEE Trans. on Nuclear Science, Volume 47, Number 6 (2000).

3) M. Cohen and J.P. David, "Radiation-Induced Dark Current in CMOS Active Pixel Sensors," IEEE Trans. on Nuclear Science, Volume 47, Number 6 (2000).

4) J. Bogaerts and B. Dierickx, "Total Dose Effects on CMOS Active Pixel Sensors," SPIE Proceedings, Volume 3965, Pages 157-167 (2000).

5) M. Cohen and J.P. David, "Radiation Effects on Active Pixel Sensors," IEEE Proceedings of the Fifth European Conference on Radiation and its Effects on Components and Systems, Pages 450-456 (1999).

6) G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," IEEE Trans. on Nuclear Science, Volume 46, Number 6 (1999).

7) R.C. Lacoe, J.V. Osborn, R. Koga, S. Brown, and D.C. Mayer, "Application of Hardness-by-Design Methodology to Radiation Tolerant ASIC Technologies," IEEE Trans. on Nuclear Science, Volume 47, Number 6 (2000).

8) W. Snoeys et. al., "Layout Techniques to Enhance the Radiation Tolerance of Standard CMOS Technologies Demonstrated on a Pixel Readout Chip," Presented at the Eighth European Symposium on Semiconductor Detectors, Schloss Elmau, Germany (1998).

9) N. Saks, M. Ancona, and J. Modolo, "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides," IEEE Trans. on Nuclear Science, Vol. 33, Number 6 (1986).