Design and operation of self-biased high-gain amplifier arrays for photon-counting sensors

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ABSTRACT

Design and operation of high-gain (>1000), low-power (< 75 μW), ultra low-noise amplifier arrays are presented. The amplifier array is operated in self-biased mode, such that all amplifiers are biased irrespective of threshold mismatches, and operate with low reset noise. The amplifiers are designed for possible incorporation as pixels of hybrid solid-state photon-counting sensor. The cell pitch is 30 μm in 1.2 μm CMOS technology. Design and experimental results from small arrays of the two most promising amplifier circuits are reported. Design issues for obtaining sub-electron input-referred noise from these in-pixel amplifiers are discussed. A performance summary is incorporated.

Keywords: Noise-reduction, IR readout, photon-counting, high-gain amplifier

2. INTRODUCTION

Many space-based telescopes and spectrometers require ultra-low read noise [1] in order to observe a large number of astrophysical phenomena associated with galactic and stellar evolution, high red-shift objects, etc.[2]. Detection of ultra-low light level signals are also required in a large number of environments involving tactical and strategic military applications, such as night vision. Detection of faint objects require either extremely long integration times to build enough signal to be above the system noise floor, or image intensification using photo-multiplier tubes or micro-channel plates (MCP). MCP approach suffers from the ungainly requirements of high voltage (~ 5000V), large mass, high power, high dead-times, small dynamic range, and "scrubbing" for stability [3]. On the other hand, flicker noise often limits the exposure time in a conventional IR readout, limiting delectability of ultra-low level IR signals. In a typical IR detection system, the analog nature of the signal makes it susceptible to noise pick-up along the entire path of the signal chain. The multiplexer noise, consisting of white noise in the MOS transistors and unwanted clock pick-up, is typically around 10-20 electrons in low-noise systems. Multiplexers with sub 10-electron read noise [4] are far and few between, and tend to suffer from a large response non-uniformity and non-linearity.

Detection of faint objects will be greatly enhanced by having readouts with sub-electron read noise. JPL has been exploring a novel approach to ultra-low-noise sensor realization in which the limitation due to read noise can be overcome by counting photoelectrons within each pixel, and generating a one-bit digital signal from each pixel, making the readout system essentially noise free. The sensor has a hybrid structure, similar to conventional IR sensors, with the important difference that the readout chip consists of a novel multiplexer that is sensitive to single photo-electrons. Consequently, such a solid-state IR sensor enables in-pixel photon-counting, greatly enhancing ultra-low light level signal detection capability. Although in-pixel digitization has been previously demonstrated, it is limited to detection of large signal fluxes[5], and are not amenable for solid-state photon-counting.

Figure 1 shows the schematic of a unit-cell of the solid-state photon-counting sensor under investigation, consisting of a photo-diode detector (PD) and cascade of high-gain amplifiers with gains A1 and A2. The readout multiplexer senses the change in the voltage at the capacitance (C_{in}) of the hybrid bump bond (that includes the detector capacitance, bump-to-readout circuit capacitance, sense transistor gate capacitance, and parasitic capacitance) in order to detect the presence of photoelectrons.

The circuit operates as follows. The photo-detector is reset using the switch (ϕ_{rst}) to bias it in the integrating mode. A photo-electron generated at the photo-diode, changes the potential at the input capacitance C_{in}. This potential is buffered by

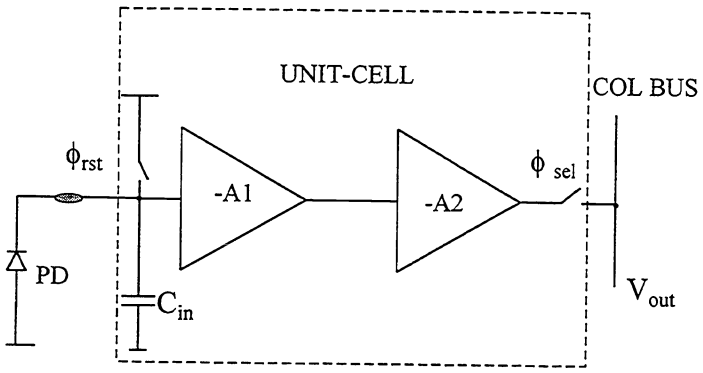

Figure 1 Schematic of the unit-cell of a photon-counting sensor

the high-gain amplifiers to cause a large voltage change at the output of cell, which is subsequently read out by selecting the relevant cell with the clock ϕ_{sel}. The unit-cell amplifiers are of high enough gain and low enough noise that the voltage change at the column (ΔV_{out}) is sufficient to allow discrimination between presence or absence of photoelectrons. Since, the gain stages are required for boosting the signal enough to allow proper thresholding, gain uniformity is not a concern. Thus, the pixel readout circuit permits counting of individual photoelectrons to produce a digital output proportional to the incident photon flux, and enable accurate ultra-low light level signal detection.

The critical component in this sensor is the high-gain, ultra-low-noise, self-biased amplifier array that enables solid-state photon counting with a high degree of spatial resolution, and a large dynamic range. In this paper, the design and operation of these amplifiers is presented. In section 3, the design requirements of the amplifiers are presented, followed by the design of two different topologies of amplifiers. In section 4, measurement results from these amplifiers are presented and discussed. In section 5, low-noise design considerations for different in-pixel amplifiers are presented.

3. DESIGN OF THE IN-PIXEL AMPLIFIERS

3.1 Design requirements

The photon-counting readout requires an extremely novel pixel design consisting of amplifiers that exhibit the following characteristics: low-power (< 100 μW per pixel during readout), high charge-to-voltage conversion gain (> 1 mV/e^-), low-noise (< 1 e^-), small cell pitch (< 30 μm), easy scalability (to 10 μm), self-biasing capability, sufficient gain uniformity (~ 10%) for multiple event discrimination, and bias current programmability. Biasing a high-gain circuit poses a considerable challenge due to the inherent threshold mismatches in MOS transistors implemented in VLSI technology. Self-biasing capability is required to ensure that all the pixel amplifiers remain biased in high-gain mode, in presence of typical threshold mismatches of 10-20 mV. Total read noise consists of white noise and 1/f noise in the MOSFETs, as well as the so-called reset noise. Since correlated double-sampling readout cannot be generally used in this scheme for elimination of reset noise, the amplifier circuits require to feature built-in reset noise reduction. A high charge-to-voltage conversion gain generally requires high voltage gain, typically around 60 dB. In section 4, the voltage gain requirements will be further reviewed. Although, gain uniformity is not critical, a high degree of gain uniformity is desirable, since this allows incorporation of multi-bit digital converter incorporation.

3.2 Design and operation of self-biased gain stages

The schematic of the unit-cell amplifier circuit with built-in dummy-switch compensated self-biasing is shown in figure 2. The in-pixel amplifier consists of a two-stage cascade of self-biased, cascode gain stages. The MOS transistors MipC, McasC, and MlnC form the first cascode gain stage, with McasC acting as the cascode transistor. The first stage is designed with a nominal gain of 37 dB, and is cascaded to a similar but lower gain stage (gain ~ 25 dB) that drives the column bus. In-pixel cascoding allows minimization of coupling capacitance between input and output, thereby increasing the sensitivity of the circuit.

The amplifier operates as follows. First, the amplifier and the detector connected to its input are reset by pulsing ϕ_{rst}. Reset is followed by self-biasing phase during which the output of each stage (V_{out1}, V_{out2}) are set to a d.c. level such that all the transistors operate in saturation mode, ensuring high-gain from the amplifiers. This is carried out by pulsing ϕ_{c1} high

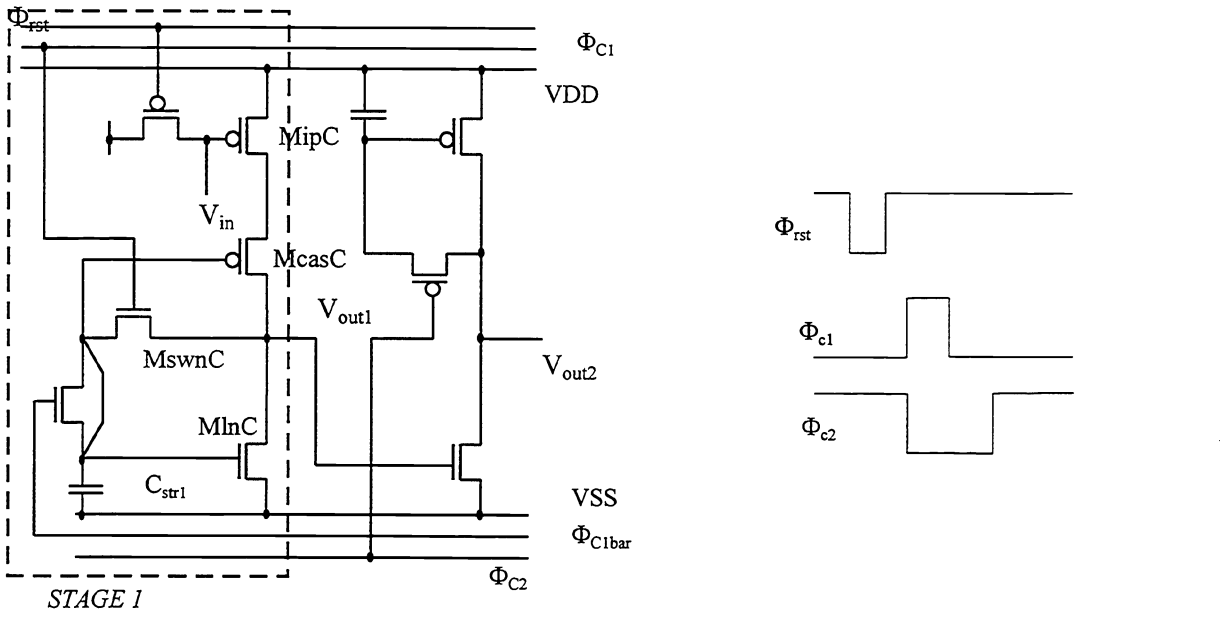

Figure 2 **Schematic of a two-stage dummy compensated self-biased amplifier with associated clocking diagram**

during which MlnC operates with its gate and drain shorted together. This results in the gate of MlnC to be charged up to the voltage necessary to maintain all MOSFETs of stage 1 (MipC, McasC, MlnC) to operate in saturation. When ϕ_{c1} goes low, the load bias generated during the self-biasing phase is frozen on the capacitance C_{str1}, and the first amplifier stage is biased in high-gain mode. To suppress biasing errors due to switch-feedthrough from MswnC while it is being shut-off, a dummy transistor compensation is used [6]. The second stage is self-biased in a similar fashion by pulsing ϕ_{c2}.

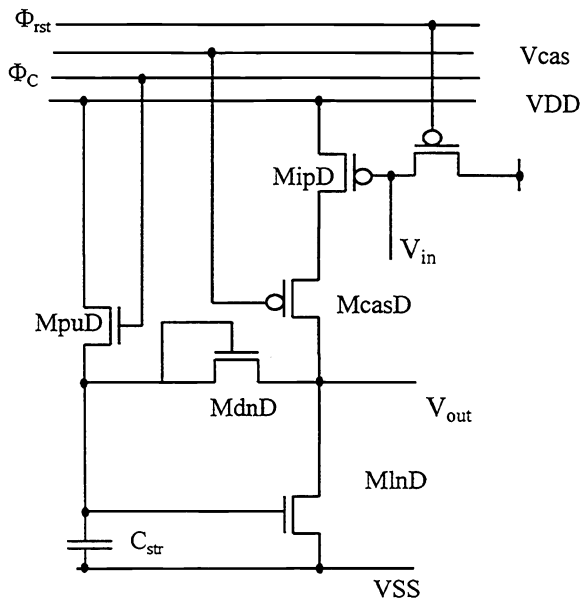

Figure 3 **Self-biased amplifier with diode shut-off switch**

The self-biasing circuitry enables proper biasing despite the threshold mismatches and variations in the input reset level. As a result, it allows amplifier operation with reduced reset noise, variation in the output reset level being dependent on the larger storage capacitance (C_{str1}) instead of the smaller input capacitance (C_{in}). The first stage output-referred reset noise is approximately given by:

$$\left\langle v_{rst}^2 \right\rangle = \frac{kT}{C_{str1}}\left(1 + \frac{1}{g_{mlnC}\,R_{sw}}\right) \qquad (1)$$

where g_{mlnC} is the transconductance of MlnC and R_{sw} is the ON-resistance of MswnC. Typically, $g_{mlnC}.R_{sw}$ is much less than unity and the reset noise is determined primarily by C_{str1}. From equation 1, the value of C_{str1} is chosen to ensure that the reset noise is much less than the voltage step due to single electron input. The choice of C_{str1} represents a compromise between cell size, speed of operation, and noise, and is designed to be 350 fF.

The resultant dimensions of the two-stage amplifier is 48 μm X 51 μm in 1.2 μm CMOS technology.

A second implementation of the high-gain stage incorporates a novel and simpler self-biasing scheme. This gain-stage features reduced cell size, fewer clocks, more reliable biasing, and faster biasing speeds. The self-biasing scheme consists of a diode-shut off switch, implemented with a gate-to-drain shorted MOSFET. A schematic of the pixel with a single-stage amplifier is shown in figure 3. This gain stage shown can be cascaded to a similar gain stage to realize a pixel with a two-stage amplifier. The self-biasing stage requires only one clock ϕ_c. In order to carry out self-biasing, ϕ_c is pulsed high momentarily to pull the node V_b high, while the output of the stage (V_{out1}) remains at a low voltage, causing MdnD to be turned ON. When ϕ_c goes low, the node discharges through the same transistor (MdnD) till no current flows through it. The current flow stops when the node V_b, which is also connected to the gate of the load transistor (MlnD), is at a potential that supports the bias current flow through the amplifier. As with the previous circuit, all transistors are in saturation at this stage, and the resultant V_b is the optimal load bias. The switch-feedthrough from MlnD is minimal because of the inherent self-limiting nature of transistor shut-off. With C_{str} ~ 350 fF, the cell size of the two-stage amplifier is 36 μm X 36 μm in 1.2 μm CMOS technology.

4. EXPERIMENTAL RESULTS AND DISCUSSION

4.1 Test chip architecture

Several chips with a variety of different unit-cell circuits were designed and tested for a parametric understanding of the operation of the pixel. The chips were fabricated using Hewlett-Packard 1.2 μm CMOS technology through MOSIS. A small photo-diode (with effective detector capacitance of 36 fF) was monolithically integrated in each pixel in order to allow measurement of response of the pixels to charge input. The chip photograph of the pixel consisting of a self-biased amplifier with diode shut-off switch is shown in figure 4. The pixel area (without the test photo-diode) is highlighted by a rectangle with white borders. The power and the GROUND buses can be identified from the thick metal lines running horizontally. The self-biasing capacitance (C_{str}), seen as a rectangle under the VDD line, takes up only a tiny fraction of the total cell area.

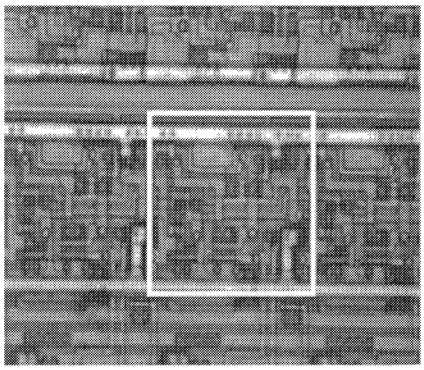

Figure 4 **Chip photograph of the pixel with self-biased amplifier**

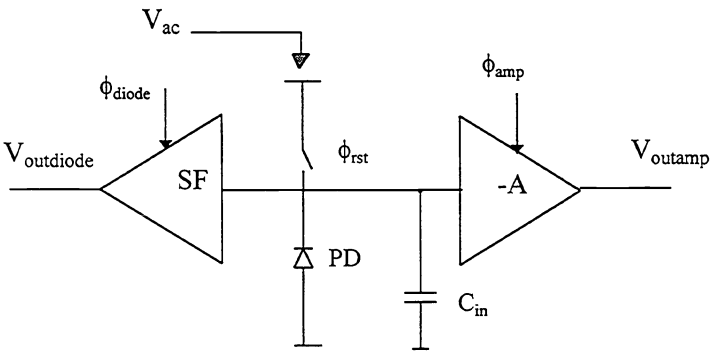

Figure 5 **Schematic of test-chip pixel for measurement of response to voltage and charge inputs.**

The test circuit consists of additional circuitry to facilitate measuring response of the circuit to voltage and charge inputs. Figure 5 shows the schematic of the test-chip pixel. It consists of the high-gain amplifier of voltage gain A, the test photo-diode (PD), and a source follower (SF) to buffer the test diode. The diode can be reset using ϕ_{rst}. A small a.c. signal can also be input through the reset switch to measure the voltage response. Selection switches ϕ_{diode} and ϕ_{amp} determine whether the source follower or the amplifier is selected for readout. The measurement was carried out from a 32 element linear array of high-gain pixels.

4.2 Voltage-gain measurement

All measurements of the pixel circuits were carried out at room temperature. An oscilloscope photograph of the voltage input and output traces of a single-stage self-biased amplifier cell with diode shut-off switch is shown in figure 6. The dip in the output trace coincides with the clock ϕ_c (shown in figure 3) being pulsed, and indicates the effect of the self-biasing operation. The output is pulled low during the self-biasing phase in order to maintain the total current flow through the load transistor. Once ϕ_c goes low, the output is restored to the appropriate bias level as demonstrated in figure 6.

The amplifier cell is biased with a current of 15 μA. The input a.c. signal is a 20 mV signal (top trace), resulting in a output of 1V p.p. a.c. signal (bottom trace). The pixel is buffered with a two-stage source follower pad-driver with gain of 0.65, so that the actual voltage gain (A_{v1}) from the cell is 76.9. Typical single-stage voltage gain was measured to be in the range of 60-100, depending upon bias current and input transistor sizes.

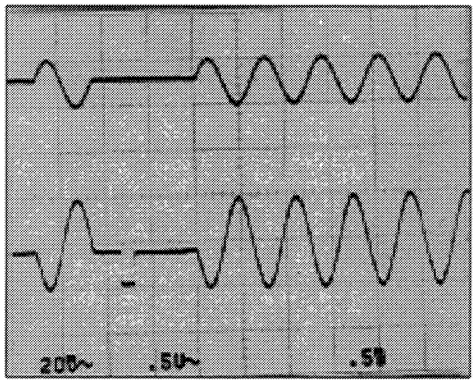

Figure 6 Oscilloscope trace of input and output from a single self-biased gain stage

Both amplifier circuits were operated over a large range of bias currents spanning from 0.5 to 50 μA. Self-biasing and high-gain were obtained over the entire range of currents, although the self-biasing time increased to more than 20 μsec. for currents smaller than 1 μA. The measured voltage gain reduces with increasing bias current, the gain reduction depending nearly as the square-root of the current. This is because the output resistance diminishes at a faster rate than the rise in the transconductance with an increase in the bias current.

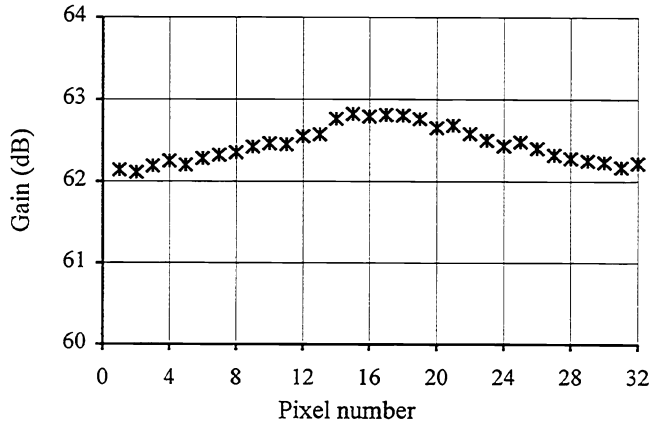

Figure 7 Measured pixel-to-pixel voltage gain uniformity

The pixel-to-pixel gain non-uniformity measured from a 32x1 linear array of self-biased amplifier with diode shut-off switch is shown in figure 7. A high degree of pixel-to-pixel gain uniformity was achieved for both self-biasing designs, measured gain non-uniformity being less than 8% even for average pixel voltage gains as high as 62 dB, as shown in figure 7. Improved gain matching (< 3%) is observed from single gain stages.

4.3 Charge-mode measurement

For measurement of response to charge input, photo-charge was created by shining light on the photo-diode, causing the net detector capacitance (C_{in} ~ 36 fF) to discharge at the rate of 1V/10 msec, and the resultant voltage swings at the output of the amplifier and the source follower buffer were measured independently by selecting either ϕ_{amp} or ϕ_{diode} respectively. If ΔV_{outamp} is the swing at the output of the pixel with the self-biased amplifier, ΔV_{outdio} is the swing at the output of the diode for the same charge (Δq) input from the photo-detector, and A_{sf} is the source follower small signal gain,

then the charge-to-voltage conversion gain (S_{pix}) of the pixel can be calculated as:

$$S_{pix} = A_{sf}\left(\frac{\Delta V_{outamp}}{\Delta V_{outdio}}\right)\left(\frac{C_{det}}{q}\right) \tag{2}$$

S_{pix} was found to be strongly dependent on the voltage gain of the pixel amplifier, tending to level out only for voltage gain (A_v) greater than 200. A maximum charge-to-voltage conversion gain of 170 $\mu V/e^-$ was measured at $A_v = 250$. The dependence of S_{pix} on the voltage gain is due to the presence of a small but inevitable parasitic capacitance (C_p) between the input and the output node, which forces the high-gain circuit to behave as a capacitive transimpedance amplifier (CTIA) in response to charge input. The charge-to-voltage conversion gain can then be calculated from the well-known expression for CTIA response, and is then given by:

$$\Delta V_{out} = \frac{q}{C_p + \frac{C_p + C_{in}}{A_v}} = \frac{q}{C_{eq}} \tag{3}$$

Figure 8 shows the measured voltage swing at the pixel output due to a fixed charge input with different amplifier voltage gains. The individual dots in figure 8 represent the measured voltage swings as a function of the in-pixel amplifier voltage gain, and the solid line represents the expected response assuming a CTIA front-end with $C_p = 0.805$ fF, and $C_{in} = 36$ fF. The predicted response is well in agreement with the measured data. The parasitic CTIA mode of operation underscores the importance of keeping the capacitive coupling between the input and output low, and hence the importance of having a cascode front-end. The measurement also indicates that a high voltage gain (> 100) is not required for obtaining a high charge sensitivity, since the response is limited by the parasitic coupling capacitance. This is especially true for pixels with smaller input capacitance, allowing further simplification of the in-pixel amplifier circuitry and enabling a reduction of the cell size.

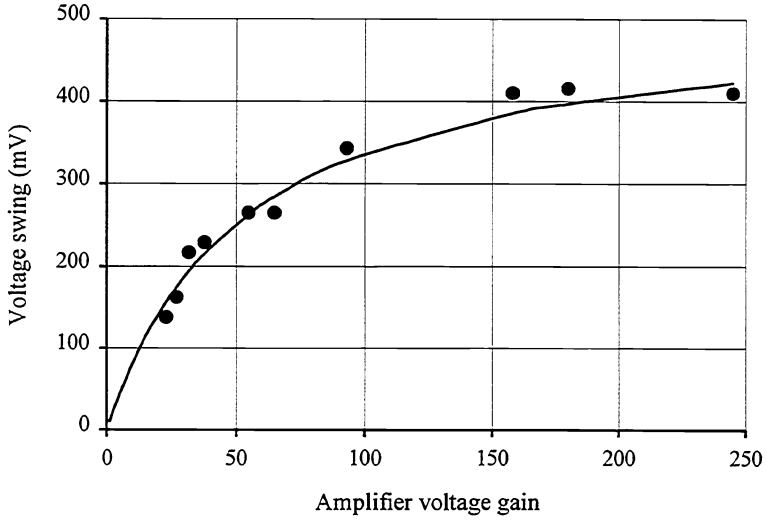

Figure 8 **Measured output swing (for a fixed charge input) of a pixel with a single-stage amplifier as a function of the voltage gain**

Noise in these circuits were measured by calculating the standard deviation of the difference of two output samples separated by a short time τ (~ 100 μsec.), while the amplifier was operating in high-gain mode under dark condition. In the two designs, input-referred noise of 3-4 electrons has been measured, which is slightly higher than the theoretical prediction of 2-3 electrons r.m.s. The cause of the excess noise is expected to be flicker noise, reduced power supply rejection, and clock pick-up noise.

A summary of the performance of different unit-cells is provided in table 1. The performance summary indicates that low-power, high-gain, self-biased amplifier arrays with small cell-size and ultra-low-noise levels are possible, and have been demonstrated for the first time. Although gain uniformity is not a concern, these amplifiers exhibit excellent gain uniformity, possibly enabling photon-counting with increased dynamic range. The table reports only the peak power, whereas the average power/pixel is much less, since the pixels consume power only when they are read out.

CHIP NAME	PHT1095	PHT1095	PHT1095
Self-bias type	dummy switch compensation	diode shut-off switch	diode shut-off switch
# of gain stages	2	2	1
Technol. (name, μm)	HP, 1.2	HP, 1.2	HP, 1.2
# of MOSFETs/cell	10	10	6
# of bias clocks	4	2	1
Array Format	64x1	64x1	64x1
Cell size (μmxμm)	48x51	36x36	28x28
Peak Power (μW)/cell	75	75	35
Voltage Gain (dB)	63.0	59.3	34.8
Max. Gain variation (%)	7.8	7.1	3.2
Noise (mV)	5.6	6.8	0.39
Estimated NEQ (elect.)	4.6	3.7	3.05
Self-biasing speed (μs)	5.0	2.5	2.0

Table 1 **Performance summary of the self-biased in-pixel amplifiers**

5. LOW-NOISE DESIGN CONSIDERATIONS

There exists a trade-off between readout unit-cell designs with two-stage and single-stage in-pixel amplifiers. A single-stage high-gain in-pixel amplifier behaves as a CTIA. The cell size is small, since only one stage amplifier is incorporated. However, the output voltage swing for a single electron input is also small, limited to around 200 μV by the sub-fF parasitic input-to-output coupling capacitance. The small signal swing makes this design more susceptible to down-stream noise pick-up. In the single-stage architecture, the output of the amplifier drives the entire column bus line, as a result of which the amplifier needs to be biased at a higher current levels, and consequently the sensor power requirements are higher.

The two-stage design allows the flexibility of independent optimization of the front-end and the column drive circuitry, enabling lower power, faster speed, and lower noise, at the expense of increased cell size. The two-stage design allows increased voltage swing (~ 2-4 mV/e^-) in response to a single electron input, as a result of the buffering gain from the second amplifier stage. The second gain stage has smaller voltage gain (~ 10-20), since it is required to drive the column-bus as well. However, in comparison with the single-stage design, a 10-20 fold increase in signal swing can be achieved.

Another parameter important for the pixel design is the total noise, measured in input-referred noise. Reduction of input-referred noise requires lowering of the effective input capacitance. Since the pixel readouts operate in a parasitic CTIA mode, reduction of noise requires lowering of both input capacitance and feedback capacitance, the noise being proportional to the square-root of the sum of the two [7].The input-referred noise in electrons of the two designs can be expressed as:

$$\left\langle N^2 \right\rangle_{stg1} = \frac{1}{q^2}\left[\frac{kT}{C_{load}}\left(1+\frac{g_{ml}}{g_{mi}}\right)\left(C_i+C_p\right)C_{eq} + V_F^2\left(C_i+C_p\right)^2\left(1+\pi^2 f_c\tau\right)\right] \quad (4)$$

$$\left\langle N^2 \right\rangle_{stg2} = \frac{1}{q^2}\left[\frac{kT}{C_{load}}\left(1+\frac{g_{ml}}{g_{mi}}\right)\left(\frac{g_{o2}}{g_{mi}}\right)\left(C_i+C_p\right)^2 + V_F^2\left(C_i+C_p\right)^2\left(1+\pi^2 f_c\tau\right)\right] \quad (5)$$

where N_{stg1} and N_{stg2} are the input-referred noise electron for the single and the two-stage design respectively. g_{ml} and g_{mi} are the respective transconductances of the load and the input transistor,, and g_{o2} is the output conductance of the second-stage. C_{load} is the column load capacitance the pixel drives, C_{qe} is the equivalent CTIA capacitance of the front-end, V_F is the gate-referred flicker noise voltage at 1 Hz, f_c is the cut-off frequency of the pixel, and τ is the correlation time constant.

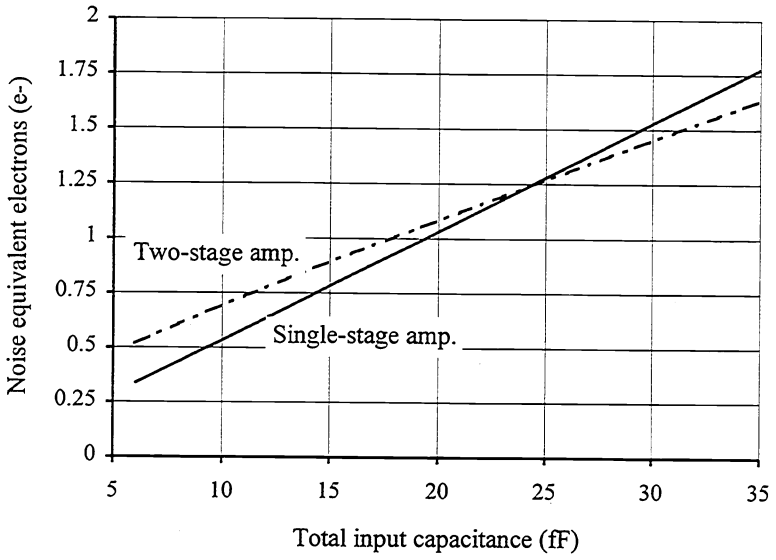

Figure 9 **Simulated input-referred noise electrons for two in-pixel amplifier architectures as a function of input capacitance**

The first term in the expression is due to white noise, and the second one is due to flicker noise.

Figure 9 shows the simulated input-referred noise (using equations 4 and 5) for both the design approaches as a function of different input capacitance. Input-referred noise of the two-stage design falls off faster than the single-stage design. This is due to the fact that in a two-stage design, the second-gain stage can be used to carry out noise shaping by appropriately choosing the bandwidth. As a result, for smaller input capacitance, a two-stage design can yield extremely low-noise. Figure 9 indicates that sub-electron read noise at room temperature is possible for input capacitance of less than 20 fF.

6. CONCLUSION

In summary, novel low-power, high-gain, self-biased amplifier arrays with small cell size and ultra-low-noise levels are demonstrated. These amplifiers are small enough in cell size and power requirements to be used as pixels for solid-state photon-counting sensors. Operation of two amplifier designs with different self-biasing circuits are presented. The self-biasing circuitry ensures proper biasing even for pixel voltage gains greater than 62 dB. It was found that the charge-to-voltage conversion gain depends on the parasitic coupling capacitance between the input and the output of the pixel, causing the front-end to behave as a CTIA. As a result, voltage gains larger than 40 dB are not required to realize a high charge sensitivity. Reduction of the coupling capacitance through improved circuit layout will lead to even higher charge-to-voltage conversion gain. Measured noise from the existing linear array of these amplifiers is between 3-4 electrons, and is limited by the size of the test detector capacitance. Simulations indicate sub-electron read noise capability for smaller detector capacitance.

7. ACKNOWLEDGMENTS

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