Deep Cryogenic Noise and Electrical Characterization of the Complementary Heterojunction Field-Effect Transistor (CHFET)

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***Abstract*—This paper discusses a characterization at 4 K of the complementary heterojunction field-effect transistor (CHFET), to examine its suitability for deep cryogenic (< 10K) readout electronics applications. The CHFET is a GaAs-based transistor analogous in structure and operation to silicon CMOS. The electrical properties including the gate leakage current, subthreshold transconductance, and input-referred noise voltage were examined. It is shown that both n-channel and p-channel CHFET's are fully functional at 4 K, with no anomalous behavior, such as hysteresis or kinks. Complementary circuit designs are possible, and a simple CHFET-based multiplexed op-amp is presented and characterized at 4 K. The noise and gate leakage current of the CHFET are presently several orders of magnitude too large for readout applications, however. The input-referred noise is on the order of $1\,\mu V/\sqrt{Hz}$ at 100 Hz for a $50 \times 50\,\mu m$ n-channel CHFET. The gate current is strongly dependent on the doping at the gate edge, and is on the order of 10^{-14} A for a $10 \times 10\,\mu m^2$ n-channel CHFET with light gate-edge region doping.**

I. Introduction

FUTURE imaging instruments for very long wavelength infrared (VLWIR) will use detector arrays cooled to deep cryogenic temperatures (below 10 K), and will require readout electronics that operate at the detector temperature. For previous cryogenic arrays of only a few pixels, it had been possible to isolate the electronics in a warm compartment and run wires to each detector in the array. The large heat load carried by these wires, and their susceptibility to crosstalk and noise pickup makes this approach impractical for the larger formats planned for future space-based VLWIR imagers. For this reason, NASA has actively been exploring readout electronics which can be functional below 10 K. Typically, VLWIR detectors have very high impedance and low dark currents, so the readout input currents must be low. Also, the expected signals are small, requiring low amplifier noise to preserve the sensitivity. For example, the Space Infrared Telescope Facility (SIRTF) plans to use detectors cooled to 2 K that will require amplifiers with less than 10^{-17} A input current, and a noise of less than 100 $nV/\sqrt{Hz}$ at 0.1 Hz. Unfortunately, there is no existing technology which is entirely suitable for this application.

This is in contrast to the situation for the more commonly encountered cryogenic temperatures which are attainable with liquid nitrogen, that is, above 77 K. In fact, many types of transistor technologies have their optimum performance in this temperature range, and the cryogenic performance of transistors above 77 K has been widely explored. Most types of transistor technologies, however, exhibit severe performance degradation or complete device failure between 77 K and 10 K, making it a challenge to find transistors that work at all below 10 K. Therefore, the deep cryogenic temperature range below 10 K is qualitatively different than above 77 K, and studies of the performance above 10 K are usually not applicable to deep cryogenic operation.

The cause of the performance degradation at deep cryogenic temperatures is the phenomenon of carrier "freeze out." In semiconductors that are not heavily doped, it requires a small but finite amount of energy to liberate carriers from the dopant atoms. At sufficiently low temperatures, the carriers lack the thermal energy required to remain free, and "freeze out" by being recaptured by the dopant atoms. This results in performance degradation such as hysteresis and excess noise, or even complete device failure. A semiconductor can be made immune to freeze out by doping it degenerately, that is, doping to such a high concentration that the dopant atom states merge with the free carrier bands, but for some types of transistors and semiconductor materials the degenerate concentration is too high for proper device operation. Freeze out is highly technology dependent, but the most important material parameter relevant to freeze out is the carrier effective mass: semiconductors that have a light effective mass freeze out at lower temperatures, and it requires a lower doping concentration to make the semiconductor degenerate. Conversely, semiconductors with a heavy effective mass freeze out at higher temperatures and it requires higher doping concentrations to make the semiconductor degenerate.

Silicon is the most highly developed material for integrated electronic circuits, but its relatively large effective mass results in poor performance at deep cryogenic temperatures. Lightly doped silicon freezes out well above 10 K, and it requires doping concentrations on the order of 10^{19} cm^{-3} to make it degenerate. Conventional silicon bipolar transistors and junction field-effect transistors (JFET's), which require moderately

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doped layers, fail completely at some temperature above 40 K. Conventional silicon MOSFET's using degenerately doped source and drain regions can operate normally down to about 20 K, by inducing charge into the frozen channel by the gate voltage. Below 20 K, they become very noisy and exhibit anomalous behavior such as hysteresis and kinks.

Since conventional silicon integrated circuit technology is unsuitable for deep cryogenic readout applications, a development effort is required. One path is to modify the existing silicon MOSFET technology to improve the performance below 10 K. This has been undertaken first at TRW [1], and is underway at Hughes and Orbit. A second path is to develop a cryogenic circuit technology in another material system, such as GaAs. GaAs is naturally well suited to deep cryogenic applications because of the very light electron effective mass. Several groups have explored of the deep cryogenic properties of GaAs transistors for cryogenic readout electronics applications [2]–[9]. For example, R. Kirschman *et al.*, have studied commercial and foundry GaAs JFET's and metal-Schottky field-effect transistors (MESFET's) at 4 K [2]–[4]. Camin, *et al.*, have tested GaAs-based MESFETs for use in particle detectors below 4 K [5]. Also, Kozlowski *et al.*, have designed GaAs-based circuits for low temperature readouts [6].

JPL has been studying GaAs-based electronics for readout electronics applications in the 2-4 K temperature range. This has included an investigation of the low-temperature properties of a type of CMOS-like GaAs-based transistor called the complementary heterojunction field-effect transistor (CHFET). The CHFET was developed by Honeywell for high-speed, room-temperature digital applications [10], and allows CMOS-like design and integration capability. Although optimized for room temperature operation, it has several features that indicate that it might retain good performance at deep cryogenic temperatures. Consequently, the properties of the CHFET have been examined at 4 K in order to determine whether it could be used in deep cryogenic readout applications. A characterization of the CHFET including the current-voltage characteristics, gate leakage current, and noise voltage are presented in the following sections.

II. The Structure of the CHFET

A cross section of the CHFET is shown in Fig. 1 Except for the doping, the structure is the same for both n-channel and p-channel CHFET's. Starting on a semi-insulating GaAs substrate, molecular beam epitaxy (MBE) is used to grow a GaAs buffer layer, an InGaAs channel layer, a high aluminum mole-fraction AlGaAs dielectric layer, and a thin passivating GaAs cap layer. As grown, all of the layers can be undoped. A WSi gate is then deposited, and the source and drain implants are made, self aligned by the gate. The implants are n-type for n-channel transistors and p-type for p-channel transistors. The CHFET is completed by adding ohmic contacts for the source and drain, and by isolating the transistor using an isolation implant. The CHFET operates in enhancement mode in a manner completely analogous to that of silicon CMOS, with the AlGaAs layer playing the role of the oxide. A gate

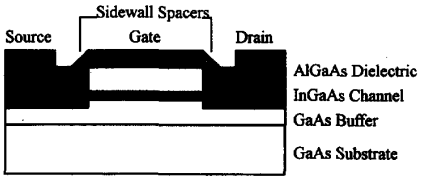

Fig. 1. A cross section of the complementary heterojunction field effect transistor (CHFET).

voltage draws electrons or holes into the channel where they are confined by the AlGaAs dielectric. The carriers move laterally, and are collected by the drain.

It is possible to fabricate the CHFET so that every part is either undoped or degenerately doped, which will make it completely immune to freeze out. The actual transistors that were measured, however, were from lots intended for room temperature applications, and several other processing steps were included. All of the devices that were measured included a delta-doped layer placed in the channel during the growth, in order to make the n-channel and p-channel turn-on voltages more symmetric. Several of the devices also included a well implant before the gate was added. The well implant was p-type for n-channel devices, and n-type for p-channel devices.

Two lots of CHFET's were measured. The first lot of CHFET's used the bare gate to align the source and drain implants. The second lot of CHFET's included a gate sidewall spacer, in order to reduce the gate leakage current. In these devices, a gate sidewall region implant was done, using the bare gate as a mask. Then gate sidewall spacers were added to the sides of the gate and the source and drain implants were done, self-aligned by the gate sidewall spacers. This allows the doping concentration in the region adjacent to the gate to be controlled independently from the source and drain doping concentration. The actual dopant species and concentrations are proprietary.

Each of the two lots consisted of a series of chips, and each chip contained a number of different sized n-channel and p-channel devices. Each chip was fabricated using a different process variation including variation of the thickness of the AlGaAs dielectric, and the presence or absence of a well implant. The different chips from the second lot also contained variations in the gate sidewall spacer widths and the doping concentration in the sidewall region. All of the chips were functional at 4 K as is discussed in Section III. The effect of some of the process variations on the gate leakage current and noise are described in Sections IV and V.

III. The Current-Voltage Characteristics of the CHFET

The transistor curves at 4 K for typical n-channel and a p-channel CHFET's are shown in Fig. 2. The data were measured using a HP4145B semiconductor parameter analyzer. The CHFET operates normally at 4 K without any anomalies, and the characteristics exhibit the expected dependence on gate voltage and device size. The subthreshold drain current versus gate voltage is shown in Fig. 3. As expected, the current in the subthreshold region varies exponentially with gate voltage, as

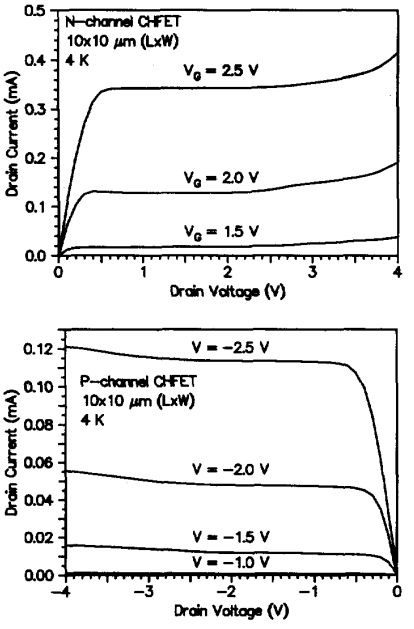

Fig. 2. The transistor curves for an n-channel and p-channel CHFET.

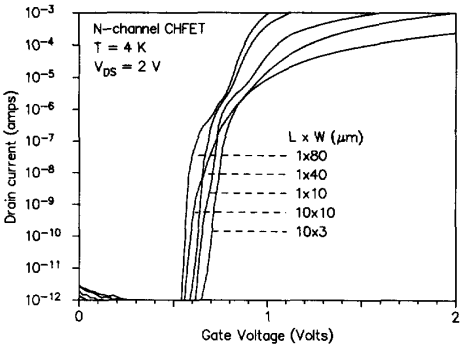

Fig. 3. The subthreshold current for various size n-channel CHFET's. The current was measured with an HP4145B semiconductor parameter analyzer which has a sensitivity of approximately 10^{-12} A.

given by

$$I_D = I_0 \exp(V_{GS}/V_a) \tag{1}$$

where I_D is the drain current, V_{GS} is the gate-source voltage, and V_a is a constant which we will refer to as the exponential voltage.

Although the subthreshold current exhibits an exponential gate voltage dependence, as expected, the value of V_a is much larger at low temperatures than expected, and this anomaly remains unexplained. The constant V_a depends on the temperature, T, and on an ideality factor, n, which is equal to the ratio of the change in channel potential to the change in gate-source voltage. That is, V_a is given by

$$V_a = nkT/q \tag{2}$$

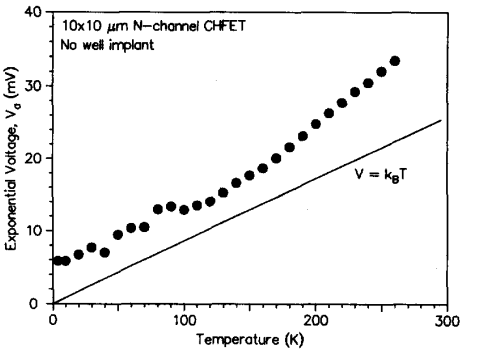

Fig. 4. The exponential voltage V_a (from the subthreshold current relation $I = I_0 \exp(V_{GS}/V_a)$) as a function of temperature plotted as circles for a $10 \times 10\,\mu\text{m}^2$ n-channel CHFET. For comparison, the relation $V = kT/q$ is plotted as a solid line.

where k is Boltzmann's constant. In devices without a well implant, the channel is in close proximity to the gate, separated only by the AlGaAs dielectric. The gate and channel are on top of the buffer layer that is undoped and essentially an insulator, and thus are widely separated from any other source of charge. Therefore, the channel potential should follow the gate-source voltage in nearly a 1 : 1 ratio, which would imply that n should be very nearly equal to one. This should be independent of temperature, since the buffer layer is undoped, and there is nothing to freeze-out. The measured value of the ideality factor n is nearly equal to one near room temperature, but becomes as large as 17 at 4 K. This can be seen Fig. 4, which plots V_a for a $10 \times 10\,\mu\text{m}^2$ n-channel CHFET without a well implant as a function of temperature from 4 K to 260 K a similar effect seen in silicon CMOS has been ascribed to the presence of band edge interface states. It is not known if interface states are responsible in the CHFET, but this anomalous behavior is of serious concern since it lowers the subthreshold gain by the ideality factor, that is, the subthreshold gain is 17 times less at 4 K than would be expected. The measured normalized subthreshold transconductance at 4 K is 0.17 mS/mm for the $10 \times 10\,\mu\text{m}^2$ CHFET of Fig. 4 when biased at a 10 nA drain current. The expected transconductance is 2.9 mS/mm.

IV. The Gate Leakage Current

The gate current of the first lot of CHFET's which did not include gate sidewall spacers has been previously reported [11], [12]. The current is due to a combination of field-emission, thermionic-field-emission, thermionic-emission, and ohmic conduction components, each of which is dominant for different values of the temperature and gate voltage. Below 10 K, the current for both positive and negative gate voltages is dominated by field emission. For reverse gate voltages (negative for n-channel CHFET's), the field emission is described well by the Fowler–Nordheim equation, while for forward gate voltages it is not. Transistors of different gate lengths and widths were examined to determine whether the current was uniform over the gate area, or was concentrated at

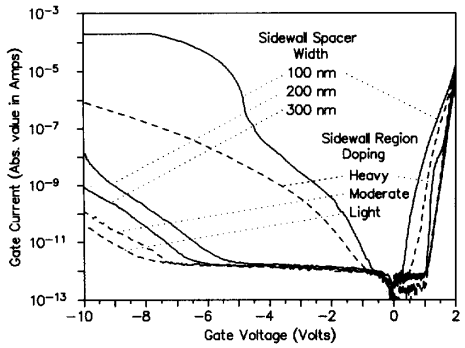

Fig. 5. The gate current versus gate voltage for devices with different gate sidewall widths and different doping concentrations in the sidewall region adjacent to the gate.

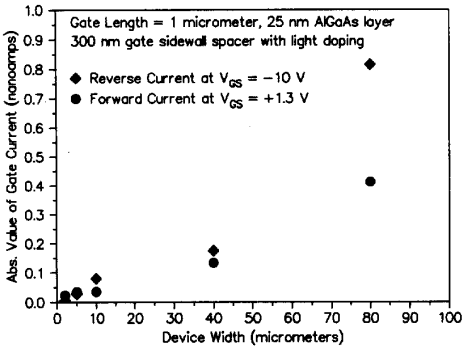

Fig. 6. The dependence of the gate current at $V_{GS} = -10$ V and +1.3 V versus width for 1 μm-long n-channel CHFET's with a 300 nm gate sidewall space and light sidewall region doping.

the gate edges. Any size dependence in the first lot, however, was overwhelmed by a large device-to-device variation. The gate current-gate voltage curves tended to cluster when plotted on a semilog scale, and at any given voltage the current of about 80% of the devices was within an order of magnitude. About 20% of the device were outliers, with much higher currents, sometimes over five orders of magnitude more. It was concluded that the current might be dominated by tunneling through point emitters at the gate edges, making the magnitude of the current device-specific and somewhat random.

Measurements on the second lot of devices with the gate sidewall spacers provided new information [13], [14]. The data were measured with the source and drain grounded using an HP4145B semiconductor parameter analyzer, and is plotted for several typical devices in Fig. 5. The flat region at approximately 10^{-12} A exhibited by some of the curves is due to the sensitivity limit of the HP4145B.

The gate current is strongly dependent on both the gate sidewall spacer width and on the sidewall region doping concentration. The three solid curves represent devices with moderate sidewall doping and spacer widths of 100, 200, and 300 nm. The current decreases monotonically with increasing spacer width. The dotted lines represent devices with a 300 nm spacer, and with light, moderate, and heavy doping in the sidewall region. Again, the current increases strongly and monotonically with increasing doping concentration. The transistor with the smallest spacer width and the heaviest sidewall doping concentration exhibits reverse gate current that is orders of magnitude larger that the other devices. In addition, the device-to-device variation of the current is larger for these sets of devices. This device-to-device variation overwhelms the size dependence. This behavior is similar to that of the first lot of devices, which did not include sidewall spacers.

The current for the devices with the widest sidewall spacer and light sidewall region doping, on the other hand, shows a regular size dependence. Both the forward and reverse currents scale linearly with width. This is shown in Fig. 6 which plots the current at −10 V and +1.5 for 1 μm-long devices as a function of width.

The reverse current does not show any systematic length dependence, while the forward current increases sublinearly with increasing length. Since the channel is depleted for reverse voltages, the reverse current is expected to be dominated by tunneling at the gate edge, and should be independent of the length. For forward voltages, there is a sheet of channel charge which can tunnel out over the entire area of the device, so it is possible that this current might scale linearly with the area. The fact that the actual dependence is sub-linear suggests that while this current is present, there is a component due to tunneling at the gate edge as well.

The gate leakage current for realistic operating conditions can be determined from Fig. 7, which plots on the same scale the drain current and gate current as a function of voltage. These data are for the CHFET with the widest sidewall spacer and the light sidewall region doping; the drain-source voltage was 2 V. The data represented by the solid lines were recorded with the HP4145B parameter analyzer, which has a sensitivity of 10^{-12} A. A Keithley 617 electrometer was used in the integrating mode to measure the gate current down to about 10^{-14} A, and these data are plotted in Fig. 7 as discrete circles. It can be seen from the subthreshold drain current data that it requires a gate voltage about 0.8 V to bias the device at about 10 nA, which is a reasonable value of bias current to use in low-power readout circuit applications. At this gate voltage the gate leakage current is on the order of 10^{-14} A.

V. The Noise Voltage

The input-referred noise voltage was measured using a feedback circuit that directly provided the input-referred noise voltage. The noise voltage for three different size n-channel CHFET's is shown in Fig. 8. The voltage noise of the largest device without the well implant is approximately $1\,\mu\text{V}/\sqrt{\text{Hz}}$ at 100 Hz. The noise decreases with increasing device size, an effect that has been observed in most types of transistors. The noise voltage for $50 \times 50\,\mu\text{m}^2$ CHFET's with and without a well implant is shown in Fig. 9. The noise is increased by about an order of magnitude by the addition of the well implant. This is expected, since additional dopants tend to increase the trapping and scattering of carriers. The noise was also measured as a function of the temperature, drain bias current, and source-drain voltage. None of these had a very significant effect. The concentration of the channel delta-

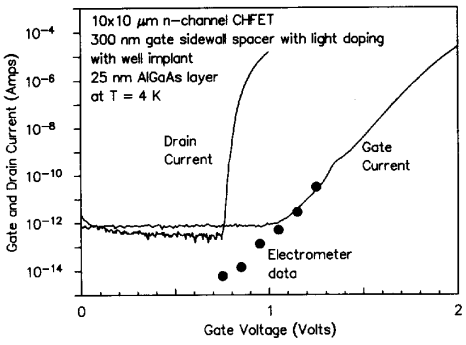

Fig. 7. Comparison of the drain current and the gate current in a CHFET with a lightly doped sidewall region and no well implant. The solid lines were measured with an HP4145B semiconductor parameter analyzer, which has a sensitivity of approximately 10^{-12} A. The circles are points taken with a Keithley 617 electrometer in the integrating (coulomb) mode.

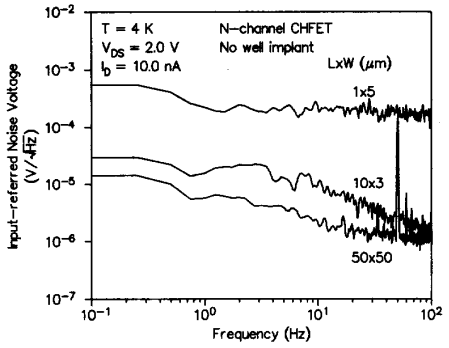

Fig. 8. A comparison of the input-referred noise voltage for different size CHFET's. For some reason, some of the devices showed a peak in the noise at approximately 50 Hz. Some sort of pickup is suspected, but its origin has not yet been found and is still under investigation.

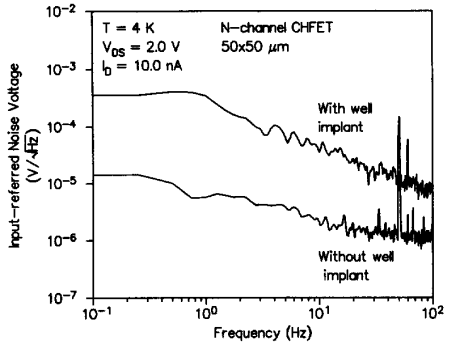

Fig. 9. A comparison of the input-referred noise voltage for $50 \times 50\,\mu m^2$ n-channel CHFET's with and without a well implant.

doping, the sidewall region doping, and the sidewall spacer thickness, likewise, did not have a significant effect on the noise.

VI. P-Channel CHFET's

All of the data discussed in this paper, with the exception of Fig. 2 are for n-channel CHFET's. The p-channel CHFET's

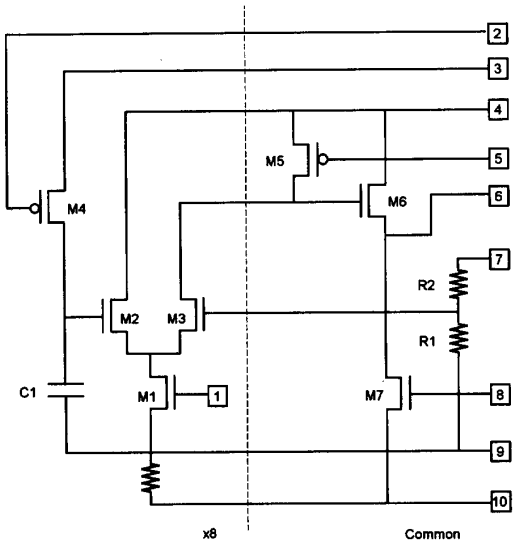

Fig. 10. The circuit schematic for a CHFET 8 × 1 switched op-amp multiplexer.

operate in a similar manner as the n-channel devices, but almost always with inferior performance. The gate leakage current is slightly higher for the p-channel devices, and the transconductance is slightly less, but otherwise the n-channel and p-channel CHFET's were quite comparable in these respects. On the other hand, the noise in the p-channel devices was several orders of magnitude higher. This is in contrast to silicon CMOS, in which p-channel devices normally have significantly lower noise than n-channel transistors. The discrepancy in the noise could be caused by the fact that the hole effective mass in GaAs is much larger than electron effective mass. This could imply that the holes in the p-doped channel are freezing out.

VII. CHFET Multiplexed Op-Amp

N-channel and p-channel CHFET's were integrated to form a simple readout multiplexer, called the switched op-amp multiplexer. The circuit consists of eight addressable cells, connected to a common output circuit. Each cell consists of a n-channel differential pair, the sources of which are connected to an addressable n-channel current source. The drain of the inverting transistor from each pair is connected to a common p-channel active load. The output voltage is taken from this node and buffered through an n-channel source follower connected to an n-channel current source load. The cell is selected by sending a bias voltage to the addressable CHFET. A capacitor simulates the detector, and the capacitor voltage can be reset through an p-channel CHFET. The circuit schematic for the switched op-amp multiplexer is shown in Fig. 10.

The switched op-amp multiplexer was tested at 4 K, and does function. There were some problems, however. The p-channel CHFET's in the circuit had very high leakage currents, and it was not possible to turn them off completely. This made it impossible to turn off the capacitor reset voltage completely, and probably reduced the impedance of the inverter load.

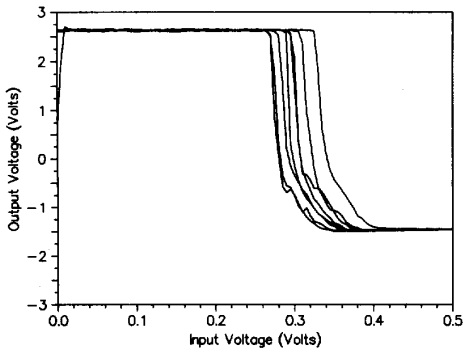

Fig. 11. The inverting transfer characteristics at 4 K for each cell of the 8 × 1 switched op-amp multiplexer.

Nevertheless, it was possible to see both inverting and noninverting action in the circuit, demonstrating a functional amplifier using complementary devices at 4 K. The inverting transfer characteristics measured at 4 K are shown in Fig. 11. There is a curve for each cell. The voltage gain at 4 K is approximately 250.

VIII. Summary

A characterization of the low temperature properties of the CHFET has been completed and the CHFET has been shown to be completely functional at 4 K. Both n-channel and p-channel devices exhibit anomaly free above threshold and subthreshold performance, with no kinks or hysteresis in the I-V curves. A amplifier and miltiplexer circuit using both n-channel and p-channel transistors has been fabricated and tested at 4 K, and was operational, although there were some problems with the p-channel transistors in this particular circuit.

The noise and gate leakage current, however, are still too high for use in readout electronics for many VLWIR sensors. The gate leakage current was reduced dramatically by the inclusion of gate sidewall spacers and lower doping in the gate sidewall region, but the best device still had a current on the order of 10^{-14} A when the transistor was biased for a 10 nA drain current. This is approximately three orders of magnitude too high for VLWIR readout applications. For large $(50 \times 50\,\mu\text{m})$ transistors, the input-referred noise voltage is on the order of 1 $\mu\text{V}/\sqrt{\text{Hz}}$ at 100 Hz for n-channel CHFET's and 100 $\mu\text{V}/\sqrt{\text{Hz}}$ for p-channel CHFET's. This is too large for VLWIR readout applications by approximately two orders of magnitude for the case of n-channel transistors and four orders of magnitude for p-channel transistors. The noise increases as the device size is reduced, or with the addition of a well implant, but is relatively unaffected by the temperature, AlGaAs layer thickness, channel delta-doping concentration, or sidewall spacer width or doping concentration.

In conclusion, the CHFET technology provides a working complementary transistor technology already suitable for some deep cryogenic applications, but some further development is needed to meet the requirements of VLWIR readout application. It may be possible to reduce the gate leakage current further by additional modifications of the gate sidewall spacer. The source of the noise is not known, and more experiments are needed before a systematic approach to reduce the noise can be suggested.

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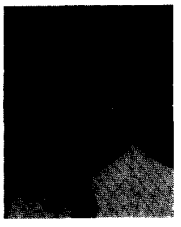
[14] T. J. Cunningham, R. C. Gee, E. R. Fossum, and S. M. Baier, "Noise and electrical characterization of complementary heterojunction field-effect transistors (CHFET)," in *High Temperature Superconductivity and Low Temperature Electronics/1993*, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ, 1993.

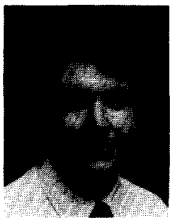
Thomas Cunningham (M'94) received the B.S. and M.S. degrees in electrical engineering from The Ohio State University in 1983 and 1984, respectively, and the Ph.D. from Yale University in 1991. His Ph.D. research was on the growth of GaAs and AlGaAs semiconductor lasers and light-emitteing diodes (LED's) using metallo-organic chemical vapor deposition, and the use of Indium-doped Indium oxide as a transparent ohmic contact to laers and LED's.

He joined the Jet Propulsion Laboratory in 1991, where he is presently a Technical Group Leader. He was been working on GaAs-based transistors for deep cryogenic infrared detector readout applications, including GaAs JFET's as well as the complementary heterojunction field transistor. He is also invloved in developing an improved cosmic ray detector using high resistivity silicon.



Russell C. Gee (M'94) received the B.S. degree in electrical engineering from the University of California, Los Angeles, in 1990. He received the M.S. degree in electrical engineering from the University of California, San Diego, in 1993. His thesis was on the fabrication and characterization of carbon-doped InP/InGaAs HBT's.

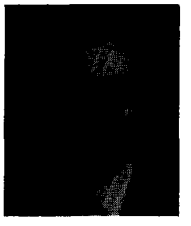
He is currently a member of the Technical Staff at the Jet Propulsion Laboratory. His current research interests include low temperature characterization of GaAs-based CHFET's and the development of CMOS and III-V active pixel sensor technology for visible and IR imaging applications.



Eric R. Fossum (S'80–M'84–SM'91) received the B.S. in physics and engineering from Trinity College in 1979 and the Ph.D. in electrical engineering from Yale University in 1984.

He joined Columbia University in 1984 as an Assistant Professor and became Associate Professor in 1989. In 1990, Dr. Fossum joined the Jet Propulsion Laboratory, California Institute of Technology, to manage image sensor and focal plane technology research and advanced development. His present research activities include CMOS active pixel image sensors for highly integrated imaging systems and very low temperature sensor readout electronics. He has published more than 100 technical papers.

Dr. Fossum received the Yale Becton Prize in 1984, the IBM Faculty Development Award in 1984, the National Science Foundation Presidential Young Investigator Award in 1986, and the JPL Lew Allen Award for Excellence in 1992. He has organized several conferences including the IEEE Workshops on Advanced Solid-State Image Sensors and SPIE Conferences on Infrared Readout Electronics. He is a member of the APS and SPIE.



Steven M. Baier (S'83–M'84) received the B.A. degree in physics from Luther College in 1982 and the M.S.E.E. degree from the University of Minnesota in 1985.

He has been with Honeywell's Technology Center in Bloomington, MN, since 1982, where he has worked on the development of novel semiconductor devices and circuits. In 1985, he served as Principal Investigator on a variety of programs which developed device and process technology for Honeywell's mixed-mode IC technology known as complementary heterostructure FET (CHFET). He is now overseeing the development of CHFET IC's and is investigating new applications of III-V technology.