Dark Current Reduction in Stacked-Type CMOS-APS for Charged Particle Imaging

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***Abstract*—A stacked CMOS-active pixel sensor (APS) with a newly devised pixel structure for charged particle detection has been developed. At low operation temperatures (< 200 K), the dark current of the CMOS-APS is determined by the hot carrier effect. A twin well CMOS pixel with a p-MOS readout and n-MOS reset circuit achieves low leakage current as low as 5×10^{-8} V/s at the pixel electrode under liquid nitrogen temperature of 77 K. The total read noise floor of 0.1 mV_{rms} at the pixel electrode was obtained by nondestructive readout correlated double sampling (CDS) with the CDS interval of 21 s.**

***Index Terms*—Active pixel sensor (APS), CMOS image sensor, correlated double sampling (CDS), detectors, fixed-pattern noise (FPN), leakage current, mass spectroscopy.**

I. Introduction

CHARGED particle detectors have been used for mass spectrometry systems and a two-dimensional charged particle imaging system has been employed to reconstruct a spectrograph or spatial distribution of the ion density. A photo-plate or a fluorescent screen with a micro-channel plate (MCP) is commonly used as the two-dimensional detector for mass spectrographs and ion micrographs [1]. Due to very small thermal noise in the MCP with high multiplication gain, this imaging system provides a high sensitivity as a single ion can be detected. However, total performance is determined by the characteristics of the screen. Because of the nonlinear response of the screen, it is difficult to obtain good linearity and quantitative accuracy when many ions are simultaneously incident on a pixel. The quantum efficiency of MCP is determined by the aperture ratio of the micro-channel and it yields signal loss in ion-to-electron conversion. Gain degradation in MCP over time is another problem in actual usage.

Matsumoto *et al.* [2] reported that spatial resolution, linearity, and dynamic range of ion micrographs and mass spectrographs were greatly improved by using a Stacked AMI (Amplified MOS Imager) compared with the conventional system. They employed a stacked imager approach in which a surface electrode located at the top of the pixel detects incoming ions directly and integrates the signal charge. The signal charge is readout by scanning pixels by on-chip readout electronics. Since no nonlinear devices, such as a florescent screen, are contained in this signal chain, linearity in ion conversion can be improved. In addition to the superior performance characteristics, a use of the stacked CMOS-APS provides several advantages, including low voltage operation, low power consumption, long lifetime, stable detectability against mass number and robustness against environment [2], [3]. However, the sensitivity of the stacked imagers was much lower than that of the MCP approach, so further improvement in noise reduction is required.

In Section II, basic imager architecture and operation of the stacked imager for charged particle detection are introduced. A problem with dark current of the conventional three-transistor NMOS active pixel under low operation temperatures is also explained in this section with experimental results. In Section III, dark current of the conventional three-transistor NMOS active pixel is analyzed with experimental results obtained from test pixel structures to make the problems clear. Then a stacked CMOS-APS with a newly devised pixel structure is presented in Section IV. Fabrication and characterization results of the new pixel are presented in Section V. The new pixel achieves much lower leakage current under low operation temperature and higher sensitivity than those of conventional stacked pixels, which permits longer integration time with low read noise, thereby yielding wider dynamic range.

II. Charged Particle Imaging for Mass Spectrometer

A. Stacked Pixel Approach

A schematic configuration of a conventional n-MOS stacked pixel for charged particle detection is shown in Fig. 1. The pixel consists of a top metal electrode and three transistors, which include a readout transistor M_{RD}, a row select transistor M_{SEL}, and a reset transistor M_{RS}. The top electrode is exposed by eliminating the surface passivation layer, so that the signal ions are irradiated directly.

The top electrode is connected to the gate electrode of M_{RD} and a source electrode of M_{RS}. At the beginning of charge detection period, the top electrode is reset to the reset voltage V_{RS} by turning M_{RS} on. Then, signal ions are irradiated onto the top electrode. Charged particles with acceleration energy of several keV generate multiple secondary electrons when they hit the surface electrode. An anode plate is located about 1 mm apart above the periphery of the imaging array and thus provides an aperture for the imaging area. By applying voltage to the anode plate of about several tens of volts, the secondary electrons generated by collision of incident ions are collected by the anode electrode. Since the kinetic energy of several keV

Manuscript received April 18, 2002; revised October 24, 2002. The review of this paper was arranged by Editor A. Theuwissen.

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Digital Object Identifier 10.1109/TED.2002.806963

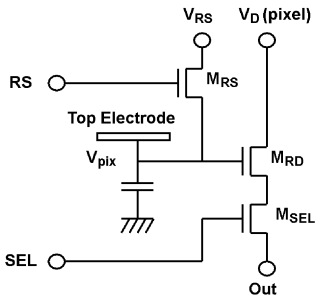

Fig. 1. Circuit configuration of a conventional stacked-type charged particle detection pixel. Voltage of the top electrode $V_{\rm pix}$ is read out through a source-follower circuit formed by $M_{\rm RD}$ and an external load circuit which is connected to the Out node.

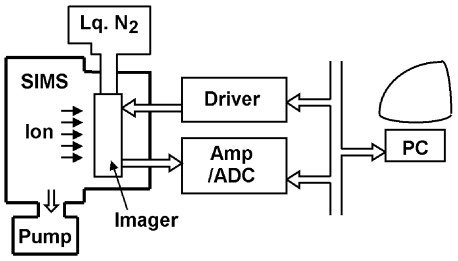

Fig. 2. Schematic block diagram of the ion imaging system. The stacked-type imager is installed in a projection-type SIMS (secondary ion mass spectrometer).

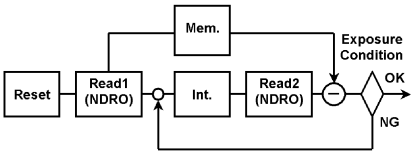

Fig. 3. Operation sequence of the nondestructive readout correlated double sampling (NDRO-CDS). Signal processing is performed by an external computer illustrated in Fig. 2.

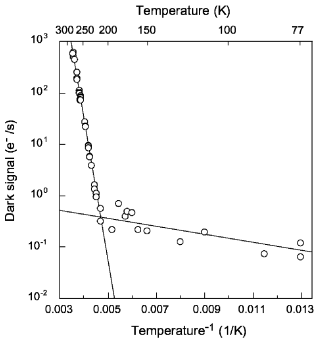

Fig. 4. Temperature dependence of dark current of a conventional charged particle imager.

of the incident ions is much larger than the electrical potential of the anode electrode, distortion caused by the anode electrode is negligible. Charge of the implanted ions and the positive charge corresponding to the emitted secondary electrons are accumulated on a storage capacitor, thereby increasing the potential of the top electrode. A multiplication factor of larger than unity is thus expected. The amount of the accumulated charge can be estimated by reading out the increase of the top electrode potential through a source-follower circuit with its load being not shown in the figure.

The feature of this stacked pixel structure is that the detecting part of charged particles and the signal readout part are separated. It results in the protection of the device from the high energy collision of the charged particles, so that long lifetime with stable characteristics can be obtained. A high fill factor is another advantage of the stacked type pixel, which gives high quantum efficiency. It improves the signal-to-noise ratio and quantitative accuracy.

The charged particle imager has been used for a secondary ion mass spectrometer (SIMS) system. A block diagram of our ion imaging system is shown in Fig. 2. The imager is installed inside SIMS and held in vacuum, so that the ion image is directly focused on the top electrodes of the imager. The signal from the imager is amplified by a low noise operational amplifier and converted to digital data, which is fed to a PC to reconstruct an image. The imager is installed in a vacuum chamber and cooled by liquid N_2 to achieve long integration time by reducing thermally generated dark current.

In order to decrease readout noise, reset noise suppression using nondestructive readout correlated double sampling (NDRO-CDS) is used [4]. The operation of NDRO-CDS is shown in Fig. 3. First, the imager is reset by turning the reset transistor $M_{\rm RS}$ on, and an offset signal that includes fixed pattern noise (FPN) and reset noise is readout nondestructively and transferred to a frame memory. After an integration period, the signal is readout again. Since the reset noise components in both images are identical, it can be suppressed by subtracting the offset image. In addition, since the second signal is also readout nondestructively, integration can be continued if the amount of signal is not large enough; namely the sensor is capable of monitoring the integration condition.

Compared to the CCD, this nondestructive readout capability of CMOS active pixel is one of advantages in applications of stacked-type imager. In stacked type CCDs, it is difficult to suppress reset noise, since the stacked electrode and a charge storage part of a pixel are connected by a metal contact, which yields incomplete charge transfer between the charge storage part and a CCD register and results in the reset noise in every transfer operation [5].

Another significant noise source is the dark current. Because of low signal intensity in actual usage of ion imaging, the integration time often exceeds one hour to obtain quantitative accuracy. Therefore, a cooling system to reduce dark current must be implemented. Fig. 4 shows a measurement result of temperature dependence of the dark current in a charged particle imager with a conventional pixel structure that consists of n-MOS transistors located in a common p-well [6]. The dark current depends on thermal generation model with activation energy of about 0.55 eV from 200 K to room temperature. The activation energy is in good agreement with half of the bandgap of silicon. However below 200 K, the temperature dependence becomes weak with an equivalent activation energy of 0.015 eV and a dark current of 0.1 e^-/s is measured even at 77 K, which suggests different mechanism in dark current generation under low operation temperatures. Assuming an integration time of one hour, the dark current of $0.1e^-$/s results in several

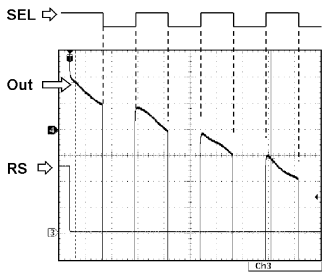

Fig. 5. Oscilloscope waveform of dark current integration, which was obtained from a test pixel structure at 100 K. The schematic configuration of the pixel is the conventional three-transistor circuit shown in Fig. 1.

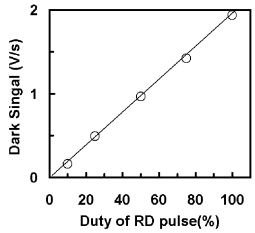

Fig. 6. Relationship between dark current under operation temperature of 100K and the duty of the select pulse SEL. Dark current is expressed as the voltage drift in V_{pix}/s.

hundreds of dark electrons, which causes significant noise due to its quantum fluctuation and variations in pixels.

III. Dark Current Analysis

In order to study generation mechanism of the dark current under low operation temperatures, test pixel structures were designed and fabricated in 0.8 μm CMOS process. Fig. 5 shows a measurement result of dark current generation in a test pixel structure operated at 100 K. The pixel configuration is the conventional n-MOS circuit as shown in Fig. 1. After the pixel was reset by a reset pulse RS, dark current was integrated with applying periodical select pulses SEL. As shown in Fig. 5, the dark current is mostly generated during the readout period when the select pulse is set at high.

In Fig. 6, dark current values are plotted versus duty of the select pulse. The vertical axis of the figure denotes the dark current and is expressed as a voltage drift/s at the pixel electrode, Vpix. As shown in the figure, the dark current is proportional to the duty of the select pulse, and the value is large compared to that of the general-purpose imagers. In general-purpose imagers, dark current is determined by thermal generation and the value is commonly in the order of a few $\sim$ several tens of mV/s. From these facts, it means that there exists a certain different mechanism in dark current generation under low temperatures and a leakage due to a hot carrier effect is the most possible cause.

It is known that minority carrier injection due to the hot carrier effect contributes to the dark current [7]. In Fig. 7, drain voltage dependences of the dark current obtained from test pixel structures with different gate length of M_{RD} are shown. The duty of the select pulse was set at 2.5×10^{-5}, which equivalently corresponds to an operation condition of a $\sim$40 k pixel imager. The dark current depends on the drain voltage exponentially,

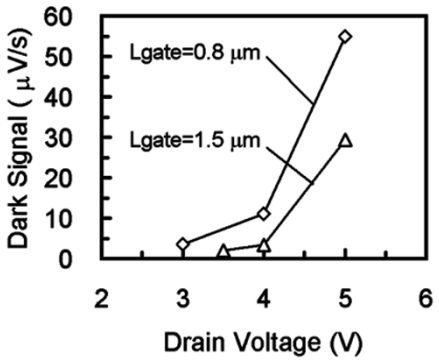

Fig. 7. Drain voltage dependence of the dark current of pixels with gate length of 0.8 μm and 1.5 μm at 100 K. The duty of the select pulse was set at 2.5×10^{-5}.

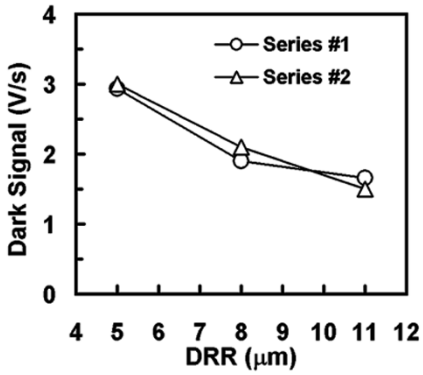

Fig. 8. Relationship between measured dark current at 100 K and the distance between M_{RD} and the n+ source of M_{RS}.

and decreases with increased gate length of the M_{RD}. These experimental results clearly suggest the contribution from the hot carrier effect. Because of low temperature, mobility of channel electrons increases, which should enhance the hot carrier effect.

The hot carriers in the readout transistor can emit photons [8] and the optically generated carriers result in excess dark current [9], [10], [12]. If the photogenerated carrier contributes dark current generation, it should depend on the distance between the readout transistor M_{RD} and the n^+-floating electrode of M_{RS}. In order to identify contribution from the photo generated carriers, three pixel structures with the distance of 5 μm, 8 μm, and 11 μm were fabricated and tested. In Fig. 8, dark current versus the distance between M_{RD} and n^+-diffusion, DRR, is plotted and it is seen that the dark current decreases to about a half with the decrease in DRR from 5 μm to 11 μm. The emitted photons also generate minority carries in the p-well region outside of the depletion layer around the n^+-floating diffusion and a part of the generated minority carriers can diffuse into the floating diffusion. Therefore the experiment was not sufficient to estimate quantitative amount of photon emission, but it identifies contribution from the electrons generated by emitted photons.

From these facts, it can be concluded that it is difficult to achieve complete suppression of the dark current by this approach due to the pixel size limitation, although increasing the gate length of the readout transistor and/or increasing the distance between readout transistor and the n^+-sense node reduces dark current.

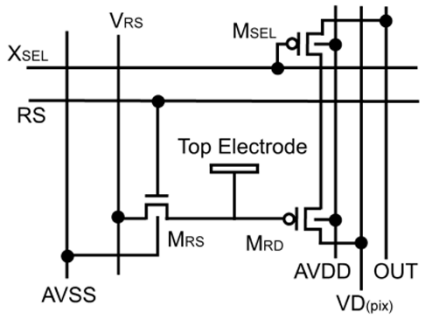

Fig. 9. Circuit configuration of the proposed CMOS pixel. The pixel consists of a pMOS readout circuit and an nMOS reset circuit. Transistor size of M_{RD} is 1.8 μm/1.1 μm (W/L).

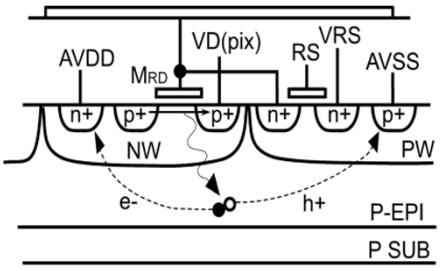

Fig. 10. Schematic cross-sectional view of the new pixel. The select transistor M_{SEL} is not shown in this figure. A black circle and a white circle denote an electron and a hole generated by a photon emitted at M_{RD}.

IV. Pixel Design for Dark Current Reduction

Assuming the leakage models mentioned above, we propose a new pixel structure. The points of the design of this pixel are suppression of the hot carrier effect and avoidance of carrier diffusion into the floating diffusion. Circuit configuration of the pixel is shown in Fig. 9. The pixel consists of p-MOS readout and n-MOS reset circuits. The hot carrier effect in p-MOS transistors is lower than that of n-MOS transistors due to lower carrier mobility [11]. In addition to smaller hot carrier generation at the readout transistor, the dark current component from photo generation can also be suppressed by implementing twin-wells into this pixel circuit. A schematic cross-sectional view of the pixel is illustrated in Fig. 10. The photo-generated carriers are mostly collected by the well regions and drained through well contacts, while only electrons generated very close to the n^+-source region of M_{RS} have a possibility to diffuse into the region. Therefore, the low hot-carrier effect and low dark current are expected with this pixel.

Since the accumulated signal has positive charge in this particular ion detection application, the pixel voltage increases with accumulated signal, and thus the top electrode should be initialized at a low voltage to extend dynamic range. Therefore, an n-MOS reset transistor and a p-MOS readout transistor are preferable.

V. Fabrication and Characterization Results

In order to confirm dark current reduction capability of the proposed pixel, a new charged particle imager was fabricated and tested. Fig. 11 shows the developed charged particle detection imager. The imager was fabricated in 0.8 μm twin-well CMOS technology. Pixel size is 20 μm $\times$ 20 μm and the number of effective pixels is 600 $\times$ 576, yielding an image area of 12.00 mm $\times$ 11.52 mm. Because of the stacked structure, a high fill factor of 88% has been achieved, and highly sensitive ion detection is possible. A reset inhibit function is implemented to achieve NDRO-CDS operation. Read noise of the imager at 100 K is measured to be 0.1 mV_{rms} referred to the top electrode voltage with NDRO-CDS where the CDS interval of 21 s and 20 kHz pixel rate are used. With a design value of pixel capacitance of 14 fF, the equivalent noise electron number is estimated to be $9e^-$. The measured read noise voltage includes

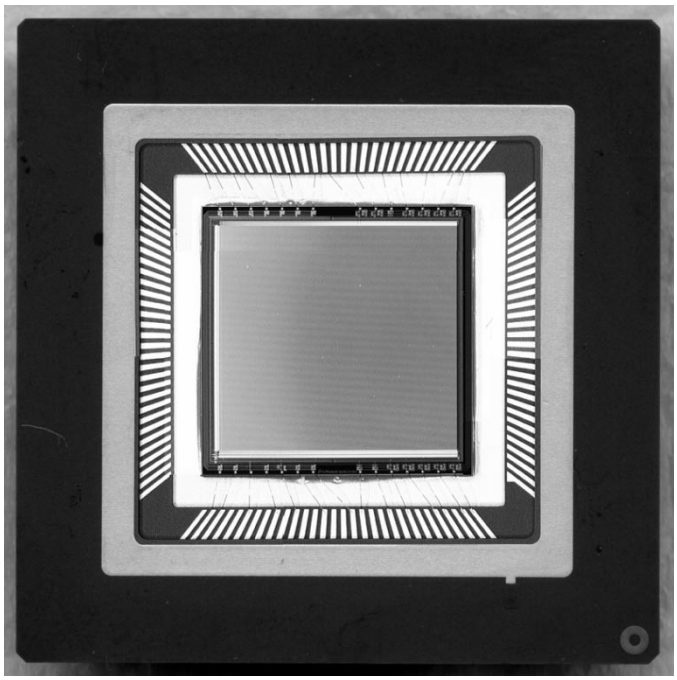

Fig. 11. Chip photo of the newly developed charged particle imager assembled in a PGA package.

those from dark current FPN and external circuits. In conventional CDS operation, reset-noise voltage is estimated from an equation of $\sqrt{2kT/C}$, where k and T denote Boltzmann's constant and absolute temperature, respectively, and is calculated to be 0.44 mV_{rms}. Therefore, the experimental result shows that noise floor was reduced to be less than 1/4 of the conventional reset noise.

The relationship between the dark signal rate at 77 K and the drain voltage of M_{RD} is shown in Fig. 12. The dark current signal has been significantly reduced to less than 1×10^{-7} V/s at the pixel electrode with the proposed pixel. The dark current is approximately two orders smaller than that of the conventional n-MOS pixel. Since the dynamic range and linearity of the ion conversion characteristics were not degraded when the drain voltage is larger than 3.5 V, the drain voltage of 3.5 V is considered as a lower limit. Dark signal as low as 5×10^{-8} V/s permits very long signal integration period. For example, when the integration time is 1 h, dark charge is estimated to be $16e^-$ per pixel with a design value of pixel capacitance of 14 fF.

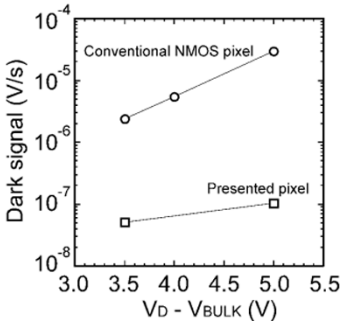

Fig. 12. Measured dark currents of the new pixel. Measured dark currents obtained from a pixel test structure of the conventional nMOS pixel are also plotted. Duty of the select pulse was 2.4×10^{-6} and the pixels were operated at 77 K.

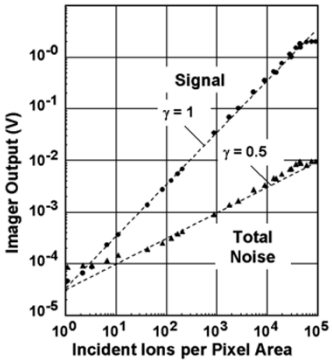

Fig. 13. Ion conversion characteristics of the imager at 77 K. Incident ions are Al^+ ions with acceleration energy of 10 keV. The horizontal axis represents the number of total incident ions per pixel area measured by a Faraday Cup. The amount of signal ions was controlled by changing the integration time. The vertical axis denotes output voltage of the imager. Values of signal and noise voltages are the averaged value and the root mean square values in a 100 × 100 pixel area, respectively.

Imager output at 77 K versus Al^+ incident ion with 10 keV energy is shown in Fig. 13. The horizontal axis denotes the number of incident ion per pixel area of 400 μm^2 and averaged signals 'Signal' and root mean square values of total noise 'Total Noise' are plotted. The NDRO-CDS operation was used in the measurement. Total noise includes dark-current fixed-pattern noise, sensitivity variations of pixels and system noise generated in the following signal chain. The input ion numbers were obtained from Faraday Cup measurement. The averaged signal output increases in proportion to the incident ion number and are very close to $\gamma = 1$ line drawn by a dotted line, which shows good linearity of the imager in a region below an output saturation level of 2.0 V corresponding to 5×10^4 ions. Noise floor of the system was measured to be 85 μV_{rms} at imager output that equivalently corresponds to about two input ions. The total noise increases in proportion to the square root of the number of incident ions in the range above ten input ions and below 10^4 ions, thus having a slope of $\gamma = 0.5$, which indicates that the noise is shot noise of the incident ions. The total noise becomes larger than that of the shot noise model when incident ions are larger than 10^4 due to sensitivity variations of pixels. Sensitivity nonuniformity of this imager is approximately 0.5% rms. The cross point between signal line and the shot noise line is very close to one incident ion, which means high quantum efficiency of the pixel due to the high fill factor. It is also found that the secondary electrons does not affect ion shot noise. Since the multiplication factor due to emission of secondary electrons is estimated to be about 4.5 through the course of this work, actual integrated charge is 4.5 times larger than that of the incident ions.

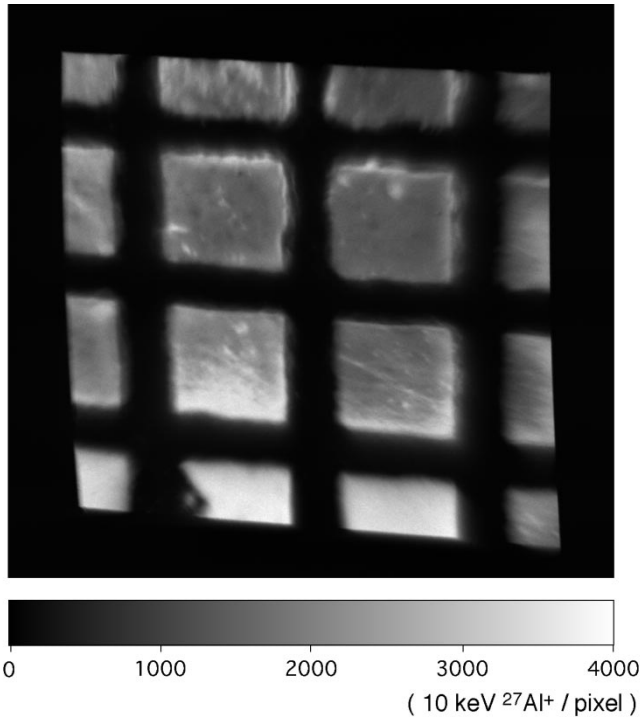

Fig. 14. Obtained Al^+ ion image from a SIMS using the imager.

TABLE I
SPECIFICATIONS OF THE CHARGED PARTICLE IMAGER

Pixel size	20μm × 20μm
Number of pixels	600 × 576
Fill factor	88%
Digital power supply	5V
Analog power supply	3.5V, 1.5V
Noise floor (with NDRO-CDS)	< 3 ions (10keV Al+ ion)
Saturation	50,000 ions (10keV Al+ ion)
Dark current	< 16e-/hour (@100K)
Chip size	14.0mm × 13.9mm

A reproduced image of Al^+ ion density distribution obtained with the imager is shown in Fig. 14. The targeted sample is an aluminum plate that is covered with Cu grids with its pitch of 25 μm and 5 μm width. The reproduced image shows good resolution characteristics of the imager with high sharpness.

Specifications of the imager are summarized in Table I.

VI. Conclusion

A low dark current stacked CMOS APS for charged particle detection has been developed using a newly devised pixel. Dark current of CMOS APS under low operation temperatures is determined by hot carrier effect. A use of a p-MOS FET for a readout transistor reduces a hot carrier effect inside the pixel and the twin-well pixel structure avoids photo generated carrier diffusion into the floating sense node. As a result, the dark current in the low-temperature region was extremely decreased. The pixel configuration also reduces read noise because flicker noise of a p-MOSFET is smaller than that of an n-MOSFET. The low dark current, low read-out noise and high fill factor of the imager permit accurate charged particle image capturing for applications such as ion and electron imaging.

The ion imaging system utilizing the stacked CMOS APS achieves wide dynamic range of 87 dB with high linearity.

In future developments, further sensitivity improvement to reach the sensitivity of the MCP based imaging system is possible by increasing the conversion factor in readout electronics and the multiplication factor at the top electrode.

References

[1] A. Benninghoven, *Secondary Ion Mass Spectrometry: Basic Concepts, Instrumental Aspects, Applications and Trends*. New York: Wiley, 1987.

[2] K. Matsumoto, H. Yurimoto, K. Kosaka, T. Nakamura, and S. Sueno, "A novel imager for secondary ion mass spectrometry," *IEEE Trans. Electron Devices*, vol. 40, pp. 82–85, Jan. 1993.

[3] S. Fuerstenau, G. Soli, T. Cunningham, B. Hancock, B. Pain, and M. Sinha, "Active pixel sensors for charge detection mass spectrometry," in *Proc. 46th ASMS Conf. Mass Spectroscopy and Allied Topics*, Orlando, FL, May 1998.

[4] I. Takayanagi, J. Nakamura, H. Yurimoto, T. Kunihiro, K. Nagashima, and K. Kosaka, "A Stacked CMOS APS for charge particle detection and its noise performance," in *Proc. Progr. IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, R18*, June 1999.

[5] Y. Matsunaga, F. Hatori, H. Tango, and O. Yoshida, "Analysis of signal to noise ratio of photoconductive layered solid-stage imaging devices," *IEEE Trans. Electron Devices*, vol. 42, pp. 38–42, Jan. 1995.

[6] T. Kunihiro, K. Nagashima, I. Takayanagi, J. Nakamura, K. Kosaka, and H. Yurimoto, "Noise characteristics of stacked CMOS active pixel sensor for charged particles," *Nucl. Instrum. Meth. Phys. Res.*, vol. A 470, pp. 512–519, 2001.

[7] J. Matsunaga and S. Kohyama, "Evidence for impact-ionized electron in substrate of n-channel MOS structure," *Appl. Phys. Lett.*, vol. 33, no. 4, pp. 335–337, 1978.

[8] P. A. Childs, R. A. Stuart, and W. Eccleston, "Evidence of optical generation of minority carriers from saturated MOS transistors," *Solid-State Electron.*, vol. 26, no. 7, pp. 685–688, 1983.

[9] S. Tam, F. C. Hsu, C. Hu, and S. Muller, "Spatially resolved observation of visible-light emission from Si MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 386–388, Oct. 1983.

[10] S. Tam and C. Hu, "Hot-electron-induced photon and photocarrier generation in silicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1264–1273, Sept. 1984.

[11] T. Ohzone, H. Iwata, Y. Uraoka, and S. Odanaka, "Photon-energy distribution of hot-carrier photoemission from LOCOS and trench-isolated MOSFET's," *Solid-State Electron.*, vol. 37, no. 7, pp. 1421–1428, 1994.

[12] C. C. Wang and C. G. Sodini, "The effect of hot carriers on the operation of CMOS active pixel sensors," *IEDM Tech. Dig.*, pp. 563–566, 2001.

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Dr. Nakamura is a member of the Institute of Image Information and Television Engineers of Japan. He served as Technical Program Chairman for the 1995 and 1999 IEEE Workshop on Charge-coupled Devices and Advanced Image Sensors.

Eric. R. Fossum (S'80–M'84–SM'91–F'98) was born and raised in Connecticut. He received the B.S. degree in physics and engineering from Trinity College, Hartford, CT, in 1979 and the Ph.D. degree in electrical engineering from Yale University, New Haven, CT, in 1984.

As a member of Columbia University's Electrical Engineering faculty from 1984-1990, he and his students performed research on CCD focal-plane image processing and high speed III-V CCDs. In 1990, Dr. Fossum joined the NASA Jet Propulsion Laboratory, California Institute of Technology, Pasadena, and managed JPL's image sensor and focal-plane technology research and advanced development. He led the invention and development of CMOS active pixel sensor (APS) camera-on-a-chip and subsequent transfer of the technology to US industry. In 1996, he joined Photobit Corporation as Chief Scientist, a company he helped found in 1995, and became CEO of Photobit Technology Corporation in 2000. While at Photobit, he and his staff commercialized the camera-on-a-chip which has been used in Logitech® and Intel® PC cameras, ultra-low-power sensors enabling the swallowable "pill-camera," and very-high-speed, high-resolution sensors used for Hollywood special effects such as in *The Mummy Returns* and *Pearl Harbor*. In late 2001, Photobit was acquired by Micron Technology, Inc. and he is presently a Senior Micron Fellow. He has also served as Adjunct Professor of electrical engineering at the University of California, Los Angeles (UCLA), and is currently Adjunct Professor of electrical engineering-electrophysics at the University of Southern California (USC), Los Angeles, and teaches undergraduate physical electronics. He has served as primary adviser to 12 Ph.D. candidates. He has published 230 technical papers and holds 53 U.S. patents.

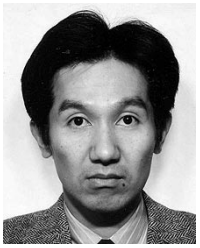
Dr. Fossum received Yale's Becton Prize in 1984, the IBM Faculty Development Award in 1984, the National Science Foundation Presidential Young Investigator Award in 1986, the JPL Lew Allen Award for Excellence in 1992, and the NASA Exceptional Achievement Medal in 1996. He was inducted into the U.S. Space Foundation Technology Hall of Fame in 1999. He founded the biannual IEEE Workshops on CCDs and Advanced Image Sensors and the SPIE Conferences on Infrared Readout Electronics. He has served on program committees for the IEDM, ISSCC, and SPIE conferences. He has served as associate editor for IEEE TRANSACTIONS ON VLSI, guest editor for IEEE JOURNAL OF SOLID STATE CIRCUITS, and was Guest Editor-in-Chief for IEEE TRANSACTIONS ON ELECTRON DEVICES Special Issue on Solid-State Image Sensors published in October 1997. He was recently named to the Board of Fellows for Trinity College, CT where he also serves on the college's Engineering Advisory Committee.

Kazuhide Nagashima was born in Tokyo, Japan, on April 9, 1972. He received the B.S., M.S., and Ph.D degrees in earth and planetary sciences from Tokyo Institute of Technology in 1996, 1998, and 2001, respectively.

Since 2001 he has been a Researcher with Venture Business Laboratory, Tokyo Institute of Technology, where he works on isotope study using SIMS about meteorites.

Takuya Kunihiro was born in Yokohama, Japan, on August 7, 1973. He received the Ph.D. degree in earth and planetary sciences from Tokyo Institute of Technology, Tokyo, Japan, in 2001.

Since 2002, he has worked as a Postdoctoral Fellow with the University of California, Los Angeles. He has conducted research on secondary ion mass spectrometry and the origin of the solar system.



Hisayoshi Yurimoto was born in Wakayama, Japan, on March 12, 1958. He received the D.Sc. degree in geoscience from the University of Tsukuba, Japan, in 1985.

From 1985 to 1994, he was a Postdoctoral Fellow and an Assistant Professor with the University of Tsukuba. He joined the Department of Earth and Planetary Sciences, Tokyo Institute of Technology as an Associate Professor in 1994. He is mainly interested in the origin of the earth and planets and secondary ion mass spectrometry.