Cosmic-ray detector with interdigitated-finger pixels for two-dimensional position information from a single wafer side

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ABSTRACT

This paper describes a type of cosmic ray detector for isotopic and energy detection of energetic nuclei which derives both dimensions of position information from one side of the detector. This simplifies the required readout electronics, since only one precision amplifier connected to the other side is required for an accurate detection of the energy loss. Two dimensional readout is enabled by the use of pixels consisting of closely spaced interdigitated electrodes alternately connected to row and column lines. Spreading of the charge produced by the cosmic ray results in the charge being collected by more than one electrode producing both a row and column signal on one side of the detector. The design, fabrication, and characterization of the interdigitated-pixel detector is discussed.

1. INTRODUCTION

This paper discusses a sensor for detection of cosmic rays consisting of energetic nuclei. Intense fluxes of energetic nuclei are emitted by solar flares. An analysis of such particles provides information on solar particle acceleration and transport, and on the elemental and isotopic composition of the Sun, which is important for an understanding of the history of solar system material.[1]

The particles of interest are the nuclei of helium and heavier elements with energies in the range of 10 to 100 MeV. The flux of the heaviest of these incident on a spacecraft can be as low as $1/cm^2$-sec, contained in a $10^6/cm^2$-sec background flux of 1 MeV protons. The cosmic ray is characterized by knowing its charge, element and isotope, incident energy, and the direction in space from which it came. Equivalently, it may be stated that a detector for such particles must be able to identify the charge, mass, incident energy, and angle of incidence.

The silicon PIN detector has been successfully used for this application. The PIN detector is composed of three layers consisting of p-type silicon, intrinsic silicon, and n-type silicon. For this application, the p-type and n-type regions are thin layers on either side of the wafer and the remainder, which forms the bulk of the wafer, is made intrinsic silicon. By "intrinsic," it is meant that the silicon is not intentionally doped. Free carriers in this region are due to generation of electron-hole pairs by thermal excitation over the band gap (a process which depends only on the silicon bandgap and the temperature and is therefore "intrinsic" to the silicon), together with carriers produced by residual background impurities. Because of the relatively small number of carriers in the intrinsic region, it can be completely depleted by a reverse bias applied between the p-type and n-type layers. When this occurs, an electric field exists across the intrinsic region, and any carriers subsequently generated in the region are swept out by the electric field resulting in a current through the device. A schematic cross-section of a PIN detector is shown in Fig. 1.

A cosmic ray passing through a PIN detector generates electron-hole pairs along its path, according to a process governed by the laws of quantum mechanics. The energy required to promote an electron from the valence band to the conduction band, i.e., the bandgap energy, as well as the kinetic energies of the free electron and hole are taken from the cosmic ray particle, reducing its energy by that amount. The dual constraints of conservation of energy and conservation of momentum restrict the interaction to a particular energy, which in silicon is approximately 3 eV. Therefore, if all of the particles energy is converted to electron-hole pairs, the incident energy is simply the number of electron-hole pairs multiplied by 3 eV. Quantum mechanics also governs the interaction rate or generation cross-section, which depends on the particle's energy, charge and mass. If the energy of the

particle is known, then this dependence allows the calculation of the charge and mass from the number of electron-hole pairs generated per unit length along the cosmic ray's path.

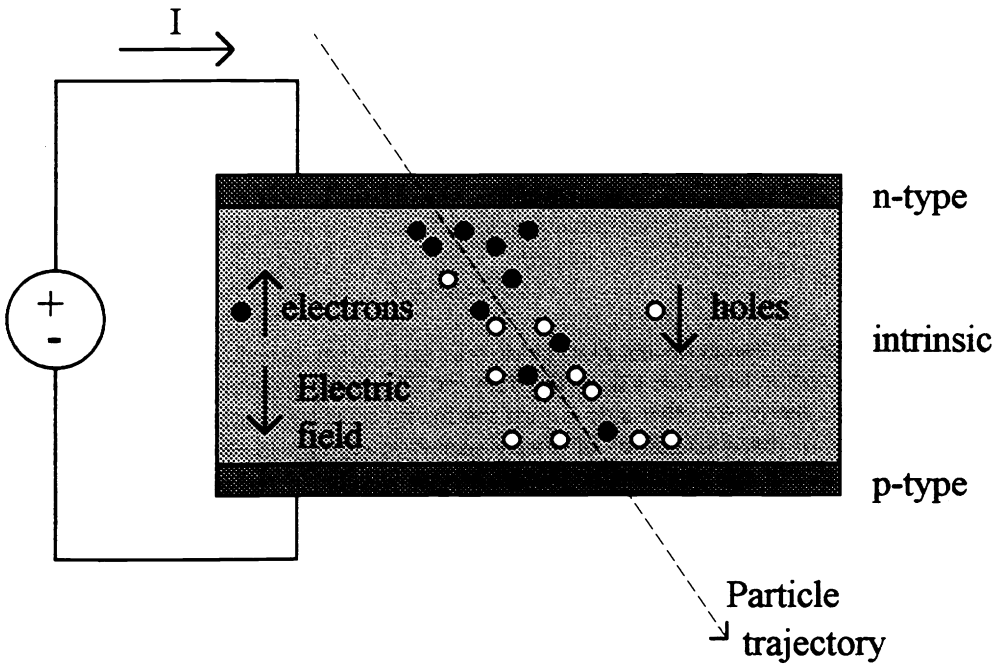

Fig. 1: A cross-section of a PIN cosmic ray detector. In operation, the intrinsic region is completely depleted by a reverse bias. Electron-hole pairs are generated along the particles trajectory as it passes through the detector. The electric field pushes electrons toward the n-type silicon layer on top, and holes toward the p-type silicon layer on the bottom where they are collected, resulting in a detectable current.

The particle's energy, energy loss per unit length and angle of incidence can be found by building a "telescope" consisting of a stack of PIN detectors as shown schematically in Fig. 2. The thicknesses of the various PIN detectors in the stack are chosen such that the particles pass completely through the first two detectors, and then are stopped within the others. The first two detectors are pixelated so that the position where the particle penetrates each are can be found. The angle of incidence, θ, with respect to the detector surface normal is given by:

$$\tan^2(\theta) = d^2/(\Delta x^2 + \Delta y^2) \quad (1)$$

where d is the spacing between the first and second detectors, and Δx and Δy are the differences between the x and y positions, respectively, on the two detectors. The total incident particle energy is related to the sum of the charge collected by all of the detectors in the stack, as previously discussed. The path length l through the first two detectors is given by:

$$l = t/\cos(\theta) \quad (2)$$

where t is the thickness of the detector. The energy loss per unit length is related to the charge collected by the first detector divided by l.

A diagram of an actual telescope consisting of four separate stacks is shown in Fig. 3. Such a detector can provide all of the information necessary to characterize incident cosmic rays. The scheme is dependent on a PIN detector that can provide two dimensional position information and an accurate measure of the charge generated by the cosmic ray.

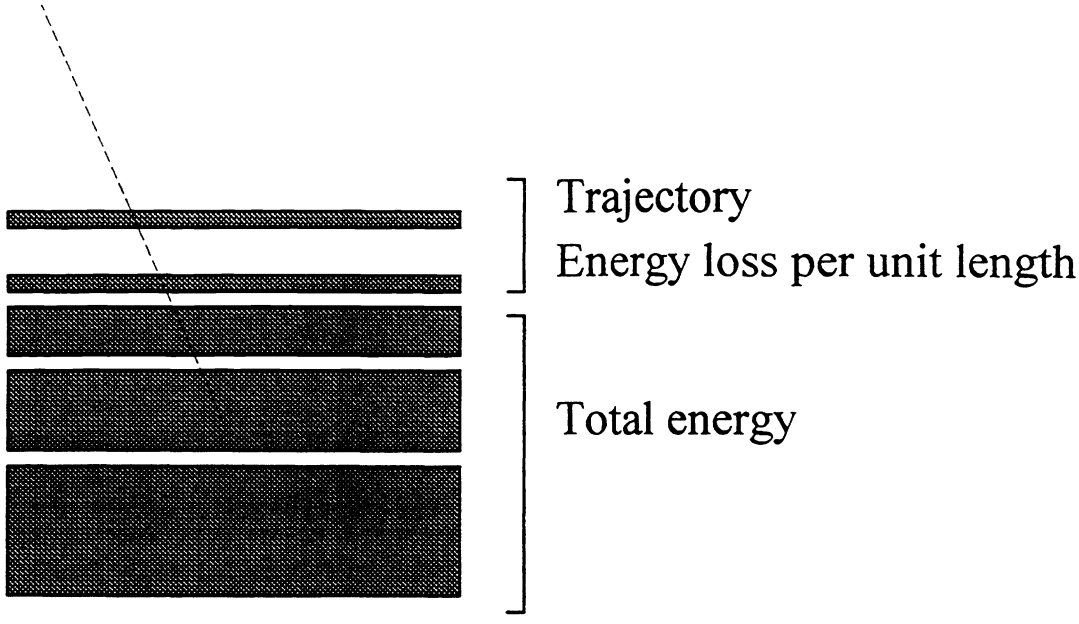

Fig. 2: A cosmic ray "telescope" consisting of a stack of PIN detectors. The first two detectors provide information about both the position and the energy loss per unit length of the cosmic ray as it passes completely through them. The remaining detectors stop the cosmic ray and determine its remaining energy.

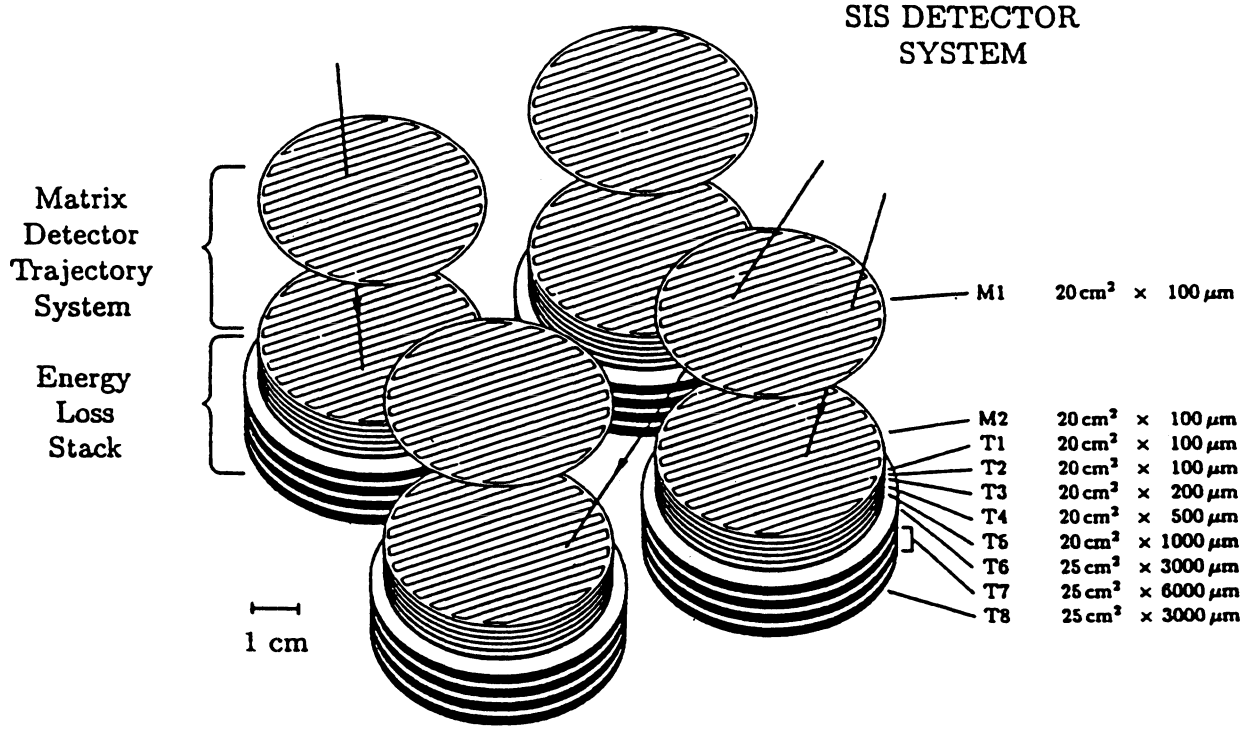

Fig. 3: The configuration of an actual cosmic ray telescope employing four stacks of 4-inch silicon PIN detectors

2. THE CONVENTIONAL DETECTOR SCHEME

The conventional method of building a PIN detector capable of measuring two dimensional position and charge is to get one position dimension from each side of the detector, by dividing each side of the detector into stripes.[2] For example, the front side of the detector can be divided into stripes to determine the row position, and the back side divided into stripes, running at right angles to those on the front, that determine the column position.

A disadvantage of the conventional scheme is that in order to accurately measure the generated charge, there must be a precision pulse height amplifier attached to each stripe on one side. A typically sized detector, e.g., 10 cm in diameter with 1-mm wide stripes, would require 100 precision amplifiers. This implies that the necessary readout electronics will be physically large and complex, and will consume relatively large amounts of power.

The readout electronics could be greatly simplified for a detector design that provided both dimensions of position information using only one side of the detector. This would reduce the precision required of the position sensing electronics to one bit accuracy, that is, it would only have to determine whether or not a particle passed through each pixel. A single precision amplifier is required for the opposite side. This scheme would greatly reduce the size, power consumption, and complexity of the readout circuitry.

One scheme for determining both position dimensions from one side of the detector involves dividing that side into stripes with a connection at each end, and relying on diffusive or resistive division of the signal between the ends in order to indicate where along the stripe the charge was collected.[3] While this has been successful for some uses, it is not suitable for this application, where the particles to be detected are co-incident with a much higher flux of moderate-energy protons. This high flux of protons will result in a "pulse pile-up" and will make the identification of the position of the higher mass nuclei impossible.

3. THE INTERDIGITATED-PIXEL SCHEME

The scheme chosen for this application is to use a pixel consisting of interdigitated electrodes alternately connected to the row and column lines. If the spacing between the electrodes is smaller than width of the cloud of carriers produced by the cosmic ray by time the cloud reaches the electrodes, then the collected charge will be divided between electrodes connected to the row and column lines. Consequently, there will be a row and column signal to identify both dimensions of the particle's position. Note that it is not important that the charge be divided evenly; it is only necessary that a discernible signal appear on both lines. Neither is it important that this charge be accurately counted: a precision amplifier connected to the other side provides accurate pulse height information. The electrodes and electronics for the pixellated side are only required to determine whether or not a cosmic ray passed through each pixel. A schematic cross-section of a PIN detector with interdigitated electrodes is shown in Fig. 4.

A schematic illustration of the interdigitated-pixel concept as viewed from the top is shown in Fig. 5. Inside the unit cell bounded by the row and column lines are a series of electrodes alternately connected to the row and column lines. The dark region in Fig. 5 represents a pixel: charge generated by a cosmic ray anywhere within the dark region will be collected by electrodes connected to row "N" and column "N." For this application, the unit cell and the pixel dimensions are 1-mm square. The size and spacing of the interdigitated electrodes shown in Fig. 5 is greatly exaggerated, for presentation clarity. The electrodes with the largest pitch are actually 40 μm wide and 40 μm apart.

4. DEVICE LAYOUT

The eventual goal is to develop a PIN detector of the kind described in the previous section with 1-mm square pixels on a 4-inch diameter wafer as thin as 50 μm. The present effort involves the development of a prototype consisting of a 9x9 array of 1-mm square pixels on a 250 μm thick substrate. The entire die size including the array and connection pads is 1-cm square. Nine die are fabricated in a single lot, using a 2-inch diameter wafer.

Two generic variations of the PIN detector have been fabricated. In one variation, the n-type polysilicon layer is patterned into the interdigitated collector pattern by wet chemical etching. The p-type implanted layer on the opposite side is uniform across the entire wafer. In the other variation, the p-type layer is patterned into the interdigitated collector pattern by selectively masking the implant. The n-type polysilicon layer is left undisturbed and uniform across the opposite side of the wafer in this variation. A given wafer is processed using one variation or the other. The high resistivity silicon wafers that were used for the patterned-polysilicon variation were polished on both sides, so that the polysilicon was deposited on a polished surface, making photolithography for the wet chemical etch possible. The patterned-implant version used high resistivity wafers with only one side polished, and with the n-type polysilicon deposited on the unpolished side.

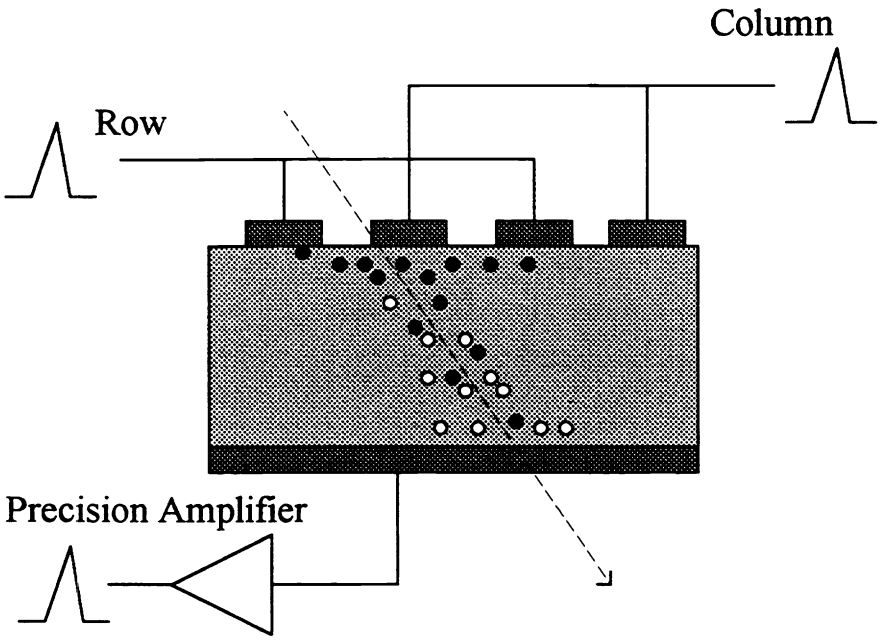

Fig. 4: A cross-section of a PIN detector with interdigitated electrodes alternately connected to row and column lines. Charge spreading due to drift and diffusion results in the charge being divided between the electrodes, creating both a row and column signal. A precision amplifier connected to a broad area collector on the opposite side of the wafer accurately determines the pulse height.

On each wafer, several arrays are used to explore other process variations. There are three variations of the interdigitated electrode width and spacing: 10 μm width with 10 μm spacing, 20 μm width with 20 μm spacing, and 40 μm width with 40 μm spacing, for electrode pitches of 20, 40, and 80 μm, respectively. The pixel pitch of 1 mm was not varied, however. The other variation involves the metallization. In one version, the metal 1 is overlaid with metal 2 in some areas. This process is referred to as metal-metal. In the other version, metal 2 was applied directly to the semiconductor, avoiding a metal-to-metal interface. This process is referred to as metal-silicon. The details of this are discussed in the next section on fabrication.

There is an array for each version of the metallization with each pixel pitch, that is, there is one metal-metal array with 20 μ m pitch, one metal-metal array with 40 μm pitch, one metal-metal array with 80 μm pitch, one metal-silicon array with 20 μm pitch, one metal-silicon array with 40 μm pitch, and one metal-silicon array with 80 μm pitch, making 6 arrays. Each is a 9x9 array of 1-mm square pixels in a 1-cm square die. The are also two 1-cm square die containing various test structures such as contact chains, capacitors, etc., and the metal-metal array with 20 μm pitch is repeated, making a total of nine 1-cm square die on each 2-inch wafer. These nine die are arranged in a 3x3 pattern. A diagram of the unit cell for an array with a 40 μm pitch showing the interdigitated electrode pattern for etching or implantation (depending on the version) is shown in Fig. 6.

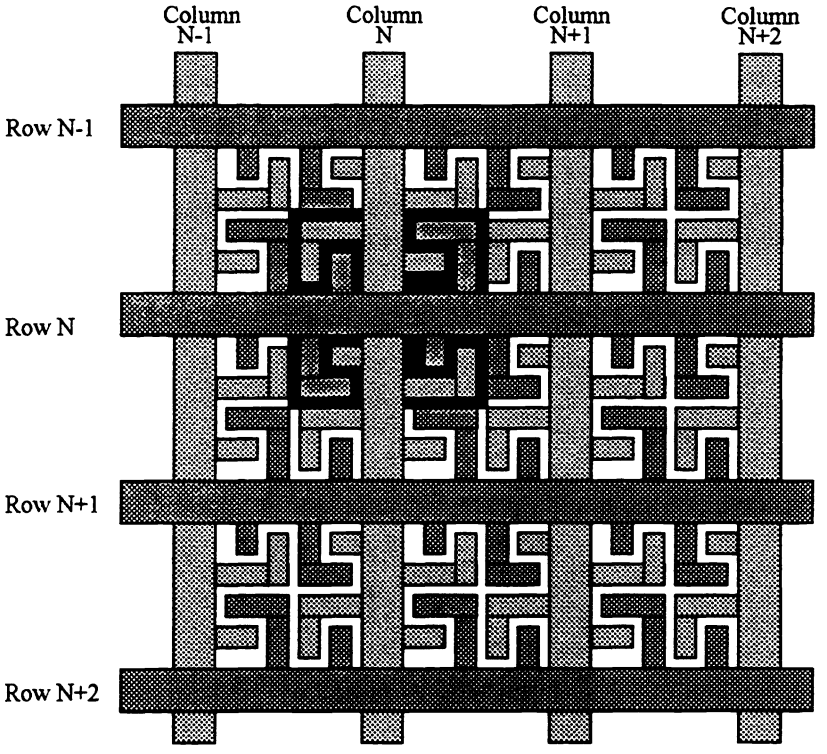

Fig. 5: An illustrative representation of the interdigitated-pixel concept. The dark square represents one pixel. The charge produced by a cosmic ray passing anywhere through the pixel is divided between row line N and column line N. The unit cell bounded by adjacent row lines and column lines contains one quarter of each of four pixels.

5. FABRICATION

The fabrication begins with a 2-inch diameter, 250 μm thick wafer of very pure high-resistivity silicon, with a resistivity on the order of 10 kΩ-cm. The residual impurities make the nominally intrinsic material lightly n-type, with a doping concentration on the order of 10^{11} cm^{-3}. A 1 μm thick layer of heavily phosphorous-doped polysilicon is then deposited on one side, in a process developed by Steve Holland[4]. This layer serves as the n-type layer of the PIN detector, and as a getter: the large number of grain boundaries in the polysilicon combined with the chemical properties of phosphorous complexes cause the polysilicon to trap impurities which would otherwise diffuse into the intrinsic silicon and contaminate it during subsequent high temperature processing. The p-type layer of the PIN structure is produced by doping the opposite side of the wafer using ion implantation.

In the patterned-polysilicon version, fabrication begins by uniformly doping the opposite side p-type using ion implantation of boron. Presently, the implant energy used is 150 keV and the dose is $3x10^{14}$ cm^{-2}. The interdigitated pattern is then etched in the polysilicon using wet chemical etching with a photoresist mask.

After the photoresist is stripped and the wafer is cleaned, a 200 Å passivating oxide is grown in a dry oxide furnace at 900 °C. Contact holes through the oxide to the polysilicon are opened using buffered oxide etch, and then the first metal layer, metal 1, is deposited. Presently metal 1 is aluminum about 1 μm thick. In the metal-metal arrays, all of the polysilicon electrodes are overlaid with metal 1. In the metal-silicon arrays, only those connected to the column lines are. Next, the intermetal dielectric is deposited by electron-cyclotron resonance chemical vapor deposition (ECR-CVD). It consists of a layer

of SiN_x , a layer on SiO_2, and another layer of SiN_x, with the total thickness being about 1 μm. Contact holes are opened in the dielectric using reactive ion etching (RIE). In the metal-metal arrays, the openings are only over the row lines; in the metal-silicon arrays, the dielectric is opened over the row lines and all of the electrodes connected to it in each pixel. The second metallization layer, metal 2, is then deposited. Like metal 1, it is aluminum about 1 μm thick.

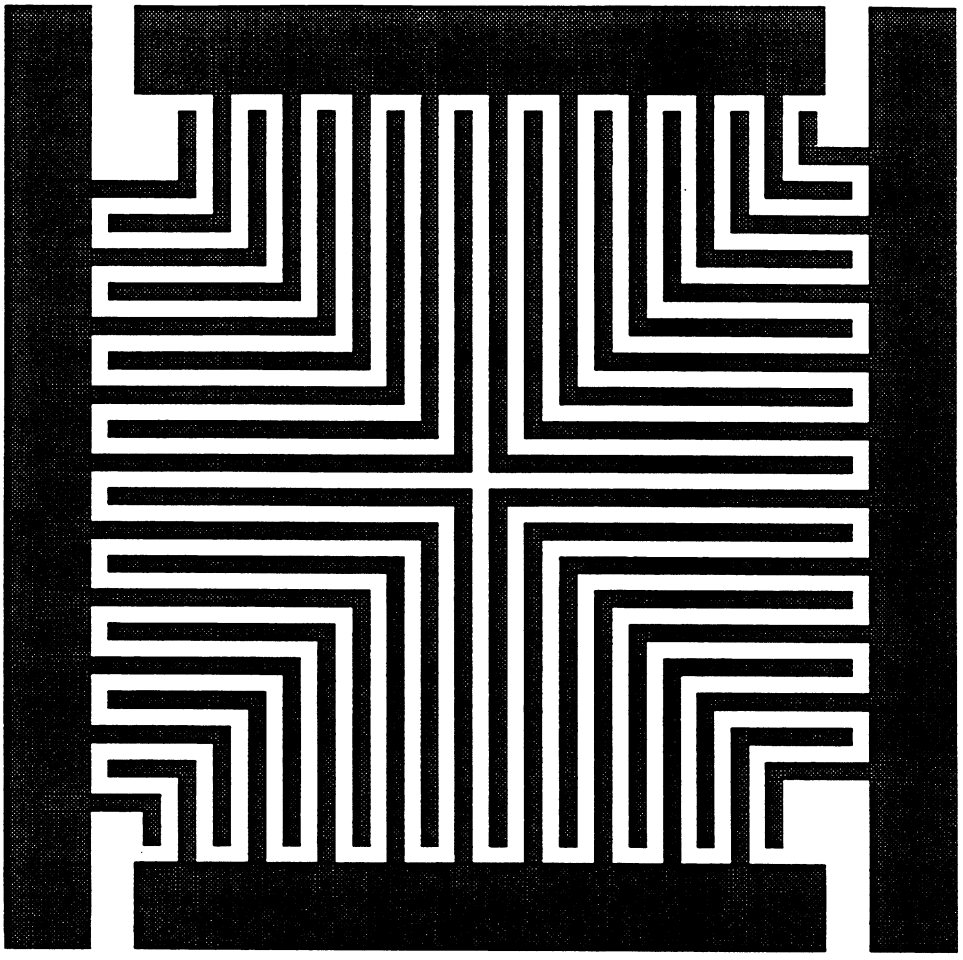

Fig. 6: The electrode pattern for one unit cell of the interdigitated-pixel PIN cosmic ray detector. For the array that uses this particular cell, the electrode width and spacing are 40 μm.

The column lines of the unit cell merge into those of the next, forming a continuous line that runs the length of the array and beyond to pads for connection by probes or wire bonding. The row lines are interrupted and must be connected to each other by horizontal lines in metal 2 that cross over the column lines, electrically separated from them by the dielectric. In the metal-metal arrays, the row line segments in the unit cell and the interdigitated electrodes connected to them are overlaid by metal 1. In theses arrays the dielectric is opened over the row line segments, exposing metal 1. Metal 2 is patterned into long horizontal stripes that contact metal 1 on these segments, then cross over the intact dielectric covering the metal 1 column lines. In the metal-silicon arrays, the dielectric is opened over both the row line segments and the interdigitated electrodes, exposing bare polysilicon. The metal 2 pattern covers the row line the segments and connects them together electrically as in the metal-

metal arrays, but also covers the polysilicon electrodes as well. The photolithography for the metal-metal arrays is more forgiving of misalignment of metal 2 since it does not have to overlay the electrodes, but it requires metal to metal contacts. Since aluminum oxidizes easily, the electrical conductivity of such contacts is a concern.

After metal 2 is deposited and patterned, the device is ready for the back metal, which is a several thousand angstrom thick layer of aluminum deposited onto the p-type implanted side. The aluminum is annealed in hydrogen/nitrogen forming gas at 400 °C for 30 minutes after each metal deposition. The device is ready for wafer level testing at this point, and can be sawed into die, mounted in a chip carrier, and wire bonded.

In the patterned-implant version, the polysilicon layer is not disturbed. First a sacrificial oxide is grown on the wafer, then the side opposite the polysilicon layer is covered with photoresist, which is then patterned. The photoresist selectively masks the implant into the interdigitated electrode pattern identical to that used for the etching in the patterned-polysilicon version. After the photoresist is stripped, the sacrificial oxide is removed and the wafer is cleaned. The implant is given a low temperature activation at 650 °C for 30 minutes. Then a 200 Å passivating oxide is grown at 900 °C in the dry oxide furnace. From here, the steps are nearly identical to that for the patterned-polysilicon device. Contact holes are opened in the oxide over the implant and metal 1 is deposited, patterned and annealed. The dielectric is deposited by ECR-CVD and contact holes are opened in it by RIE. Metal 2 is deposited, patterned, and annealed. There are metal-metal arrays and metal-silicon arrays, identical to the patterned-polysilicon version. After the back metal is deposited and annealed, the device is ready for testing and packaging.

6. TEST RESULTS TO DATE

Several lots of both the patterned-polysilicon version and the patterned-implant version have been fabricated, and initial electrical characterization has been performed. Unfortunately, all of the devices that have been tested so far exhibit an anomalously high dark current, on the order of 1 $\mu A/cm^2$. Measurements by Holland[4] indicate that dark currents as low as 1 nA/cm^2 can be achieved. In addition, there is a soft breakdown at an applied voltage of between 10 V and 80 V. The anomalously high current has impeded further testing. The source of the high dark current and break down are not presently known.

A systematic search for the cause of the anomalous current is now underway. Once it is eliminated, new lots will be fabricated and an electrical characterization of the dark current, line-to-line resistance, and line-to-line capacitance will be performed. The devices will be then undergo particle testing at the Space Radiation Laboratory, initially using an alpha particle source, and then using heavy ions from radioactive sources or accelerated by a Van De Graaff generator.

7. ACKNOWLEDGMENTS

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