Characterization of Evaporated Cr–SiO Cermet Films for Resistive-Gate CCD Applications

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Abstract—**Characterization of electron-beam evaporated Cr–SiO films (cermet) useful for resistive-gate charge-coupled device (CCD) applications is reported. The films are evaporated from powder sources of different Cr–SiO compositions. Auger electron spectroscopy (AES) depth profiling is carried out to measure the uniformity of the cermet composition. Electrical conduction in the cermet films is measured for temperatures ranging from 50 to 370 K, before and after annealing. The electrical characteristics of cermet/GaAs Schottky diodes are measured and compared with Cr/GaAs and Al/GaAs diodes. The effect of rapid thermal annealing (RTA) on the cermet/GaAs diodes and cermet films is investigated. A resistive-gate GaAs CCD delay line is fabricated and tested to demonstrate the performance of the evaporated Cr–SiO cermet as a resistive material.**

I. Introduction

PLANAR, nonoverlapping-gate charge-coupled devices (CCD's) have potential barriers or troughs under inter-electrode gap regions and thus can suffer a reduction of charge transfer efficiency (CTE). The channel potential under the gap depends on the voltage applied to the adjacent electrodes, the ratio of gap size to insulator thickness for surface-channel CCD's, the ratio of gap size to the channel thickness for buried-channel CCD's, the dielectric constant of a material in the gap, and the amount of surface or interface charge in the gap.

One way of reducing the gap problem is to reduce the ratio of gap size to insulator thickness or channel thickness, causing the resultant fringing field to reduce the magnitude of potential barriers or troughs. In silicon CCD's, overlapping polysilicon gates have been successfully employed to effectively eliminate the gap problem. However, in high-frequency short-gate-length devices, overlapping gates have strong capacitive coupling that can effectively "short out" adjacent phases and lead to a variety of problems, including excessive drive power and impedance mismatch. Furthermore, submicrometer dimension gaps can result in a low gate-to-gate breakdown voltage.

The resistive-gate structure CCD (RGCCD) was first proposed by Kim and Snow to eliminate the gap-induced potential barrier problem in silicon CCD's [1]. In their structure, the channel potential under the inter-electrode gaps is controlled by covering the gaps with a resistive layer, allowing the potential to follow the clock waveforms. Since the structure consisted of wide electrodes and narrow gaps, the resistivity of the material covering the gaps must be carefully controlled to be low enough for the potential to follow the clock waveforms, but not so low as to cause excessive power consumption. Such stringent control requirements can introduce manufacturing difficulties. Furthermore, the low power advantage enjoyed by silicon CCD's is eroded by power dissipation in the electrodes.

In the high-speed GaAs CCD arena, power consumption is not as critical of an issue. A modified resistive-gate structure for GaAs CCD applications was proposed and fabricated by Higgins *et al.* [2]. A schematic illustration of the RGCCD structure and its potential profile in the channel are shown in Fig. 1. Unlike the previous structure, this structure has wide inter-electrode gaps covered with a thin resistive layer between narrow finger-type electrodes. This resistive layer, which forms a Schottky contact with the underlying GaAs, acts as an electrostatic potential divider, providing a uniform applied electric field along the channel. The major advantages of this structure, in addition to excellent CTE, are a fast transfer of signal charges due to the fringing field and the compatibility of the resulting CCD and high-performance FET's with thin active layers. With this structure, CCD circuits operating with several gigahertz clock signals have been reported [3]–[5].

Another interesting application of the resistive-gate structure is a millimeter-wave oscillator proposed by Cooper and Thornber [6]. In their device structure, the resistive layer is used as the gate of a long FET in order to apply a uniform lateral electric field in the channel. The field can induce a transferred-electron effect in the GaAs channel. Simulation of this device shows the possibility of making a voltage-tunable oscillator that operates at frequencies exceeding 50 GHz. A similar effect may improve CTE in GaAs CCD's [7].

The properties of the resistive layer are important to CCD performance. It should have a high sheet resistance that ranges from a few kilo-ohms per square to mega-ohms per square, depending upon the CCD geometry. For GaAs applications, the film must make a low-leakage Schottky contact to the semiconductor. For imaging applications, the material must be transparent in the wavelength of interest.

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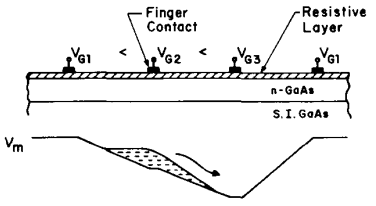


Fig. 1. Schematic illustration of the device structure and channel potential of a resistive-gate charge-coupled device.

The primary choice of a resistive film for GaAs CCD's is an insulator-metal (cermet) composition. The sheet resistance of this film can be easily controlled by the thickness of the film or by the compositional ratio of a metal to a dielectric material. Characterization of cermet films with various combinations of metal and dielectric (W–Al_2O_3 [8], Cr–SiO [9], Ni–SiO_2 [10], Mo–SiO_2 [11], etc.) by various deposition methods including sputtering from a composite target [8], co-sputtering [11], [12], and flash evaporation [9] have been reported. Since the metals used for the cermet are usually refractory, an annealing process can be performed after deposition. In GaAs CCD applications, this can eliminate the use of another capping layer for the annealing of an implanted GaAs channel layer. Another feature of cermet films is that they are typically transparent to visible light and thus may be applicable to imaging devices.

The evaporation temperatures of Cr and SiO are much lower and closer to each other than other combinations of metal and dielectric mentioned above, which makes the Cr–SiO cermet a good choice for electron-beam evaporation. The use of a mixture of powders as an evaporation source makes it convenient to change the film composition for each application, since an optimum sheet resistance of a cermet might vary from design to design.

In this work, the electrical conduction in an electron-beam-evaporated Cr–SiO cermet with various compositions was measured with temperature ranging from 50 to 370 K. Auger electron spectroscopy depth profiling was carried out to measure the compositional uniformity of the cermet, and optical transmission was measured for light with wavelengths from 300 to 900 nm. Cermet/GaAs, Cr/GaAs, and Al/GaAs Schottky diodes were fabricated, and current–voltage characteristics were measured and compared. The effect of annealing on the electrical conduction of the cermet and the *I–V* characteristics of the diodes was measured as well. A resistive-gate CCD delay line is fabricated with a 45 wt.% Cr–55 wt.% SiO cermet and tested to demonstrate the performance of the evaporated Cr–SiO cermet as a resistive-gate material.

II. Fabrication of Cermet/GaAs Schottky Diodes

The source of the evaporation was prepared by mixing powders of Cr and SiO, with grain sizes less than 0.04 and 0.013 mm, respectively, into 30 wt.% Cr–70 wt.% SiO, 45 wt.% Cr–55 wt.% SiO, and 50 wt.% Cr–50 wt.% SiO compositions.

GaAs n-type wafers with ⟨ 100 ⟩ orientation and doping concentrations of $2.3 \times 10^{17}/cm^3$ and $2.0 \times 10^{16}/cm^3$ were used as substrates. The following steps were performed for substrate cleaning: 1) degrease in hot trichloroethylene with ultrasonic agitation for 5 min, 2) soak in acetone for 3 min, 3) rinse in D.I. water for 2 min, 4) rinse in methanol for 5 min, and 5) dissolve native oxides by dipping into $NH_4OH : H_2O$ (1 : 2) solution.

The backsides of the wafers were then deposited with Au–Ge, which was alloyed in forming gas (5 percent hydrogen and 95 percent nitrogen). A positive photoresist was coated on the front side and optically pattered in preparation for a lift-off process.

Glass substrates were also prepared to measure electrical conduction, optical transmission, and the AES depth profile of the cermet films. In addition, pilot glass substrates with 1-cm spacing gold electrodes were used for *in-situ* monitoring of the cermet film sheet resistance during the evaporation.

Cr–SiO cermet films were deposited by electron-beam evaporation in a Denton vacuum evaporation system with a deposition rate and thickness monitor. The residual gas pressure before evaporation was 5×10^{-7} torr. The beam voltage of electron gun was about 2.2 kV, and the beam current was less than 0.1 A, producing a deposition rate of 5 to 8 Å/s. GaAs, glass, and pilot glass substrates were placed closely, and the sheet resistance of the film on the pilot glass substrate was monitored to stop the evaporation when the resistance reached the desired value (typically 400 kΩ/□). Some change of resistance was noted following the evaporation, probably due to the cooling of the substrate.

The cermet layer on the GaAs substrate was then patterned by lift-off. Aluminum was subsequently deposited and patterned on the cermet layer to provide electrical contacts. Independently, Cr/GaAs and Al/GaAs Schottky diodes were formed using electron-beam evaporation and lift-off as well.

Annealing of the cermet films and diodes was performed for 45 s at 425°C in a Heatpulse 210 RTA system in a forming gas ambient.

III. Measurements

A. AES Depth Profile

To measure the compositional uniformity of the evaporated film, an AES depth profile was performed on the nominal 45 wt.% Cr sample using a Leybold-Heraeus LHS-10 UHV surface analysis system. The weight percentage of Cr content was calculated and plotted as a function of sputter time in Fig. 2. AES analysis showed that a significant amount of SiO (about 50 percent) decomposed into Si and O during e-beam evaporation. However, measurement of the electrical conduction in an e-beam-evaporated SiO film (no Cr) showed very high sheet resistance, and it is concluded that the decomposed Si does not contribute to the electrical conduction of the cermet film. No significant change of Cr content profile was observed after annealing.

Maintaining an evaporation rate of 5 to 8 Å/s gave a

TABLE I
THICKNESS, VALUES OF PARAMETERS R_0, E_a, AND ROOM-TEMPERATURE SHEET RESISTANCE OF Cr-SiO CERMET FILMS BEFORE AND AFTER ANNEALING WITH VARIOUS CHROMIUM CONTENTS IN THE POWDER SOURCE

Sample	Cr wt. %	Thickness (Å)	$R_\square$ at 300 K (MΩ/□)		R_0 (KΩ/□)		E_c (meV)	
			Before Annealing	After Annealing	Before Annealing	After Annealing	Before Annealing	After Annealing
A	30	3500	2.82	6.81	0.64	35.4	345	136
B	45	2900	0.25	2.66	1.12	24.9	144	80
C	50	850	1.22	2.42	7.33	37.1	128	85

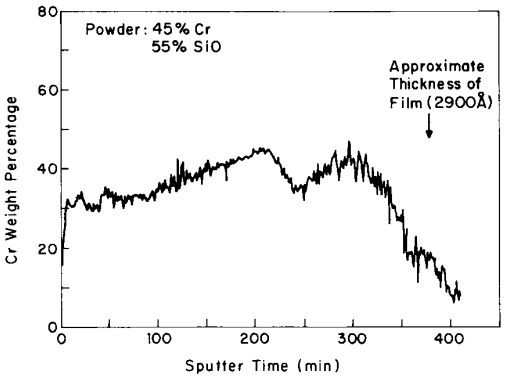


Fig. 2. AES measurement of weight percentage of Cr in the cermet film deposited from 45 wt.% Cr-55 wt.% SiO powder source as a function of sputtering time.

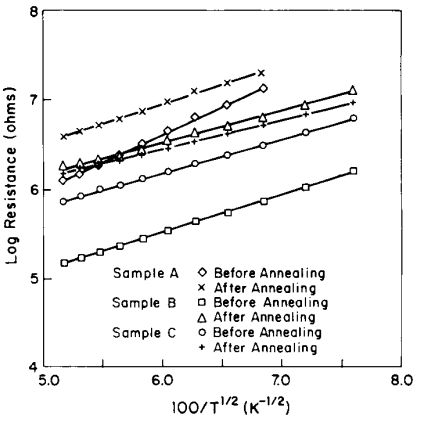


Fig. 3. Temperature dependence of the sheet resistance of cermet films before and after annealing.

cermet Cr content slightly less than that of the powder source. Although the Cr content increased with increasing evaporation rate, evaporation with higher rates (>10 Å/s) produces spitting of the powder source.

B. Sheet Resistance of Cermet

The thickness of each film was measured by a Tencor Alpha-Step 200. The composition, thickness, and sheet resistance of the films at room temperature before and after annealing is shown in Table I. The temperature dependence of the sheet resistance was measured in a nitrogen-cooled cryostat. With an applied electric field of approximately 2 V/cm, the sheet resistance of the films as a function of temperature before and after annealing is shown in Fig. 3. A conduction mechanism of a cermet at low electric fields was proposed by Neugebauer and Webb [13]. Since the electric field applied for the measurement is low and the temperature is low as well, the resistance of these films can be expressed by the following equation [9]:

$$R(T) = R_0 \exp\left\{(E_c/kT)^{1/2}\right\} \qquad (1)$$

where E_c is the constant related to the microscopic structure of the film.

The characteristics of the cermet films fabricated are in good agreement with this equation. The R_0 and E_c values are also shown in Table I. Annealing at 425°C for 45 s in forming gas ambient significantly affects these values, and may be due to a change in the structure of the metal grain [8], [9].

C. Cr-SiO Cermet/GaAs Schottky Diode Characteristics

Cermet/GaAs Schottky contacts were fabricated on n-type GaAs substrates of two different doping concentrations. Capacitance-voltage analysis showed their doping concentration to be $2.3 \times 10^{17}/\text{cm}^3$ and $2.0 \times 10^{16}/\text{cm}^3$. The area of the diodes was 2×10^{-3} cm^2. The composition of cermet was 45 wt.% Cr-55 wt.% SiO. The current-voltage characteristics of cermet/GaAs diodes and Cr/GaAs diodes before and after annealing are shown in Fig. 4, and the electrical parameters of cermet/GaAs diodes that are fitted using a thermionic emission model are listed in Table II.

Reverse leakage current of cermet/GaAs diodes was less than that of other diodes before annealing. After annealing, reduction of the leakage current was observed for each diode, but the leakage current of cermet/GaAs diodes was reduced significantly more than the other diodes. The reduction of leakage current is attributed to the increase of the Schottky-barrier height. The ideality factor increased slightly after annealing, which is reasonable since the thermionic current is reduced to the point where other conduction currents come into effect. Prior to annealing, the forward bias characteristic of the cermet/GaAs diodes showed higher series resistance than other diodes, which was reduced after annealing. Al-cermet contact resistance is the most likely cause of the anomalous pre-anneal series resistance.

TABLE II
ELECTRICAL PARAMETERS OF CERMET/GAAS SCHOTTKY DIODES WITH DIFFERENT DOPING DENSITIES BEFORE AND AFTER ANNEALING

Doping Density	$2.0\times10^{16}/cm^3$		$2.3\times10^{17}/cm^3$	
Annealing	Before	After	Before	After
Barrier Height (V)	0.70	0.85	0.64	0.77
Ideality Factor	1.00	1.06	1.00	1.21
Leakage Current (A/cm^2) at -3 V	2.0×10^{-5}	1.5×10^{-7}	2.2×10^{-3}	1.0×10^{-5}

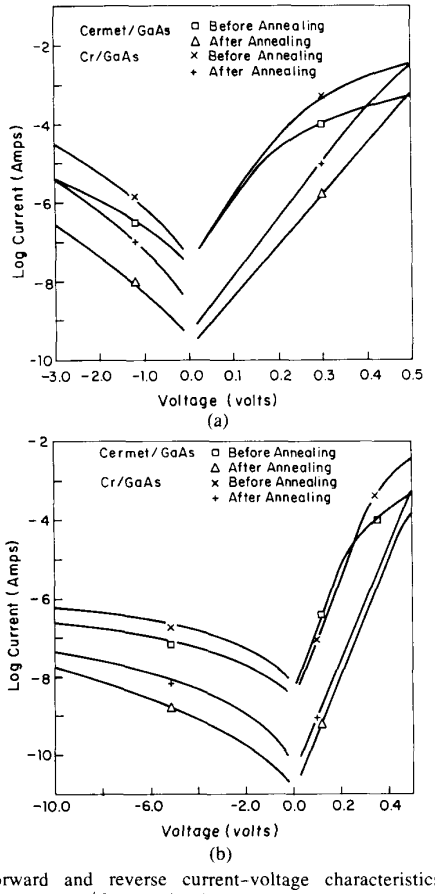


Fig. 4. Forward and reverse current-voltage characteristics of cermet/GaAs and Cr/GaAs Schottky diodes. The area of the diodes is 2×10^{-3} cm^2. Note voltage axis scale change at origin. (a) Substrate doping concentration of $2.3 \times 10^{17}/cm^3$. (b) Substrate doping concentration of $2.0 \times 10^{16}/cm^3$.

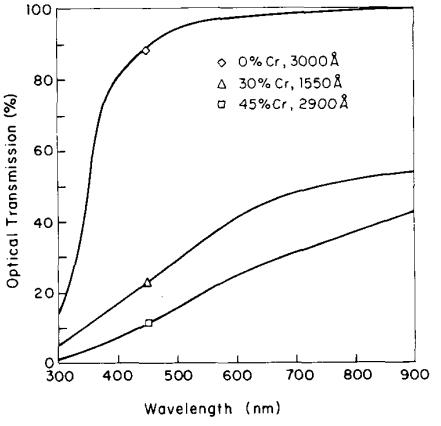


Fig. 5. Optical transmission of cermet films and SiO film as a function of wavelength. (corrected for glass substrate).

D. Optical Transmission of Cermet

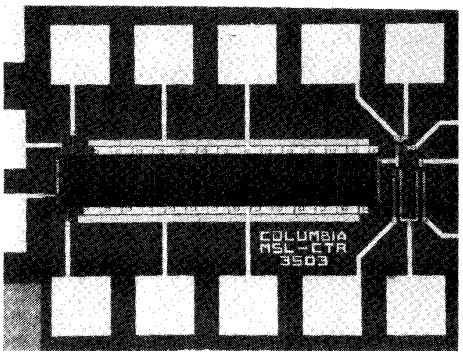
The optical transmission of the cermet films was measured by an IBM 9420 UV-Visible Spectrophotometer with a wavelength ranging from 300 to 900 nm and corrected for substrate absorption. The transmission of the cermet films and that of an SiO film are shown in Fig. 5. It suggests that most of the absorption is due to the granular metal.

IV. DISCUSSION AND CONCLUSION

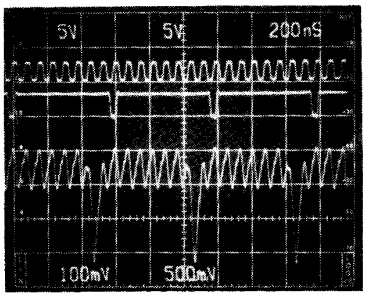
The AES depth profile of the Cr content in the cermet film shows less than a 10-percent compositional nonuniformity. Maintaining an optimal evaporation rate during evaporation is important to produce a uniform film composition. The use of mixed powders as an evaporation source is a convenient way to find an optimum cermet composition, but sputtering a cermet target or co-sputtering metal and dielectric targets may produce more uniform films.

Electrical conduction in a cermet shows a semiconductor-like behavior for temperatures between 50 to 370 K. Since the sheet resistance of the film changes quite dramatically with temperature, correction of the resistance value of the pilot sample used to stop the evaporation is necessary for those devices operating at higher or lower than room temperature. Another possibility for the temperature stabilization of sheet resistance is to anneal the film for a longer time (450°C, 2 h) [12], making the transport characteristics semiconductor-like at low temperature but metal-like at higher temperature, producing less resistance variation with temperature.

Cermet/GaAs, Al/GaAs, Cr/GaAs Schottky contacts are fabricated and current-voltage characteristics are measured and compared. The current-voltage characteristics of the cermet/GaAs, Al/GaAs, and Cr/GaAs Schottky diodes before annealing are almost the same, which can be attributed to the Fermi-level pinning of the GaAs and metal interface. However, annealing the cermet/GaAs diode at 425°C as short as 45 s reduces reverse leakage current by nearly two orders of magnitude, producing better Schottky-diode characteristics than those of annealed Al and Cr Schottky diodes. Annealing also reduces contact resistance to the cermet.



(a)



(b)

Fig. 6. (a) Photograph of resistive-gate CCD delay line with 15 stages of four-phase electrodes. The channel is 100 μm wide and the electrodes are 1 μm wide spaced by 10 μm. The doping density of the channel is $2.0 \times 10^{17}/\text{cm}^3$, and thickness is 0.16 μm. The sheet resistance of the cermet was 850 kΩ/ and 1200 Å thick. (b) Waveforms of delay line operated at 13-MHz clock frequency. Upper, middle, and bottom waveforms are one of the clock signals, input signal, and output signal of read-out amplifier, respectively.

To demonstrate the performance of the e-beam-evaporated Cr-SiO cermet thin film, a resistive-gate GaAs CCD delay line was fabricated and tested at relatively low clock frequency to observe the effect of the cermet/GaAs diode leakage current on the device performance. The photograph and waveforms of the delay line are shown in Fig. 6. The effect of leakage current was not observed at frequencies as low as several hundred kilohertz clock signals. The charge transfer efficiency (CTE) of this device was better than 99.9 percent at 13-MHz clock frequency. As demonstrated by the device application, the excellent Cr-SiO cermet/GaAs Schottky contact property shows promise for use as a resistive layer in high-performance resistive-gate CCD's.

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Prof. Fossum organized the 1986 IEEE Workshop on Charge-Coupled Devices. He has received the IBM Faculty Development Award and the Analog Devices Career Development Award. In 1986, he received the National Science Foundation Presidential Young Investigator Award.

Theoretical Study of the Piezoelectric Effect on GaAs MESFET's on (100), (011), and $(\bar{1}\bar{1}\bar{1})$Ga, and (111)As Substrates

TSUKASA ONODERA AND HIDETOSHI NISHI

Abstract—**This paper discusses the influence of piezoelectric charge on GaAs MESFET's fabricated on (100), (011), and $(\bar{1}\bar{1}\bar{1})$Ga, and (111)As substrates. We use a two-dimensional device simulation, including a piezoelectric charge model with an edge-force approximation. We found that piezoelectric charge has very little influence on GaAs MESFET's fabricated on (011) substrates. Furthermore, the threshold voltage shift of MESFET's on $(\bar{1}\bar{1}\bar{1})$Ga has the opposite sign as those on a (111)As plane substrate. We also found that orientation effects are much smaller for substrates other than the (100) substrate. This indicates the potential of orientation-effect free alignment of FET's in high-speed GaAs LSI's with (011) or (111) substrates.**

I. Introduction

THE electrical characteristics of GaAs MESFET's fabricated on the (100) substrate depend on the orientation of the gate finger [1]. The stress-enhanced preferential diffusion model [1]–[3] and the piezoelectric effect model [4], [5] were proposed to explain this. We confirmed that the piezoelectric effect was the main cause of orientation effects by observing the gate-orientation dependence of GaAs MESFET parameters, which is related to the sign of the internal stress in the dielectric overlayer [6]. Because a high degree of threshold voltage control for GaAs LSI fabrication is important, there has been much interest in the piezoelectric effect. Two-dimensional device analysis shows that the change in MESFET characteristics is due to the change in the effective thickness of the channel, which is caused by a potential barrier of piezoelectric charge [7]. External stress also affects GaAs MESFET characteristics [8]. Recently, measurements of external stress are compared with calculations, based on two-dimensional finite-element analysis for mechanical stress and one-dimensional device analysis [9].

With gate lengths of 2.0 μm or less, the piezoelectric effect improves device parameters for a certain combination of gate orientation and dielectric overlayer. It reduces the gate length dependence and improves the K-value and subthreshold characteristics [6], [10]. However, the orientation effect still limits GaAs IC layout.

This paper shows that (011) and $(\bar{1}\bar{1}\bar{1})$Ga or (111)As plane substrates can achieve orientation-independent GaAs MESFET characteristics.

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II. Theory

We used a two-dimensional device simulator [7] to analyze the piezoelectric effect on MESFET's fabricated on various GaAs substrates. We used the concentrated edge-force approximation [11] to calculate the stress distribution in the substrate. We have generalized the model equations derived by Asbeck *et al.* to calculate the piezoelectric charge distribution for [011] and [$0\bar{1}1$]-oriented FET's on a (100) GaAs substrate, for the calculation of those for FET's along with arbitrary orientations on various planes of a GaAs substrate. The simulator consists of four major parts.

The first part calculates the two-dimensional distribution of the stress tensor σ, or in vector-like notation $\boldsymbol{T}$, in the vicinity of the MESFET on a GaAs substrate. The cause of the stress in the substrate is assumed to be the stress in both the dielectric overlayer [4]–[7] and the gate electrode [8]. When a stressed overlayer is deposited on the surface of a substrate, the stress on the substrate is intensified near the discontinuities in overlayer thickness [12]. The concentrated edge force f_E represents the intensified stress at the edge of discontinuities. For the edge of the Schottky-gate electrode of the WSi_x-gate self-aligned GaAs MESFET, shown in Fig. 1, f_E is modeled by (1), the sum of intensified stress due to the dielectric overlayer σ_f, and the gate metal σ_g.

$$f_E = \sigma_f d_f + \sigma_g d_g. \tag{1}$$

Here, d_f represents the thickness of the dielectric overlayer and d_g the thickness of the gate metal. Because of the negligibly small stress in WSi_x with 60-percent Si content [13], we only accounted for the stress in the dielectric overlayer. We approximate that the gate width W_g is much larger than gate length L_g, and assume that the GaAs substrate is elastically isotropic; the six elements of the stress