

CMOS Evolution:

THE DIGITAL CAMERA-ON-A-CHIP GETS ACTIVE

Active Pixel Sensor CMOS imaging tech, developed at the Jet Propulsion Lab, is now commercialized into awaited "camera-on-a-chip" apps. The inside story.

By Dr. Eric R. Fossum

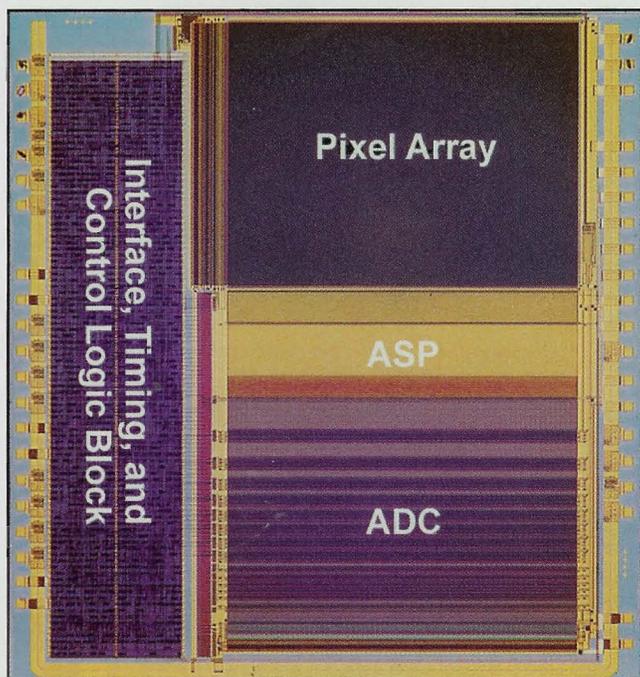


Figure 1. Photobit 1/4" format 512x384 element digital color camera-on-a-chip with pixel array, analog signal processor (ASP), analog-to-digital converter and on-chip interface, timing, control and smart function digital block.

techniques. This is because the camera is basically a single chip and a lens, although other digital signal processing (DSP) chips might be added to the system to provide for compression and interface functions. Miniaturization is important for many portable

applications such as digital still cameras, laptop computers, PDAs and automobiles, as well as for unobtrusive cameras in desktop videoconferencing and other fixed-camera uses.

A second major advantage is cost. While CCDs and CMOS image sensors might be priced competitively (especially now that CMOS image sensors are competing on the market), a CMOS APS camera system can be much less than a CCD camera system. This is because CCD camera systems require many supporting components such as timing

generators and signal processing chips to complete the system. These various ancillary chips add to the component cost and manufacturing cost of a CCD system. In a CMOS APS camera system, these functions are all integrated onto a single chip, keeping component and manufacturing costs low.

A third significant advantage of the CMOS APS camera-on-a-chip is reduced power consumption. Because the entire system is integrated on a single chip, the power required for inter-chip I/O in a CCD system is eliminated. Another source of power consumption in a CCD system is the large and varied voltage levels required by CCD driving circuitry. Each power supply in a CCD system results in power inefficiency, and since power is voltage X current (IV), or capacitance X voltage X voltage X frequency (CV^2f), the use of higher voltages in a CCD system has a direct impact on power dissipation. Low voltage CMOS (e.g. 3.3V) technology can reduce power. Typically, a complete CMOS APS camera-on-a-chip with digital output dissipates under 75 mW.

There are other advantages associated with the CMOS APS technology. A key advantage is functionality. Because the APS technology allows for nearly random access to each pixel, many functions previously difficult to implement with CCDs can be readily performed with the APS technology, such as

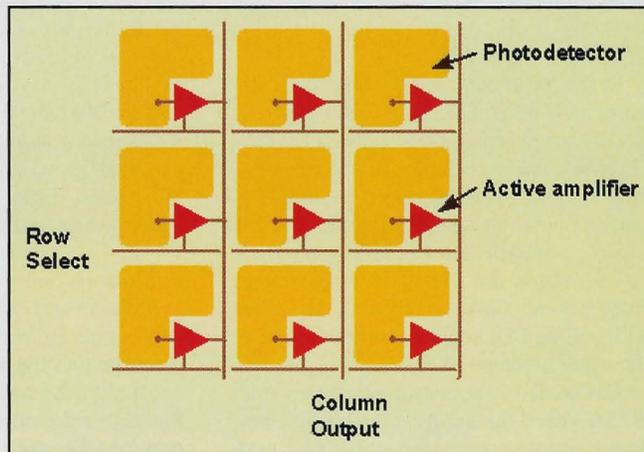
The digital camera-on-a-chip, based on CMOS active pixel sensor (APS) technology, is now entering the marketplace.

The digital camera-on-a-chip has a full digital interface so that there are no analog signals going into the chip or coming out of it. Supply voltage biases other than V_{DD} (e.g. 3.3 V) are generated on-chip or through simple resistor dividers. The chip has a serial interface for setting up its operational mode and reading out control status registers internal to the chip. Output pixel data is digital with embedded digital line and frame sync signals.

This system-on-a-chip is a major advance for camera system designers for many reasons. First, the camera can be easily miniaturized without resorting to exotic packaging

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Figure 2. Active pixel sensors have an amplifier built into every pixel for lower noise and faster readout.



readout of small windows of interest for machine vision and tracking applications, electronic pan and zoom for consumer applications and ultra high intrasene dynamic range imaging.

Background: How did we get here?

There are several important forces that have brought the CMOS APS camera-on-a-chip to the forefront of advanced imaging attention. MOS-type image sensors had their genesis in the late 1960's. Both passive and active pixels were examined, but the performance of the early MOS technology was poor and consequently image quality of the sensors was concomitantly poor and unreliable.

When the CCD was invented in late 1969, its charge domain operation solved many of



Figure 3. Photobit's 10 cm² dental X-ray sensor is in volume production for a custom-design customer. (Radiograph courtesy of Schick Technologies)

the operational problems of MOS image sensors. Since then, CCDs have achieved extraordinarily high levels of performance with low readout noise, high dynamic range and excellent responsivity. Like the marvel of Boeing 747 flight, the CCD is highly complex and its functionality is a testament to nearly 30 years of superb engineering evolution. Any other imaging technology, such as CMOS APS, must achieve similar levels of performance to displace CCD technology, or have other overwhelming advantages such as very low power or new functions.

CMOS out of the JPL

In the early 1990's, two independently motivated efforts led to a resurgence in CMOS image sensor development. The first effort was to create highly functional single-chip imaging systems where low cost, not performance, was the driving factor. This effort was spearheaded by separate researchers at the University of Edinburgh in Scotland (later becoming the firm VISION) and Linkoping University in Sweden (later becoming IVP).

The second independent effort grew from NASA's need for highly miniaturized, low-power, instrument imaging systems for next-

generation deep space exploration spacecraft. Such imaging systems are driven by performance, not cost. This latter effort was led by our group at the U.S. Jet Propulsion Laboratory with subsequent transfer of the technology to AT&T Bell Labs (Lucent), Kodak, Intel, National Semiconductor and several other major U.S. companies, and the startup of Photobit. The convergence of the efforts, combined with customer demand for miniaturized, low-power and cost-effective imaging systems, has led to significant advances in CMOS image sensors and the development of the CMOS APS camera-on-a-chip.

The CMOS APS achieves high imaging performance for two reasons. First, unlike the passive pixel, the active pixel provides *gain* within the pixel. Charge that is generated by pixel illumination is amplified during readout and used by analog signal processing (ASP) circuits at the bottom of each column. Second, unlike its early MOS predecessors, our approach to CMOS APS uses correlated double sampling (CDS) to achieve higher quality images. The use of CDS has two important advantages. It reduces temporal noise from the pixel readout circuitry, and it suppresses fixed pattern noise (FPN) from the in-pixel amplifiers. It was this combination of active pixel plus column-parallel ASP circuits that led to the first high performance CMOS APS, demonstrated by our group at JPL in 1993.

Contributing to the recent activity in CMOS image sensors is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has outpaced similar improvements in CCD technology. Furthermore, sensor pixel size is limited by both optical physics and optics cost, making moot the CCD's inherent pixel size advantage for most applications. Recent progress in on-chip signal processing (and off-chip DSP) has also reduced CMOS image sensor FPN to acceptable levels. In addition, the transition from analog imaging and display systems to digital cameras tethered to PCs permits digital FPN correction with negligible system impact.

Two camps now

At the present time there are two philosophical camps in digital cameras-on-a-chip, depending on the application of the chip. In one camp (advocates include Intel, Kodak and Photobit) color interpolation and image compression takes place off the chip in a host com-

puter or sister video processing chips. This approach permits adaptive processing to meet a wide variety of applications, but requires a sister chip or computer. It is a particularly important approach when interface bandwidth is limited (e.g. USB or Firewire) since video chips produce a large amount of data and color interpolation triples that data volume.

At the June 1997 IEEE Workshop on CCDs and Advanced Image Sensors in Brugge, Belgium, the Jet Propulsion Laboratory described a very low power 256x256 element sensor designed for NASA space applications with a serial interface for both command and data output, on-chip DACs for programmable internal biases (e.g. ADC reference) and self-calibrating ADCs. At the August 1997 Hot Chips Symposium at Stanford, Photobit announced its optical format 512x384 digital color camera-on-a-chip. This sensor delivers 8b raw data at 3-39 full frame/s (programmable) using on-chip analog to digital converters and features a serial interface port for controlling window of interest size and position, on-chip autoexposure logic and low power operation.

The second camp advocates putting as much of the color interpolation and other digital signal processing on the same chip as the image sensor. This is important for a variety of stand-alone applications and for direct replacement of CCD-based digital camera systems. For example, at the 1997 International Solid-State Circuits Conference (ISSCC) in San Francisco, a paper by Matsushita described a research project where a low resolution sensor was integrated with ADC and DCT compression circuitry. At the 1998 ISSCC, Lucent Technologies will present a paper on an experimental 352x288 CMOS APS with on-chip digital color interpolation operating at 30 frame/s. At the same meeting, VLSI Vision will present a 306x244 single-chip color camera with analog composite color video NTSC output encoding.

In addition to mainstream market applications, there are many niche applications for CMOS imaging technology. Photobit offers a custom image sensor design service for particular applications that can benefit from a tailored CMOS APS design, and has delivered numerous sensors to high profile customers such as Kodak, Lucent and ITT.

One interesting application area is in medical X-rays. At the 1998 ISSCC, Photobit will present a paper on a CMOS dental X-ray chip it developed with a strategic partner over the past few years. This "camera-on-a-chip" is probably one of the world's largest commercial CMOS chips, measuring over 37mm x 28mm (>10 cm²). The chip, placed in the patient's mouth, detects the onset of X-ray irradiation, integrates the X-ray image, and self-initiates the readout of the pixel data and a subsequent dark reference frame. (See picture above)

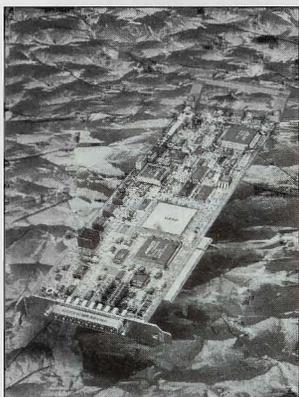
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with up to four hosts and up to eight disk drive channels. Active/Active Redundant Controller support provides failover protection for mission-critical apps, while the remote Dial-In capability allows system setup, diagnostics and maintenance procedures to be performed from remote locations. Half and full-height systems in tower or rackmount configurations features environmental monitoring and alert systems, redundant hot swappable power supplies and fans and automatic remote fault-notification. Supports RAID Levels 0, 1, 0+1, 3 & 5 concurrently. Systems are scalable to 19+ Terabytes. CYBERSTORAGE SYSTEMS, INC.

CIRCLE 213

PROGRAMMABLE FRAME GRABBER

The HI*DEF Accura is a programmable high speed frame grabber that captures video from any non-standard video source and provides digital images for mission critical applications. The HI*DEF Accura



offers four software selectable inputs to capture high-speed analog signals in real-time with programmable analog sampling rates up to 140 MHz with less than ±500 picoseconds of jitter. The Accura

can be connected to four different analog sources such as outputs from CT, MR, Ultrasound, and Nuclear Medicine devices. Plus, it also captures color images from non-interlaced computer displays up to 1280x1024@75Hz. IMAGRAPH

CIRCLE 214

1.3K X 1K PROGRESSIVE SCAN

The TM-1300 is a 10-bit camera that features a 1300(H) x 1030(V), 2/3" format interline type progressive scan CCD with the capability to asynchronously capture images of objects in motion. The TM-



1300 scans at a 12 frame/sec. rate and features an internal converter which outputs a real-time 45fps signal for display on an SXGA monitor. An internal 8-bit frame store captures and holds randomly triggered images for playout to storage

media or an image processing system. Also, an RS-232C port permits remote control of camera functions. Apps include machine vision, surveillance, archiving, medical imaging, etc. PULNIX

CIRCLE 215

C++ GRAPHICAL IMAGING

Image ++ is an object oriented graphical development tool for C++ image processing applications running under Windows 95 or Windows NT. The package allows the user to build up a block diagram of their image processing algorithm and see the results. Functions can then be modified if required at C++ source code level to fine tune the algorithm. Microsoft Visual C++ and Borland C++ are supported with source code editing and compilation. A library of over 50 image processing functions are also provided in the package. KANE COMPUTING

CIRCLE 216

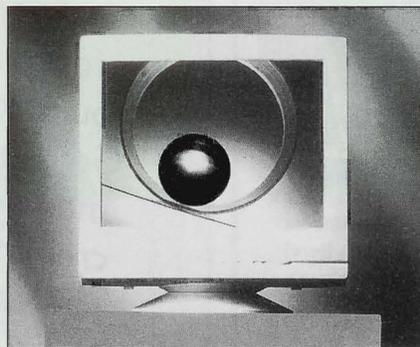
HI-RES MICRO CAMERA

Recently introduced is a micro-camera system for microscopy, achieving a 1.4 Million pixel resolution through a special color CCD hi-res digital camera with a 2/3" Vacancy Transfer imager. This system is a low-cost solution to a variety of microscopy apps. Various lenses are available in addition to a C-mount adapter, allowing for stand-alone use or in conjunction with a conventional microscope. A digital printer is available that produces near photo quality hard-copy and image archiving software brings images into the PC for processing, storage and network output. SCALAR AMERICA

CIRCLE 217

ON-SCREEN MENU CRTS

The 17" P70 is an upgraded version of the P-17 with improved horizontal frequency and additional controls for rotation adjustment and color temperature. It



features an ultra-fine 0.25mm dot pitch, 16" diagonal viewing area and 1600 x 1280 max resolution. The P70 is TCO92-compliant and incorporates DQ-DAF electronic gun technology which produces 20 percent less spot aberration than conventional guns. The 15"

P50 has a new crystal pigment tube that offers better contrast, more uniform color reproduction and lower power consumption than shadow-mask tubes. The P50 has digital on-screen controls, a .27mm dot pitch, up to 1280 x 1024 res and is TCO 92-compliant. PANASONIC COMPUTER PERIPHERAL COMPANY

CIRCLE 218

LINEAR CCD W/ANALOG

The XRD4417 is a linear CCD digitizing sub-system for flat-bed and sheet-fed scanners, as well as multifunction printers and CCD imagers. It's CCD interface circuitry requires only an external decoupling capacitor to perform correlated double sampling (CDS) of an input signal. A 6-bit programmable gain amplifier (PGA) in the device increases the signal to the appropriate level to match the 10-bit A/D converter input range. The XRD4417 samples at 1.54 million samples per second and offers low-noise and operates from a single 5V power supply. EXAR CORPORATION

CIRCLE 219

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FOSSUM

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What's next?

The history of microelectronics teaches us that integration leads to greater reliability, lower system power and plummeting system cost/performance ratios. CMOS-based imaging systems-on-a-chip can be expected to reflect these long-standing trends as they develop over the next five years. We can expect the emergence of a plethora of imaging applications and the insertion of image capture systems in many aspects of our personal lives. Look for low-cost single-chip cameras in your car, office, home and doctor's office. Widespread video teleconferencing is inevitable as are debates over privacy versus security.

The great battle between CCDs and CMOS APS is just beginning as CMOS APS begins to not only open new markets but to absorb market segments previously "owned" by CCDs. CCD manufacturers can be expected to counter with cost reductions (as has already begun) and with lower power requirements. While CCD cameras could, in principle, be shrunk to two-chip solutions (CCD plus a do-all CMOS chip), improved functional capabilities and low power advantages are fundamental to CMOS-based imaging technology. The next five years will be interesting times, indeed. ■