CMOS Digital Camera With Parallel Analog-to-Digital Conversion Architecture

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This paper presents two implementations of a CMOS digital camera, and a low-power comparator circuit suitable for focal-plane applications.

The CMOS digital camera consists of a CMOS active pixel image sensor (APS) integrated with an array of single-slope analog-to-digital converters (ADCs). Single slope analog-to-digital (A/D) conversion was selected as it is simple and easy to implement on the focal plane since the requirements on the circuit components are not severe and the real estate requirement is moderate for low-resolution application. The digital camera employs a column parallel architecture where each column of pixels shares a single readout circuit and ADC. The image sensor consists of an array of CMOS APS pixels with row and column decoders and clock generator circuits. Both row and column decoders were designed to give full random access of the imager array to easily implement electronic pan/zoom functions. A clamping and sample/hold circuit in the readout signal chain reduces fixed pattern noise (FPN) and kTC noise from the pixel prior to A/D conversion. Each ADC consists of a comparator, and a set of output latches and control logic circuit formed using standard CMOS logic. All the ADCs share a single off-chip ramp generator and counter circuit that provides the reference signal.

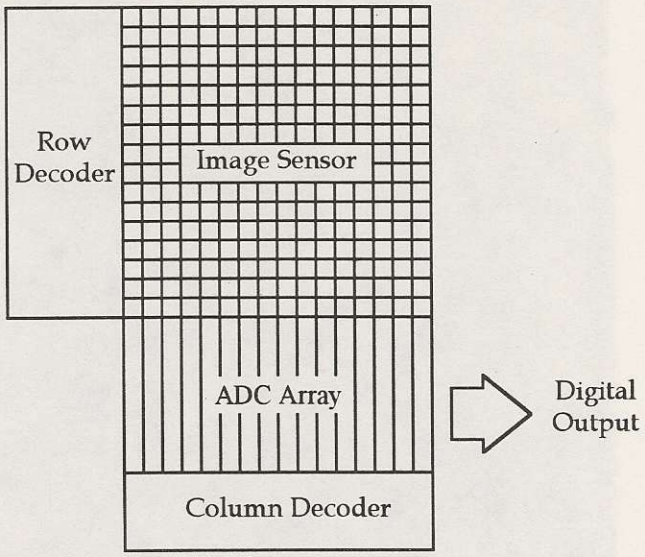
The digital camera was first demonstrated as a 32×31 test array and was fabricated using a double-poly, double-metal 2 μm n-well CMOS process. The ADC and the image sensor were designed to achieve 30 Hz frame rate operation of a 128×128 element array. The pixel size was 40 μm × 40 μm with a 26% fill-factor, and the ADC channel was 40 μm × 2.5 mm. The design was also expanded to a QCIF array (176×144

pixels) and fabricated using AT&T's 0.9 μm linear CMOS technology which is a double poly, double metal n-well process. Poly-poly coupling capacitors in the readout circuit were the only deviation from a standard digital CMOS process. The pixel size was reduced to 20 μm × 20 μm while preserving a fill-factor of 27%. The ADC channel was also scaled down to 20 μm × 1.2 mm.

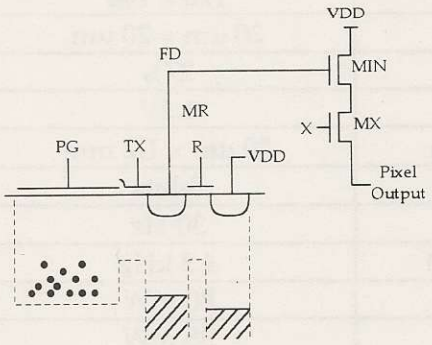
Both implementations were operated with a single 5V supply voltage and one additional d.c. voltage. Digital output with 8-bit resolution was achieved at video rate (30 Hz frame rate). The capability of achieving 10-bit resolution with the same design was also demonstrated. It was seen that on-chip A/D conversion actually reduces power dissipation on the focal plane by eliminating the large transistors needed to drive an analog output signal off the focal plane. Low-power operation was achieved with a supply voltage of 3.5V with power dissipation of 2 mW and 35 mW in the test array and QCIF array respectively. Column-wise FPN (60 mV) due to comparator offsets and capacitance mismatches was much larger than pixel-to-pixel variations. Temporal noise of the image sensor and ADCs was measured to be approximately 1 mV (r.m.s.). The ADC was characterized using a test circuit on the test array. Both differential and integral non-linearities were less than 1/2 LSB.

The low power, low complexity and low FPN requirements for the comparator used in the parallel single-slope ADC motivated a study for improvement of the comparator structure. The new comparator uses a current-mode approach for the storage of one input and reuse of the same transistors for both analog inputs (ramp and signal), thus avoiding the problem of transistor mismatch encountered in differential structures. One other major advantage of this new structure is the ability to operate in a continuous-time mode (no switching) using the fact that one of the inputs (input signal related to a pixel value) is constant during conversion. The circuit has been fabricated in a digital 0.9 μm CMOS process and is functional with a power supply down to 1.5V. The measured offset is 1 mV. The comparator fits into 20 μm for pitch matching with the pixel array (actual size: 20 μm × 200 μm).

Digital Camera Architecture



Schematic of Pixel



Schematic of Single-slope ADC

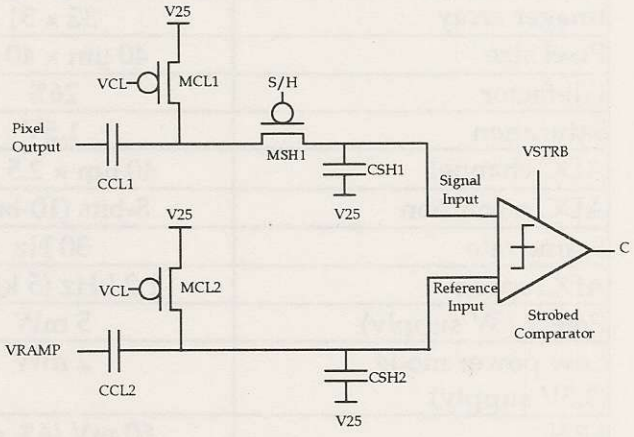
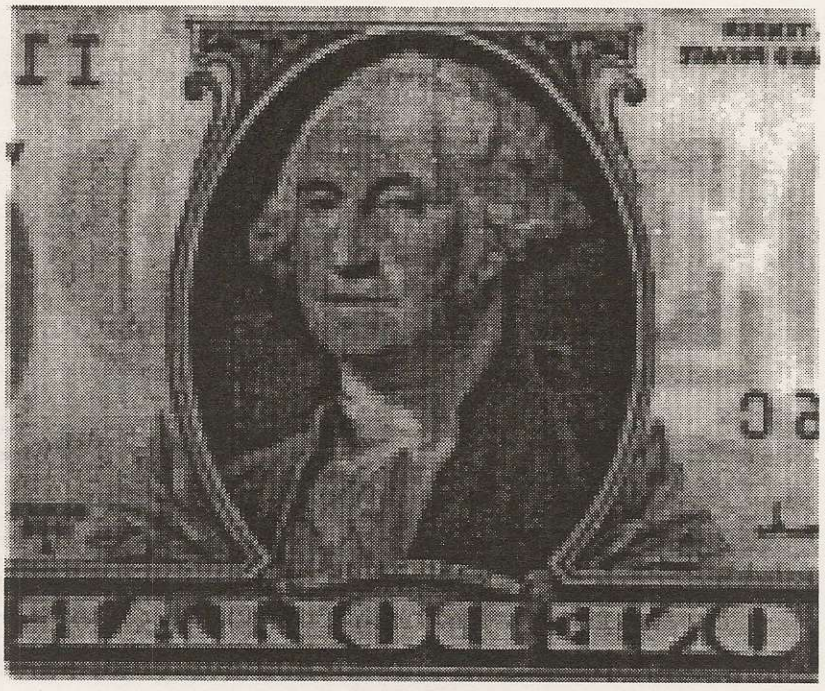


Image from Digital Camera DIGCAM1



Summary of Results

	SSADC2	DIGCAM1
Technology	2 μm n-well, double-poly, double-metal	0.9 μm n-well, double-poly, double-metal
Imager array	32 × 31	176 × 144
Pixel size	40 μm × 40 μm	20 μm × 20 μm
Fill-factor	26%	27%
Saturation	1.5V	1.2V
ADC channel	40 μm × 2.5 mm	20 μm × 1.2 mm
ADC resolution	8-bits (10-bits*)	8-bits
Frame rate	30 Hz	30 Hz
ADC speed	1.2 kHz (5 kHz*)	4.3 kHz
Power (5V supply)	5 mW	80 mW
Low power mode (3.5V supply)	2 mW	35 mW
FPN	60 mV (4% sat.)	60 mV (5% sat.)
Noise	1 mV	1 mV
Dark current	0.22 V/s	0.36 V/s
Differential non-linearity	< 1/2 LSB*	
Integral non-linearity	< 1/2 LSB*	

* Measured on test ADC in the last column of the test array.