CCD IMAGE SENSOR WITH DIFFERENTIAL, PYRAMIDAL OUTPUT FOR LOSSLESS IMAGE COMPRESSION

Sabrina Kemeny*, Habib Torby, Henry Meadows
Columbia University, EE Dept., 1312 Mudd Building, New York, NY 10027

Richard Bredthauer, Melanie LaShell
Ford Aerospace, Ford Road, Newport Beach, CA 92658

Eric R. Fossum
JPL/California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

ABSTRACT

The first integration of a 256 x 256 buried-channel frame-transfer CCD image sensor with CCD-based reformatting circuitry to enable on-chip difference encoding for hierarchical lossless image compression is reported. The 28 frames per second pyramidal pixel output is in 3 x 3 pixel blocks with the center pixel first. The reformatting circuitry occupies 2% of the active chip area with an estimated power dissipation of 150μW at a 30 Hz frame rate.

INTRODUCTION

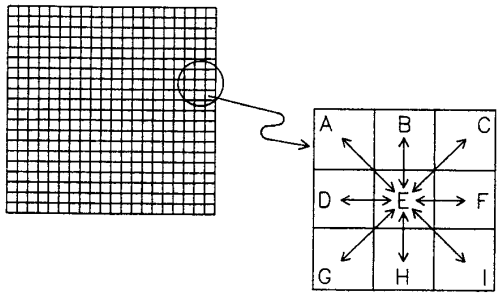
Image compression is an important element in telecommunications systems, particularly in those in which bandwidth is limited. *Lossless* compression is important in scientific and medical applications. This paper describes a novel CCD image sensor which has been specifically designed for hierarchical (pyramidal) lossless image compression and transmission.

In pyramidal image transmission, images of increasing resolution are progressively transmitted. However, a conventional CCD image sensor has a raster-scan output format. Thus, buffering of the image data must be performed by digital memory followed by subsequent access of the pixels in hierarchical order. Although not overly complex, buffer memory and digital image reorganization circuitry places additional power, weight and size burden on the transmission electronics system - an important consideration in a scientific spacecraft, for example.

Lossless compression of the reorganized image can be enhanced by encoding the intensity difference between adjacent elements in each pyramid level[1]. It has been shown by simulation that the majority of the compression (up to 86%) occurs in the lowest level (base level) of hierarchy, that is, by encoding differences between adjacent pixels in a local neighborhood (see Fig. 1).

IC ARCHITECTURE

This paper reports the first integration of a frame-transfer CCD image sensor with a CCD-based neighborhood reconstruction circuit to enable direct difference encoding of the base layer at video rates. The complete integrated circuit consists of five major portions as shown in Fig. 2. The imager sensor is a 256 x 256 three-phase CCD, adjacent to a 256 x 256 frame-storage array. A neighborhood reconstruction circuit delivers three lines of pixel data simultaneously to a pixel resequencing section. The resequencer separates the three lines into 3 x 3 blocks of pixels. The final section is the sampling output block which separates the center pixel from its eight surrounding neighbors, and provides sequential, differential output and off-chip drive capability. The IC is implemented using a triple-poly, double-metal buried n-channel CCD process. Pixel size is 15μm



Hierarchical Code:
E, E−F, E−D, E−I, E−H, E−G, E−C, E−B, E−A

Fig. 1 Hierarchical code formed by differences in intensity between the center pixel and its eight surrounding neighbors.

*present address: JPL/California Institute of Technology, 4800 Oak Grove Drive, Pasadena, CA 91109

IEEE 1991 CUSTOM INTEGRATED CIRCUITS CONFERENCE

by 15μm. The image and frame store sections occupy 3.9 mm x 7.74 mm, with the remaining circuitry occupying an additional 2% of chip area, or 0.61 mm^2.

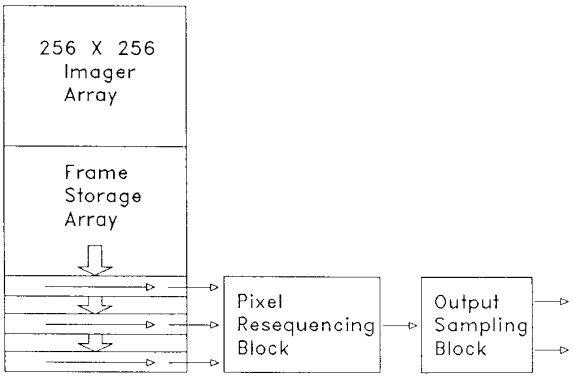


Fig. 2 Block diagram of IC architecture.

DESIGN AND OPERATION

Design and operation of the sections is now described. The image data is moved to the frame storage section following frame integration by rapidly transferring the charge in the parallel registers, as in conventional frame transfer imagers. Following frame transfer, three lines of the image are loaded into the neighborhood reconstruction (NR) registers by continued vertical parallel transfer. The three lines are then shifted horizontally by applying a channel stop bias to the vertical transfer gates. This novel architecture, which allows both the vertical and horizontal flow of charge is shown schematically in Fig. 3, and is referred to as SP^3, due to the multiple serial/parallel transfer structures. Contact to the fully symmetric horizontal shift registers' poly electrodes is made from metal bus lines running over the SP^3 structure. The three lines of image data are thus delivered in parallel to the end of this section, with pixel data in each line arriving serially. A photograph of the structure is shown in Fig. 4.

The three rows of image data are input to the pixel resequencing block which outputs a continuous serial stream of nine-pixel neighborhoods with the center pixel in each local neighborhood output first. The resequencing block utilizes the wire transfer technique[2] which combines elements of bucket brigade and CCD devices to effect the reordering of the pixels. In this technique charge packets are transferred across wires, allowing the crossing of signal paths. Fig. 5 is a photograph of the lower right hand corner of the chip showing the pixel resequencing block. A wire transfer structure is appended to the end of each of the three 256-stage serial SP^3 registers with the center and bottom row wires interchanged, such that the center row pixels are output first. Each 3 x 3 pixel block is wire transferred into a 12-stage SP^3 register which receives the packets in parallel (three at a time). The first three packets are transferred in and serially shifted up. The second (central) set of three packets are then wire transferred in and these three packets along with the first three are shifted down, such that the first stage of the 12-stage shift register contains the central packet. The final three packets are loaded

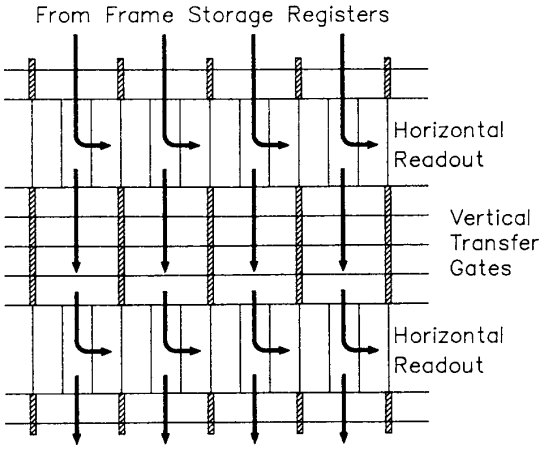


Fig. 3 Schematic of horizontal and vertical charge flow through a portion of the SP^3 structure.

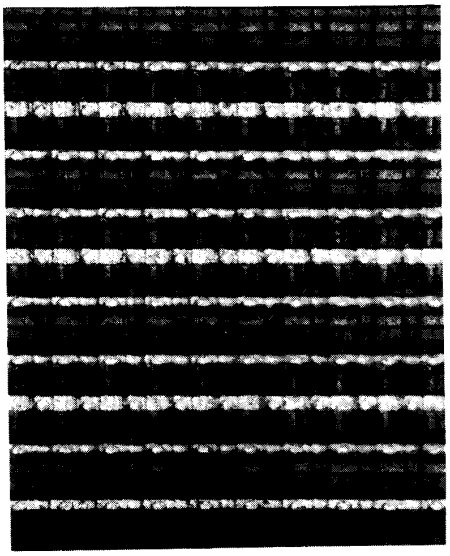


Fig. 4 Photograph of a portion of the SP^3 structure.

into the 12-stage SP^3 register and the nine pixel neighborhood is transferred in parallel to a conventional parallel-to-serial 9-stage CCD register for serial output. While the nine pixels are being transferred out of the conventional register, the subsequent nine-pixel neighborhood is reordered such that a continuous output stream is generated.

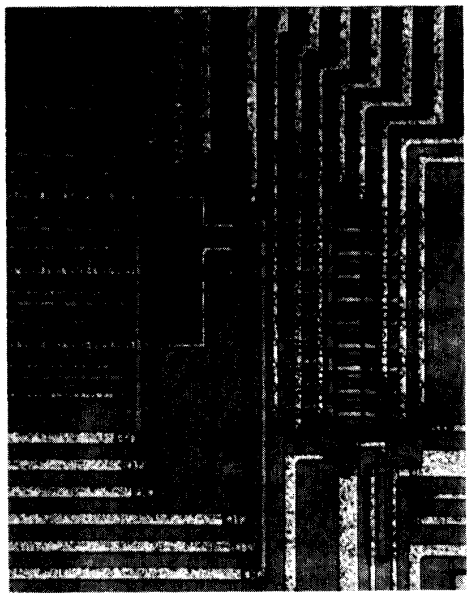


Fig. 5 Photograph of the image reorganization circuitry.

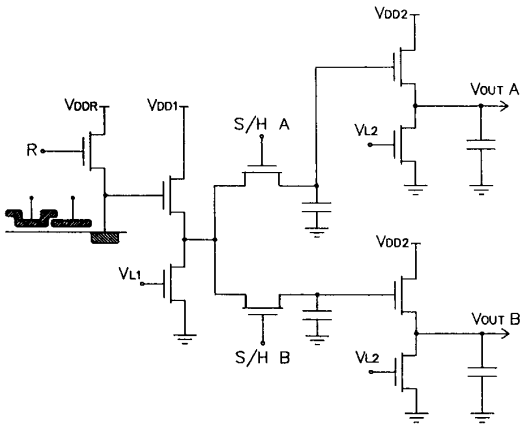


Fig. 6 Circuit diagram of output sampling stage.

The serial pixel stream is loaded into the output sampling block. This block consists of a first stage source-follower output amplifier (which can be seen in Fig. 5) followed by dual (parallel) sample-and-hold circuits (Fig. 6). The first pixel data is sampled by the upper S/H circuit. The subsequent eight pixels from the neighborhood are sampled by the lower S/H circuit. The S/H circuits are buffered by a matched pair of source-followers with active load transistors, which in turn drive the output pads. Thus the difference in output voltage between the matched circuits is proportional to the difference between the center pixel intensity and each of its surrounding neighbors.

EXPERIMENTAL RESULTS

The chip was tested both electrically and optically. The imaging and processing circuitry was operated with 5 volt three-phase clocks, yielding a total estimated dissipated power of 150μW at a 30 Hz frame rate, not including the off-chip drive amplifiers. These add an estimated 7 mW of power since they were designed to drive an oscilloscope directly (1 MΩ 22 pF load), but in principle need only drive an A/D converter.

Electrical

The circuit was tested electrically at the wafer-probe and chip level at a 277 kpixel and at a 2 Mpixel/sec output rate respectively. An additional serial-to-parallel charge electrical input structure was added above the imaging section to facilitate quantitative testing. Charge transfer efficiency in the frame transfer imager section was measured to exceed 0.99996/stage, and CTE in the horizontal SP^3 registers was measured to be 0.99991/stage at 1 Mpixel/sec and 0.9996/stage at 2 Mpixel/sec. Overall output amplifier sensitivity was measured to be 3.2μV/e^-. Intrinsic read noise levels could not be assessed due to test station noise limitations. Matching of the output amplifier pair was measured to be better than 0.05%, with some chip to chip variation observed. (Mismatch can be corrected using an off-chip preamplifier prior to A/D conversion, if needed.)

Optical

Optical testing was performed at a 2 Mpixel/sec output rate (26-28 frames/sec). A 28-85 mm Nikon lens was used to focus an image onto the chip. Raw output from the chip was first buffered by a pre-amplifier, which through gain and offset correction, provided a 0-1.5 volt signal which was then inverted and sent to a raster scan converter for display. To demonstrate functionality, a photograph taken from the screen of the scan converter is shown in Fig. 7. The larger image is a portion of the complete 256 x 256 image captured (at a

26 Hz frame rate) by multiplexing the imager output through the upper SP^3 register and bypassing the pixel resequencing circuitry. The inset image is composed of one of the eight difference-encoded elements (center pixel minus neighboring diagonal pixel) of each 3 x 3 block yielding an 80 x 80 subsampled "edge" image also generated at a 26 Hz frame rate.

Fig. 7 Demonstration of IC functionality. Photograph taken from video monitor showing portion of image sensor output when reformatting circuitry is bypassed. Inset real-time "edge" image using on-chip reformatting circuitry is described in text. (Note - actual hierarchical code of Fig. 1 not amenable to display.)

CONCLUSION

In summary, a CCD image sensor has been integrated with additional charge-domain circuitry to enable pyramidal, differential output of the image data, thus simplifying downstream electronics and reducing system size, power and weight of lossless hierarchical compression hardware. The additional circuitry occupies an additional 2% of chip area and inconsequentially increases IC power dissipation. Signal integrity is not compromised by the structure since charge transfer efficiency is high and the number of transfers is not increased. A summary of IC characteristics is given in Table 1 and a chip photograph in Fig. 8.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the technical assistance of S. Mendis during the course of this work. This work was supported by the NSF Center for Telecommunications Research at Columbia University and a NSF Presidential Young Investigator Award (ERF).

TABLE 1

IC CHARACTERISTICS AND PERFORMANCE SUMMARY

Imager architecture	*3-phase frame transfer*
Number of pixels	*256 x 256*
Pixel size	*15μm x 15μm*
Charge capacity	*100,000 electrons*
Chip area	*5.4 mm x 9.4 mm*
Imager area	*3.9 mm x 3.9 mm*
Processor area	*0.61 mm^2*
CTE vertical register	*0.99996*
CTE SP^3 register	*0.99991*
Power dissipation (excluding drive circuitry)	*150μW*
Output amplifier sensitivity	*3.2μV/electron*
Package	*68 pin leadless*

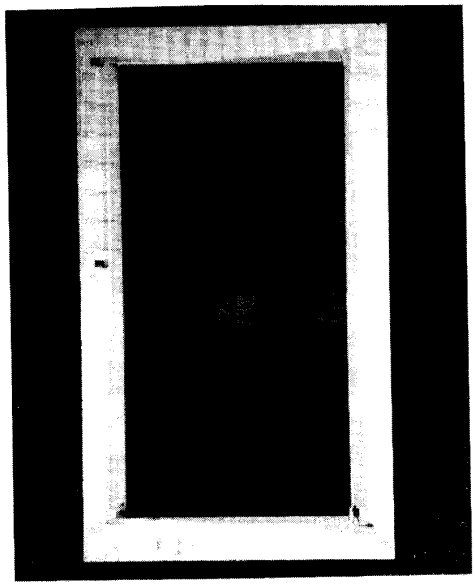


Fig. 8 Chip photograph.

REFERENCES

1. H.H Torbey and H.E. Meadows, "System for Hierarchical image coding/decoding," CTR Tech. Rep. No. 94, Columbia University (1988).
2. E.R. Fossum, "Wire transfer of Charge Packets Using a CCD-BBD Structure for Charge-Domain Signal Processing," to appear in IEEE Trans. Electron Devices, Feb. 1991.

into the 12-stage SP^3 register and the nine pixel neighborhood is transferred in parallel to a conventional parallel-to-serial 9-stage CCD register for serial output. While the nine pixels are being transferred out of the conventional register, the subsequent nine-pixel neighborhood is reordered such that a continuous output stream is generated.

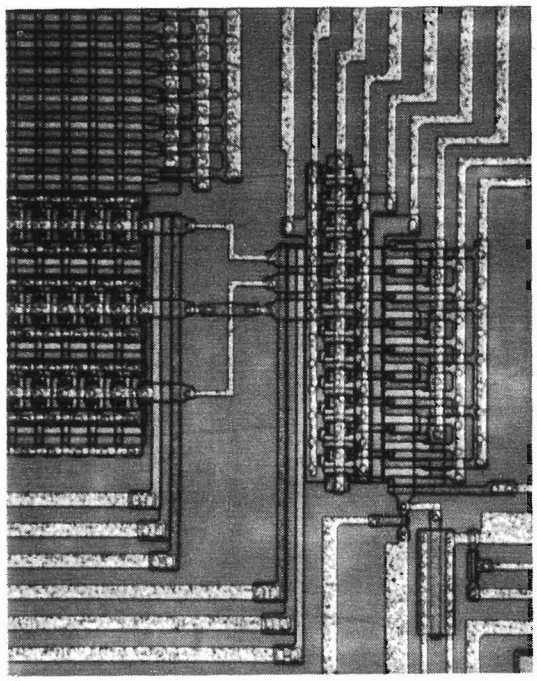


Fig. 5 Photograph of the image reorganization circuitry.

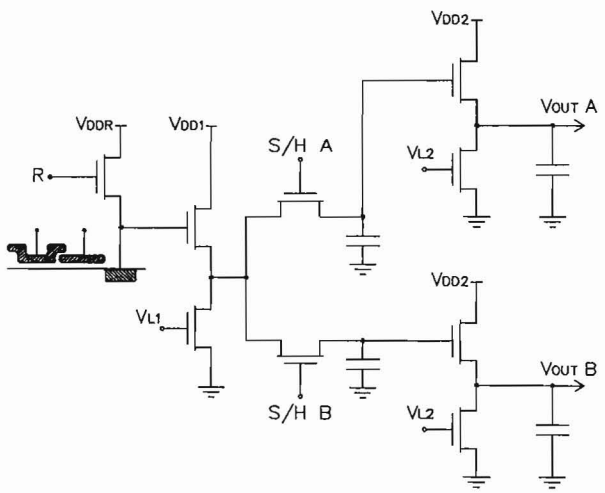


Fig. 6 Circuit diagram of output sampling stage.

The serial pixel stream is loaded into the output sampling block. This block consists of a first stage source-follower output amplifier (which can be seen in Fig. 5) followed by dual (parallel) sample-and-hold circuits (Fig. 6). The first pixel data is sampled by the upper S/H circuit. The subsequent eight pixels from the neighborhood are sampled by the lower S/H circuit. The S/H circuits are buffered by a matched pair of source-followers with active load transistors, which in turn drive the output pads. Thus the difference in output voltage between the matched circuits is proportional to the difference between the center pixel intensity and each of its surrounding neighbors.

EXPERIMENTAL RESULTS

The chip was tested both electrically and optically. The imaging and processing circuitry was operated with 5 volt three-phase clocks, yielding a total estimated dissipated power of 150μW at a 30 Hz frame rate, not including the off-chip drive amplifiers. These add an estimated 7 mW of power since they were designed to drive an oscilloscope directly (1 MΩ 22 pF load), but in principle need only drive an A/D converter.

Electrical

The circuit was tested electrically at the wafer-probe and chip level at a 277 kpixel and at a 2 Mpixel/sec output rate respectively. An additional serial-to-parallel charge electrical input structure was added above the imaging section to facilitate quantitative testing. Charge transfer efficiency in the frame transfer imager section was measured to exceed 0.99996/stage, and CTE in the horizontal SP^3 registers was measured to be 0.99991/stage at 1 Mpixel/sec and 0.9996/stage at 2 Mpixel/sec. Overall output amplifier sensitivity was measured to be 3.2μV/e$^-$. Intrinsic read noise levels could not be assessed due to test station noise limitations. Matching of the output amplifier pair was measured to be better than 0.05%, with some chip to chip variation observed. (Mismatch can be corrected using an off-chip preamplifier prior to A/D conversion, if needed.)

Optical

Optical testing was performed at a 2 Mpixel/sec output rate (26-28 frames/sec). A 28-85 mm Nikon lens was used to focus an image onto the chip. Raw output from the chip was first buffered by a pre-amplifier, which through gain and offset correction, provided a 0-1.5 volt signal which was then inverted and sent to a raster scan converter for display. To demonstrate functionality, a photograph taken from the screen of the scan converter is shown in Fig. 7. The larger image is a portion of the complete 256 x 256 image captured (at a

26 Hz frame rate) by multiplexing the imager output through the upper SP^3 register and bypassing the pixel resequencing circuitry. The inset image is composed of one of the eight difference-encoded elements (center pixel minus neighboring diagonal pixel) of each 3 x 3 block yielding an 80 x 80 subsampled "edge" image also generated at a 26 Hz frame rate.

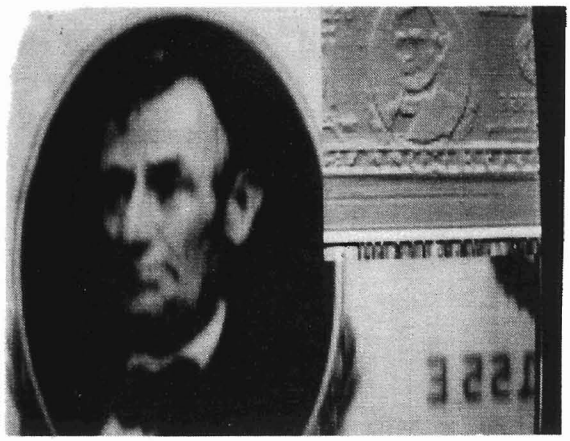


Fig. 7 Demonstration of IC functionality. Photograph taken from video monitor showing portion of image sensor output when reformatting circuitry is bypassed. Inset real-time "edge" image using on-chip reformatting circuitry is described in text. (Note - actual hierarchical code of Fig. 1 not amenable to display.)

CONCLUSION

In summary, a CCD image sensor has been integrated with additional charge-domain circuitry to enable pyramidal, differential output of the image data, thus simplifying downstream electronics and reducing system size, power and weight of lossless hierarchical compression hardware. The additional circuitry occupies an additional 2% of chip area and inconsequentially increases IC power dissipation. Signal integrity is not compromised by the structure since charge transfer efficiency is high and the number of transfers is not increased. A summary of IC characteristics is given in Table 1 and a chip photograph in Fig. 8.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the technical assistance of S. Mendis during the course of this work. This work was supported by the NSF Center for Telecommunications Research at Columbia University and a NSF Presidential Young Investigator Award (ERF).

TABLE 1

IC CHARACTERISTICS AND PERFORMANCE SUMMARY

Imager architecture	*3-phase frame transfer*
Number of pixels	*256 x 256*
Pixel size	*15μm x 15μm*
Charge capacity	*100,000 electrons*
Chip area	*5.4 mm x 9.4 mm*
Imager area	*3.9 mm x 3.9 mm*
Processor area	*0.61 mm^2*
CTE vertical register	*0.99996*
CTE SP^3 register	*0.99991*
Power dissipation (excluding drive circuitry)	*150μW*
Output amplifier sensitivity	*3.2μV/electron*
Package	*68 pin leadless*

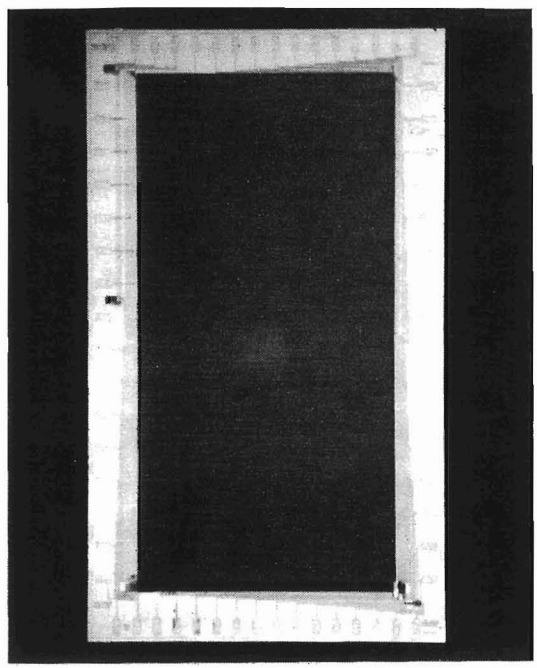


Fig. 8 Chip photograph.

REFERENCES

1. H.H Torbey and H.E. Meadows, "System for Hierarchical image coding/decoding," CTR Tech. Rep. No. 94, Columbia University (1988).
2. E.R. Fossum, "Wire transfer of Charge Packets Using a CCD-BBD Structure for Charge-Domain Signal Processing," to appear in IEEE Trans. Electron Devices, Feb. 1991.