CCD FOCAL-PLANE REAL-TIME IMAGE PROCESSOR

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ABSTRACT

A focal-plane-array chip designed for real-time, general-purpose, image preprocessing is reported. A 48 X 48 pixel detector array and a 24 X 24 processing element processor array are monolithically integrated on the chip. The analog, charge-coupled device-based VLSI chip operates in the charge domain and has sensing, storing, and computing capabilities. The chip was fabricated with a double-poly, double-metal process in a commercial CCD foundry. The simulation of an edge detection algorithm implemented by the chip is presented. An overview of the chip performance is described as well.

1. INTRODUCTION

Image preprocessing tasks can be performed using local neighborhood operations on image array picture elements (pixels). Generally, these preprocessing functions consume the greatest portion of time required by the vision process. In the course of effecting the preprocessing tasks, each pixel may undergo as many as 100 to 500 simple arithmetic operations per frame. The frame rate may range from 1 Hz in low speed systems, to 100 Hz in systems operating on a par with human vision, to 1000 to 10,000 Hz in high performance systems. The number of operations required in a 100 Hz frame rate system with a modest array size of 100 X 100 pixels could easily exceed hundreds of millions of operations per sec (Mops). Advances in very high speed integrated circuits (VHSIC) may allow serial computing systems to achieve such high throughput, but a parallel computing approach can be used to alleviate the performance requirements. Unfortunately, massively parallel computing systems are presently incompatible with the portability needs of a mobile system. Furthermore, the advantages of massively parallel systems are often offset by the problem of loading and unloading the parallel data from a serial data stream at sufficiently high data rates.

Since the image data arrives in a parallel manner and is transduced to an electrical form in parallel, it seems natural to perform spatially parallel image preprocessing on the image plane itself (as proposed by Fossum[1], Joseph et al.[2], and Beaudet[3].) It also seems natural to integrate the sensing and computing circuits on the focal plane. Charge-coupled device (CCD) structures are well-suited

for such a system. Because of its analog nature, the image data can be compactly represented in the charge domain, requiring a single electrode for storage. The image data are refreshed at the frame rate; therefore the dynamic nature of CCD signal representation is generally not a concern. Charge-transfer devices already have established themselves as a technology of choice for image data readout. The difficulty lies in the design of the charge-domain circuits.

In order to recognize the significance of integrating sensing and computing circuits on the focal plane, the following example is considered. A 128 X 128 pixel imager operates at a frame rate of 50 Hz. Each pixel may undergo as many as 250 operations per frame to implement an image processing task. The throughput requirement to process the data collected by the imager in real-time is approximately 200 Mops. A charge-coupled analog processing element (PE) operating at a modest frequency of 25 MHz yields a throughput of 1 Mops, assuming that 25 cycles are required per operation. A 14 X 14 PE array is needed to meet the 200 Mops requirement, ignoring multiplexing time. The above array sizes could be generalized to N X N pixels and M X M PEs. The size of the pixel subarray supported by each PE is n X n, where n = N/M. The integration of the two arrays, the detector array and the processor array, is the crucial step toward achieving real-time focal-plane image processing. Different planar and vertical architectures may be adopted to realize this integration (Eid and Fossum[4]).

In this paper, a CCD focal plane array analog image processor is reported. The IRET (in real-time) chip is designed for real-time, general-purpose, image preprocessing. Simulation and performance overview of IRET is described as well.

2. IRET ARCHITECTURE AND DESIGN

IRET was conceived as a vehicle for testing the integrability of the sensing and processing arrays. Planar integration of the two arrays was adopted in IRET because three-dimensional integrated circuit technology essential for vertical integration was not available to us. The unit cell array architecture was the choice for IRET first generation because it is less complex than the two-array architecture[4]. A detector array of 48 X 48 pixels and a processor array of 24 X 24 PEs are integrated monolithically on IRET. The unit cell of the integrated array consists of one PE and a subarray of 2 X 2 pixels. The PE is a set of various computing and communicating elements, and each PE supports 4 pixels.

IRET is desiged with a single-instruction, multiple-data (SIMD) architecture. In this approach, each PE in the array carries out the same instruction, but on a different piece of data depending on the position of the cell in the array. Each PE does not have to be ultra-fast to achieve real-time processing as in the case of serial approaches. A modest clock frequency of 25 MHz and a modest array size of 24 X 24 PEs achieve a total throughput as high as 576 Mops.

The size of the detector subarray supported by each PE, n, is very significant. Increasing n enhances the fill factor and improves the spatial resolution of the imager. However, n is limited by the throughput of each PE. A realistic estimate of 1 Mops/PE throughput yields n = 9 with 250 operations per pixel per frame at 50 frames per second. The unit cell size is estimated to be 495 X 495 um^2 with a detector pitch of 55 um and a detector area of 22 X 22 um^2. The choice of n = 2 reduced the complexity of the design and yielded a unit cell size of 360 X 360 um^2 with a detector pitch of 180 um and a detector area of 22 X 22 um^2.

CCD technology is the heart of this architecture (Fossum[5,6]). The capabilities of CCDs enabled integrating sensing, computing, and storing elements on the same chip. Despite the different functional orientations of these elements, they are all analog and operate in the charge domain. There is no need for A/D or D/A conversion between different stages. CCDs are digitally programmable through the sequence of applied clock waveforms and so is the array processor. The compactness of CCDs was essential in achieving high density layout. The dynamic nature of CCDs is a key factor in the estimated low power dissipation. Details of the several tradeoff issues that were involved in the design of IRET can be found elsewhere (Eid and Fossum[7,8]).

In addition to the conventional way of transferring charge in the semiconductor channel (channel charge transfer), IRET employs the unconventional way of transferring charge over wires connecting two or more semiconductor channels (wire charge transfer) described by Fossum[9]. This provides flexible layout and achieves the compactness requirement dictated by parallel architecture.

3. SIMULATION

A simulator for IRET was developed. The IRET simulator takes into account the inefficiency of channel charge transfer and wire charge transfer. It considers the different sources of noise: input shot noise of the sensor array and thermal noise due to charge transfer, charge resetting, and charge filling and spilling. It also takes into account the inaccuracy of the different computing circuits due to misalignment of fabrication masks, thermal noise, and any other source. An edge detection algorithm was implemented on the simulator. The channel and the wire charge transfer efficiencies were assumed to be 0.9999 and 0.99, respectively. The inaccuracy of the computing circuits was assumed to be 1%.

The edge as detected by IRET simulator was found to be comparable to that detected by a digital computer implementing the same algorithm[4]. The inaccuracy of the computing circuits was exaggerated to 10 % and the edge detection algorithm was once again implemented by IRET simulator. There was no visually perceived difference between the two cases[4], though the display unit and/or the halftoning routine may have limited the visual perception of any numerical difference.

4. PERFORMANCE

The basic functions of IRET are: capture of the image data, performing local neighborhood operations, and output of a serial data stream that represents the processed image. It performs the local neighborhood operations using basic arithmetic functions such as addition, subtraction, splitting, and magnitude comparison. It also uses conditional addition and subtraction; that is, addition and subtraction conditioned on magnitude comparison.

IRET is a general-purpose image processor. It can be programmed to implement various image preprocessing tasks[8], each being a convolution of the image data array with a kernel. The kernel has a central element and some surrounding ones. The shape and size of the kernel may differ depending on the nature of the task. IRET can be programmed to perform A/D conversion on the processed data prior to output.

Characterization of a test chip (2 X 2 PE array) using electrically injected signal charge packets showed that the different computing circuits in the unit cell to be functional. The capability of the unit cell to communicate with the nearest neighbor in horizontal or vertical direction was established as well. The linearity, however, seems to be lower than the estimated limit. The high capacitance of the analog bus connecting different sensing, storing, and computing circuits within the unit cell may have contributed to this problem. The lack of electrostatic screening gates in the wire transfer stages[9] used to transfer signal charge packets between different circuits may have been another cause. Comprehensive evaluation of the performance is currently underway.

Since sensing and computing circuits are integrated in the same unit cell, they are physically close to each other (in the range of 200 um X 200 um). This resulted in an unforeseen problem. Though shielded, the computing circuits were affected by light which made them unfunctional. This matter is currently under investigation. A possible reason behind this problem is the lack of proper isolation between sensing and computing circuits. Photogenerated electrons can travel for long distances (about 1.4 mm) before they recombine if are not integrated. This may contribute to the integration of photogenerated electrons by potential wells of computing rather than sensing circuits. Another possible cause is interference and/or reflection effect by incident light, particularly at wavelengths comparable to the thickness of the shielding layer.

5. CONCLUSIONS

The design of a CCD focal plane array analog image processor chip (IRET) has been described. An IRET simulator was developed and the simulated performance shows good promise. An overview of the performance was presented.

6. ACKNOWLEDGMENTS

The authors wish to gratefully acknowledge the assistance of Dr. R. Bredthauer of Ford Aerospace, Newport Beach, California, in the fabrication of IRET. This work was supported by an NSF Presidential Young Investigator Award and the NSF Center for Telecommunications Research at Columbia University.

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