

An Analysis of the Temperature Dependence of the Gate Current in Complementary Heterojunction Field-Effect Transistors

Thomas J. Cunningham, *Member, IEEE*, Eric R. Fossum, *Senior Member, IEEE*, and Steven M. Baier, *Member, IEEE*

Abstract—The temperature dependence of the gate current versus the gate voltage in complementary heterojunction field-effect transistors (CHFET's) is examined. An analysis indicates that the gate conduction is due to a combination of thermionic emission, thermionic-field emission, and conduction through a temperature-activated resistance. The thermionic-field emission is consistent with tunneling through the AlGaAs insulator. The activation energy of the resistance is consistent with the ionization energy associated with the DX center in the AlGaAs. Methods reducing the gate current are discussed.

THE complementary heterojunction field-effect transistor (CHFET) technology uses an undoped AlGaAs insulator under the gate to confine charge carriers in a GaAs or InGaAs channel [1]–[3]. This technology allows MOS-like complementary transistor capability in III–V systems with the advantages of very high channel mobility and immunity from carrier freeze-out. Such a technology holds great promise for low-noise, low-power circuitry that operates at cryogenic temperatures necessary for very low-temperature (2–4 K) imaging detector arrays such as those envisioned for the Space Infrared Telescope Facility (SIRTF). It has the disadvantage, however, that the GaAs–AlGaAs or InGaAs–AlGaAs band discontinuity which confines the channel charge presents a much lower potential barrier to carrier leakage than in the Si–SiO₂ system. This tends to result in nonnegligible gate leakage currents, which must be understood and controlled if the CHFET technology is to be successful in this analog application.

Previous attempts have been made to model the CHFET gate current as two back-to-back diodes [4]–[6], but required very unrealistic ideality factors ($n > 5$) in order to fit the measured current versus voltage (I – V) data. This paper presents the temperature dependence of the gate I – V data. An analysis of the data indicates that the conduction is due to a combination of thermionic emis-

sion, thermionic-field emission, and ohmic conduction through a temperature-activated resistance.

The structure of the CHFET is similar to that of a MODFET except that the AlGaAs layer is undoped. Starting on a semi-insulating GaAs substrate, MBE is used to grow a half-micrometer GaAs buffer, then an InGaAs channel, followed by an AlGaAs dielectric layer. All of the grown layers are undoped except for the InGaAs channel, which may be delta-doped. The experimental devices that were examined for this study used an In_yGa_{1–y}As channel thickness of 150 Å with $y = 0.25$ and $y = 0.20$ and an Al_xGa_{1–x}As dielectric thickness of 250 Å with $x = 0.50$ and $x = 0.75$. A WSi gate serves as a self-aligned mask for the source and drain implants. The implants are n-type for n-channel devices and p-type for p-channel devices. Suitable ohmic contacts are subsequently made to the source and drain. The details of the CHFET fabrication have been previously published [1], [4].

The CHFET is an enhancement-mode device whose operation is analogous to that of a silicon MOSFET. Applying a suitable gate voltage induces a charge to accumulate in the InGaAs channel by drawing carriers from the source: electrons in the case of n-channel devices and holes in the case of p-channel devices. The AlGaAs dielectric plays a role analogous to the oxide in an MOS transistor; it provides a potential barrier that confines the channel charge, preventing conduction between the channel and gate. It is expected, however, that some leakage current to the gate exists, caused by the quantum-mechanical tunneling of carriers through the potential barrier (field emission) and thermionic emission of carriers over the barrier. The magnitude of this current is expected to depend strongly on the gate voltage and the device temperature.

The I – V measurements of the gate current were made using an HP4145 semiconductor parameter analyzer with the source and drain grounded. The resulting I – V curves measured at temperatures from 10 to 290 K for a typical n-channel device are shown in Fig. 1. As expected, the current exhibits components due to field emission and thermionic emission, each of which is dominant in differ-

Manuscript received June 22, 1992.

T. J. Cunningham and E. R. Fossum are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109.

S. M. Baier is with the Honeywell Systems and Research Center, Honeywell Inc., Bloomington, MN 55420.

IEEE Log Number 9205346.

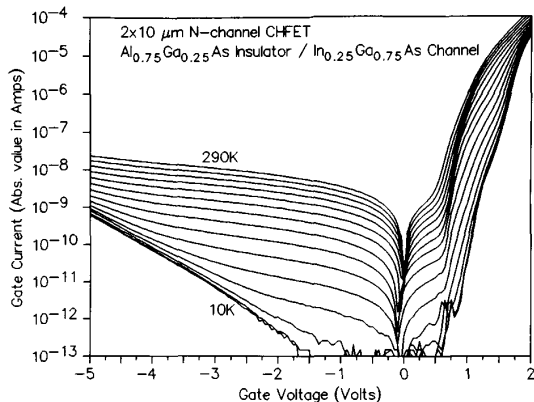


Fig. 1. The gate current as a function of gate voltage, with temperature as a parameter. Data are shown for every 20 K from 10 to 290 K. This device is a $2 \times 10\text{-}\mu\text{m}$ ($L \times W$) n-channel CHFET with a $250\text{-}\text{\AA}$ $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ dielectric layer and a $150\text{-}\text{\AA}$ $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ channel. The threshold voltage V_{TH} of this device is 0.65 V .

ent temperature and voltage ranges. In addition, there is an unexpected component due to a temperature-activated ohmic conductance, which will be described in more detail later.

The field-emission component of the total current dominates at higher voltages of either polarity. Below approximately 50 K , the current is dominated by nearly pure field emission, and exhibits little temperature dependence as the device is cooled further. Above 50 K thermal broadening results in thermionic-field emission, which increases with increasing temperature. For negative voltages the field-emission current is described reasonably well by the Fowler-Nordheim expression for field emission through a triangular barrier [7]. The barrier height derived from a least mean-square-error fit is approximately 0.48 eV . This is 28% less than the AlGaAs/GaAs direct conduction band discontinuity of 0.69 eV (for $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$), but this discrepancy is reasonable considering band filling and the nonparabolicity in the effective mass, both of which act to reduce the effective tunneling barrier. The field emission for positive voltages is not well fit by the Fowler-Nordheim expression, which is not surprising because the voltage dependence of the current is complicated by the change in the channel charge density and quasi-Fermi level with a change in voltage.

At lower voltages and higher temperatures, the current is dominated by thermally activated conduction mechanisms. For low voltages of both polarities and temperatures just below room temperature, conduction is dominated by a simple ohmic resistance with a strong temperature dependence. The gate leakage current is given simply by $I_G = V/R$ where R is given by

$$R = R_0 \exp(E_a/kT). \quad (1)$$

Separate measurements indicate that this conductance exists not only from gate to source and gate to drain, but also from source to drain on a given device as well as from

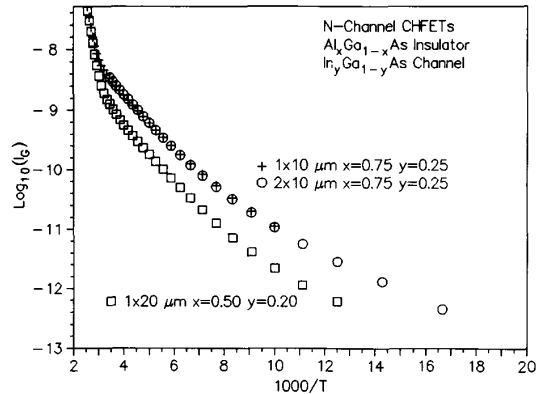


Fig. 2. An Arrhenius plot of the gate current at a fixed gate voltage of -1 V . Plots are shown for a device with an $\text{Al}_{0.50}\text{Ga}_{0.50}\text{As}$ dielectric layer and for two different devices with an $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ dielectric layer.

device to device on the same chip. In fact, this conductance acts as if it is due to a spreading resistance in that the resistance measured between any two points on the chip is approximately the same, being on the order of $10^9\ \Omega$ at room temperature. A possible explanation is that the AlGaAs dielectric layer contains some type of trap that makes the AlGaAs layer uniformly conducting across the entire chip. This is supported by the following analysis.

An Arrhenius plot of the gate current at a fixed gate voltage of -1 V for devices with different aluminum mole fractions x in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ insulator is shown in Fig. 2. The slope of the Arrhenius plot is proportional to the activation energy. The devices with $x = 0.75$ exhibit a linear portion on the Arrhenius plot for the temperature range of 290 to 180 K . The slope in this linear portion implies an activation energy of 0.095 eV . The Arrhenius plot for the device with $x = 0.50$ is not as linear as that for the devices with $x = 0.75$, but it clearly has a different slope, implying that the activation energy varies with the aluminum mole fraction, and thereby supporting the hypothesis that the AlGaAs is responsible for the conduction. The value of the activation energy is also consistent with a known defect level in AlGaAs, namely the DX center. The empirical activation energy of 0.095 eV for the devices with $x = 0.75$ is within 14% of the calculated energy of 0.081 eV for the DX level. This is calculated assuming that the AlGaAs conduction band edge lies $0.357 - 0.22(x - 0.39)\text{ eV}$ above the GaAs conduction band edge, and that the DX level lies 0.197 eV above the GaAs conduction band edge, independent of x [8]. The calculated DX level for $x = 0.50$ is 0.136 eV . The fit for the temperature range from 290 to 180 K for the device with $x = 0.50$ yields an activation energy of 0.102 which differs from the calculated value by 36%. It does show the proper trend, however, that the activation energy increases with decreasing aluminum mole fraction. Also, because of the greater curvature of the plot, the assignment of the activation energy is somewhat arbitrary. For example, if the fit

is done only for the temperature range from 290 to 250 K, the resulting activation energy is 0.127, which is within 8% of the calculated value.

Above room temperature, thermionic emission dominates conduction, as demonstrated by the change in slope of the plots in Fig. 2. The activation energies for this process are 0.435 for the devices with $x = 0.75$ and 0.440 for the device with $x = 0.50$. These values appear too small to describe emission directly over the AlGaAs barrier to the gate. It is possible that the conduction mechanism involves emission out of the source into the channel in the region surrounding the device where a large-area contact is made to the AlGaAs layer, facilitated by the thermally activated conductance mechanism described above.

An examination of the p-channel devices showed I - V characteristics analogous to those for the n-channel devices. All of the conduction mechanisms present in the n-channel devices also appeared for the p-channel devices, and conducted currents of approximately the same order of magnitude.

An understanding of these gate leakage mechanisms suggests methods for reducing the gate leakage current for device operation at various temperature ranges. The room-temperature leakage at moderate voltages should be reduced many orders of magnitude by eliminating the ohmic conduction mechanism. The field emission and thermionic components might be reduced by suitable tailoring of the AlGaAs thickness and aluminum mole fraction.

In summary, an examination of the temperature dependence of the gate leakage current implies that the gate conduction is due to a combination of thermionic-field emission, thermionic emission, and thermally activated ohmic conduction. The activation energy of the ohmic conduction is approximately 0.1 eV, which is consistent with the depth of the DX center in AlGaAs. This implies

that the room-temperature gate current at low gate bias can be reduced substantially by reducing the trap density in the AlGaAs. The device-to-device variation in the field emission was too large to allow the size dependence to indicate whether the field emission was dominated by the emission from the channel or the channel edges.

ACKNOWLEDGMENT

The research described in this paper was conducted by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The authors would like to thank Dr. A. C. Warren of the IBM T. J. Watson Research Center for the use of his heterostructure modeling program, HETMOD, and Dr. T. Krabach of JPL and Dr. J. Woodall of IBM for useful discussions.

REFERENCES

- [1] P. P. Ruden *et al.*, "AlGaAs/InGaAs/GaAs quantum well doped channel heterostructure field effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 10, p. 2171, 1990.
- [2] P. P. Ruden *et al.*, "Quantum-well p-channel AlGaAs/InGaAs/GaAs heterostructure insulated-gate field-effect transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 11, p. 2371, 1989.
- [3] D. E. Grider *et al.*, "Delta-doped complementary heterostructure FETs with high y -value pseudomorphic $\text{In}_y\text{Ga}_{1-y}\text{As}$ channels for ultra-low-power digital IC applications," in *IEDM Tech. Dig.*, 1991, p. 237.
- [4] F. L. Schuermeyer, M. Shur, and D. E. Grider, "Gate current in self-aligned n-channel and p-channel pseudomorphic heterostructure field-effect transistors," *IEEE Electron Device Lett.*, vol. 12, no. 10, p. 571, 1991.
- [5] C-H Chen, S. M. Baier, D. K. Arch, and M. S. Shur, "A new and simple model for GaAs heterojunction FET gate characteristics," *IEEE Trans. Electron Devices*, vol. 5, no. 5, p. 570, 1988.
- [6] J. H. Baek *et al.*, "New mechanism of gate current in heterostructure insulated gate field effect transistors," *IEEE Electron Device Lett.*, vol. EDL-7, no. 9, p. 519, 1986.
- [7] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, p. 403.
- [8] M. Lannoo, "Theoretical treatments of DX and EL2," *Semi. Sci. Tech.*, vol. 6, p. B16, 1991.