

An Active Pixel Sensor Fabricated Using CMOS/CCD Process Technology

Paul P. K. Lee, Russell C. Gee*, R. Michael Guidash, T-H. Lee, and Eric R. Fossum*

Microelectronics Technology Division, Eastman Kodak Company
1669 Lake Avenue, Rochester, New York 14650-2008
Tel: (716) 477-2869, Fax: (716) 477-4947, Internet: ppklee@Kodak.COM

*Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

Abstract

To improve the blue response and the dark current limitations of the active pixel sensor, a new CMOS imager has been integrated with a pinned photodiode using a mixed process technology. This technology combines an n-well 2- μm CMOS and a linear/fullframe CCD processes to provide the best features from both. Design of Experiment and Technology Computer Aided Design tools were used to develop and optimize this mixed technology. A 256 x 256 pinned photodiode active pixel sensor was designed and fabricated. The imager is 1.2 cm square with a pixel pitch of 40 μm , realizing a fill-factor of 30%. The characteristics of the CMOS/CCD technology were obtained from measurements on test circuits. The operation of the imager was verified using test structures. This work demonstrates the promise of incorporating image-sensor CCD technology in CMOS active sensor.

Introduction

This paper describes the integration of the active pixel sensor (APS) architecture normally fabricated in conventional Complementary Metal Oxide Semiconductor (CMOS) technology with a pinned photodiode (PPD) device using a mixed process technology. This new technology allows mix and match of CMOS and high performance Charged-Coupled Device (CCD) modules. The PPD [1] becomes the photoactive element in an XY-addressable area array with each pixel containing active devices for the transfer, readout, and reset functions. It is a standard photosensitive element, available in a high performance true two-phase CCD technology developed previously for CCD-based image sensors [2]. An n-well 2- μm CMOS technology was combined with the CCD process to provide the best features from both. A Design of Experiment approach was used with Technology Computer Aided Design (TCAD) tools to develop and optimize the new mixed process technology without sacrificing any CCD performance while minimizing impact to the CMOS device characteristics [3]. By replacing the polysilicon photocapacitor or photogate in conventional APS with the pinned photodiode, deficiencies in poor blue response and high dark current are minimized [4].

A 256 x 256 pixel PPDAPS was designed with a pixel pitch of 40 μm . The imager is 1.2 cm square, realizing a fill-factor of 30%. It is designed to operate with standard 5 V clock voltages. The architecture and details of the imager are presented. Considerations in the CCD/CMOS process integration are also discussed. Fabrication results show that the performance obtained with the mixed technology is comparable to the conventional processes by using measurements on conventional CCD linear image sensors and CMOS test circuits. The PPDAPS device operation is demonstrated using test structures containing the actual pixel layout from the 256 x 256 imager. This work promises improvement in APS performance by incorporating image-sensor technology in its design and fabrication.

Process Integration

Process blocks from a modular 2 μm CCD-BiCMOS technology were selected to integrate the pinned photodiode and the CMOS fabrication sequences. Starting with a double polysilicon, double metal, true two-phase CCD process designed for fabricating high performance image sensors, four masking and three ion implants steps were added to form n-well CMOS devices on the p-substrate as the CCD. During process integration and optimization, a design of experiment approach combined with 1-dimensional and 2-dimensional process and device simulation (Technology Computer Aided Design) tools were used to ensure that the CMOS and the CCD devices perform comparably to those fabricated with separate process technologies. A summary of the process flow is given in Figure 1.

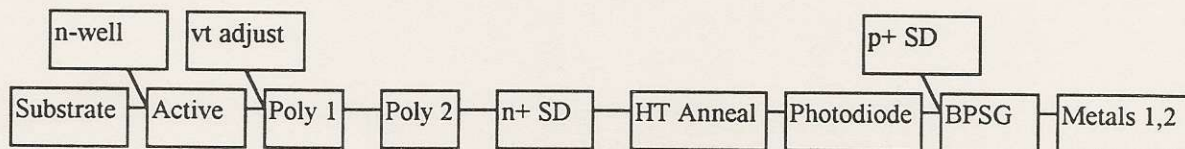


Fig. 1. Fabrication Process Flow showing the insertion of CMOS-specific modules in the CCD process. The bottom row of boxes represent the baseline CCD process flow. The CMOS modules are depicted by the top row of boxes with lines joining them to the baseline flow where they are inserted. In addition, an additional masking step (p-field) is used without extra ion implantation with the Active process block.

Imager Design

The basic architecture of the APS is similar to earlier designs implemented at Jet Propulsion Laboratory and uses the $2\text{ }\mu\text{m}$ CMOS design rule. The array size is 256×256 , resulting in a 1.2 cm square die. A 40-pin pad frame is used for all input and output signals and power connections. Row and column addressing is accomplished using 8-input NAND gates implemented using overlapping polysilicon 1 and 2 gates of NMOSFETs connected in series. For each column, circuitry designed to reduce fixed pattern noise is incorporated in the output drive chain. On-chip sample and hold capacitors are implemented by stacking a MOS capacitor underneath a poly1/poly2 capacitor. Both the signal and the reset levels are delivered off-chip for a correlated double sampling circuit to reduce noise. The output signal chain implements a double delta sampling (DDS) technique that was developed at JPL to eliminate column to column fixed pattern noise [5].

The pixel design is depicted in cross-section in Fig. 2 and the layout is shown in Fig. 3. In addition to the transfer gate which is a buried channel device, three MOSFETs are used to handle reset, row select, and output drive. The pinned photodiode area is L-shaped to maximize photoactive area, resulting in a 30% fill-factor. Overlapping polysilicon control lines are also used to maximize the photoactive area. Anti-blooming control is achieved by setting the transfer and reset gates to 1.25 V , allowing lateral overflow into the reset drain.

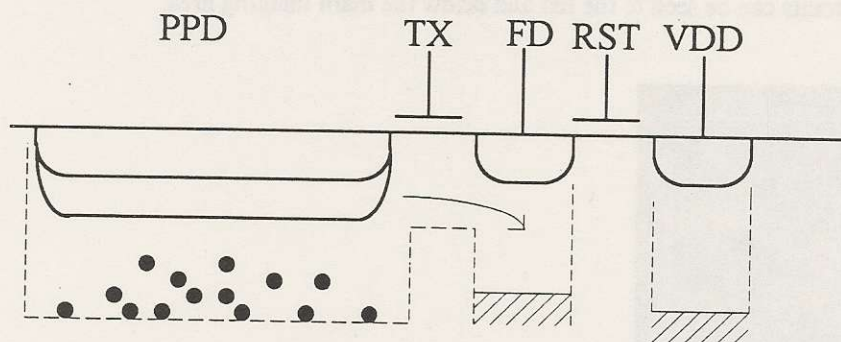
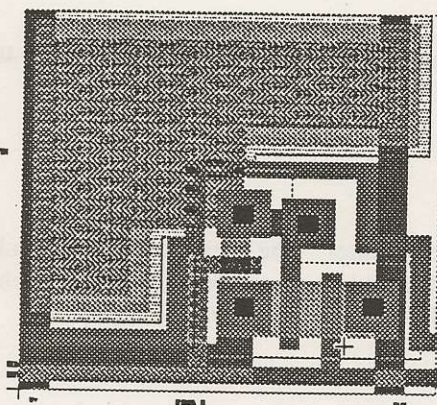


Fig. 2. Schematic cross-section of the pinned photo diode active pixel sensor. Charges integrated in the PPD is moved into the floating sensing diffusion FD for readout by the transfer gate TX. Then the signal is reset via the reset gate RST to power supply voltage VDD.



Pixel Design Parameters:

Dimension: $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$
 Fill-factor : 30%
 Photoactive Element: pinned photodiode
 Transfer Gate: buried channel, poly 1
 Row Select: poly 1, $W/L = 6/2$
 Reset Gate: poly 2, $W/L = 3/2$
 Output Drive: poly 1, $W/L = 6/2$

Fig. 3. Details of a pixel. The pixel size is $40\text{ }\mu\text{m}$ square and contains the pinned photodiode and three transistors.

Fabrication Results

The device characteristics measured on the wafers of the initial fabrication run are summarized in Table I. Since the present work requires 5 V operation, the zero bias potential values are changed from the nominal process. Both the buried channel and the diode potentials are lower to use 5 V gate voltages.

Table I
Comparison of Device Characteristics for 5 V Operation.

Device Characteristics	5 V Operation	Nominal Operation
Poly 1 n-channel depletion V_t	2.60	3.03
Poly 2 n-channel enhancement V_t	0.89	0.89
Poly 2 n-channel depletion V_t	2.60	3.05
Poly 2 p-channel enhancement V_t	-0.53	-0.56
Photodiode potential	3.38	5.28

A photograph of the finished chip is shown in Fig. 4. The CMOS row and column addressing and the column readout circuits can be seen to the left and below the main imaging area.

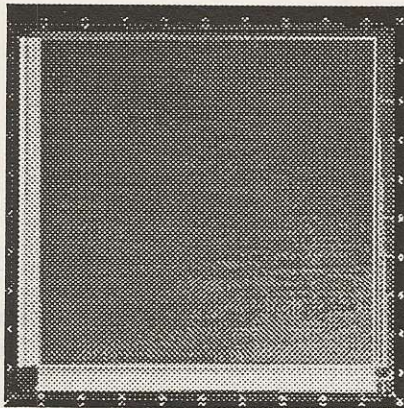


Fig. 4. Die photograph of the 256 x 256 pinned photodiode APS. The imager measures 1.2 cm a side with a 40-pin pad frame. It can be packaged in a ceramic pin grid array.

Conclusion

A pinned photodiode has been integrated into a CMOS active pixel sensor. The initial fabrication results indicate that 5 V operation is feasible, and this work demonstrates the promises of overcoming the poor blue response and dark current problems presently faced by APS built with CMOS-only technology.

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