Active Pixel Sensors

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A new type of image sensor is emerging from the most advanced image sensor R&D laboratories in Japan. This sensor, termed an active pixel sensor (APS), may one day supplant charge-coupled devices (CCDs) in many applications. The charge-coupled device relies on the shifting of charge to read out the image. The active pixel sensor acts like a random access memory (RAM) device wherein each pixel contains its own selection and readout transistors. The readout of the signal takes place then over metallic wires rather than by shifting the charge in the semiconductor. This gives the APS several advantages over the APS.

In this article the active pixel sensor concept is explored. The current state of the art of CCDs is examined. The active pixel sensor concept is then introduced. Activities in various laboratories are described. A discussion of the applications for APS technology is presented in the conclusion.

Charge-coupled devices were invented circa 1970 at the Bell Telephone Laboratories. In the intervening 23 years, the CCD has become the primary technology used in scientific image sensors. The details of CCD technology are complex, even for students of semiconductor device physics. It is not possible to provide a complete description of CCD operation in this paper, but the interested reader is referred to texts such as that by Yang[1] or Tompsett[2]. The virtues of the CCD include its high sensitivity, high fill-factor, and large formats. The high sensitivity arises from a high net quantum efficiency of the order of 40%, the high fidelity of reading out the CCD, and the low noise output amplifier. Typical output amplifier noise is of the order of 5 electrons r.m.s. due to the low capacitance of the output sensing node. The high fill-factor of a CCD pixel (80%-100%) is due to the fact that the MOS photodetector is also used for the readout of the signal. The large format of CCDs (typically 1024x1024, and as high as 4096x4096) has been enabled by the concurrent drive of the semiconductor memory business to improve silicon wafer quality and fabrication yield.

The Achilles' heel of CCDs is fundamental to the CCD operating principle -- the need for nearly perfect charge transfer. The CCD relies on the transfer of charge (usually electrons) from under one MOS electrode to the next through sequencing of voltages on the electrodes. The electrons are transported through the bulk silicon material macroscopic distances (e.g., centimeters) before they reach the output sense node. A typical CCD has three electrodes per pixel, so that in a 1024x1024 imager, the electrons may be shifted, on the average, several thousand times. The ratio of electrons successfully transferred to number left behind per electrode is the charge transfer efficiency (CTE). The CTE needs to be as close as possible to perfect to enable

[1]E.S. Yang, Microelectronic Devices, McGraw-Hill, NY (1988).
[2]C. Sequin and M. Tompsett, Charge Transfer Devices, Academic Press, NY (1975).

scientifically acceptable performance of the CCD. A single defect in silicon can trap electrons and degrade charge transfer efficiency. If the CTE is given by η, the net fraction of signal transferred after m transfers is simply η^m. Thus if a CCD is operating with a CTE of 0.9999 (1 electron lost out of 10,000), then a typical pixel signal in a 1024x1024 image sensor undergoes a fidelity degradation of nearly 20% by the time it reaches the output amplifier. Since this is unacceptable in most applications, large format CCDs have been developed to have CTEs that range from 0.99999 to 0.999999. For a CCD charge packet size of 1000 electrons, a CTE of 0.99999 implies that only one electron is lost for every 100 transfers! It is truly amazing that CCDs have been developed with such a high level of transfer efficiency and that the number of defects in a silicon wafer has dropped to essentially zero.

The need for nearly perfect charge transfer leads to a number of weaknesses in CCD technology. For example, CCDs performance is very susceptible to bulk radiation damage. In space applications, image sensors are continuously bombarded by energetic particles and photons. This radiation exposure can result in significant bulk displacement damage. The damaged silicon traps electrons and reduces charge transfer efficiency. Typical dose tolerance for a scientific CCD is of the order of 10 krads, depending somewhat on the radiation source. For long duration planetary instruments and certain earth orbits, the radiation softness of CCDs is significant issue. For many terrestrial applications (e.g., x-ray and electron imaging) the radiation softness of CCDs is also of concern.

To get high transfer efficiency, CCDs are often driven with relatively large voltages (by microelectronics standards). CCDs are also represent high capacitance loads to driving electronics so that the power requirements to drive the CCD make on-chip integration of clocks and drivers nearly impractical. Yet, the key to achieving future camera miniaturization is to integrate as much as possible on the same chip as the sensor. A further impediment to such miniaturization is that the CCD fabrication process is quite different from that of CMOS -- a preferred technology for implementation of on-chip signal processing. While some integrated CMOS/CCD processes have been demonstrated, undesirable compromises in the performance of one technology or the other must typically be made.

There are many other weaknesses in CCDs that ultimately stem from the need for nearly perfect charge transfer efficiency. These include limited spectral sensitivity range (i.e. that of silicon), difficulty to achieve large array sizes (CTE requirement gets larger with larger array size), difficulty to implement CCDs with large pixel sizes at high data rates, and limited readout rates.

There are a number of non-CCD image sensor technologies already in the market place. These include the photodiode array, the charge injection device (CID) and hybrid infrared image sensors. The first two have large input-referred noise floors (typically several hundred electrons r.m.s. for a single read) and need not be considered further here. Hybrid infrared sensors, could, in principle, by adapted for visible use. However, the hybrid approach in which a detector is bump-bonded, pixel-by-pixel, to a readout

multiplexer IC, is an expensive technology and is limited in size to approximately 512x512 formats. Typical noise floors in these focal-plane arrays are in the 30 electrons r.m.s. range.

In the active pixel sensor, several active transistors are integrated within the pixel for readout purposes. These transistors are used for pixel readout selection and for amplifying or buffering the pixel output signal. Twenty years ago, an active pixel sensor with a practical pixel size was not possible due to the state-of-the-art of microlithography in the early 1970's. The technological push of the semiconductor industry has driven microlithography to the sub-micron regime, and 1.25 micron CMOS is practically an industry standard. It is in the shadow of this progress that the fundamental advantage CCDs had over any other imaging technology has been eclipsed. CCDs in the 1970's were attractive because only three electrodes were required per pixel to make them operate. A 30 micron pixel was thus possible. However, pixel size is determined more by scientific imaging optics in the 1990's than by microlithography constraints. Thus, there is a new window of opportunity to take advantage of the advances in microlithography as it continues its inevitable evolution driven by the digital microelectronics industry.

A simple example of an active pixel is illustrated below. In this example, a lateral APS structure that resembles a short CCD is shown. Charge is integrated under the photogate PG. To read out the signal, the pixel is selected using transistor S. The output node is reset using transistor R. The signal charge is then transferred from under PG into the output node. The change in the source follower voltage between the reset level and final level is the output signal from the pixel. The source follower might drive a column line terminated with clamp and/or sample-hold circuits. These column-parallel circuits could then be scanned for serial readout of the sensor. Since the illustrated APS requires only a single intra-pixel charge transfer, many of the problems associated with charge transfer in CCDs are eliminated. If implemented in 0.8 micron CMOS, a 16 x 16 micron pixel could have an intrinsic fill-factor of over 50%. To improve fill factor to the levels typically associated with CCDs, one needs to utilize the emerging microlens technology. JPL is pursuing this type of approach in conjunction with on-chip analog-to-digital conversion to explore cameras-on-a-chip for future microspacecraft applications.

Much more sophisticated active pixel structures are being pursued elsewhere in order to achieve small pixel size and high fill factors. For example, Toshiba is using its double-gate floating surface transistor to increase the sensitivity of the output amplifier to 200 μV/electron[3]. To reduce the pixel size, the charge storage area can be located vertically under the (or over) the readout transistor. The presence or absence of photo-generated charge can be used to modulate the readout transistor output signal. This approach is used by Olympus in its charge modulation device (CMD) approach to active

[3]Y. Matsunaga, H. Yamashita, S. Manabe, and N. Harada, *A high-sensitivity MOS photo-transistor for area image sensors,* IEEE Trans. Electron Devices, vol. 38(5) pp. 1044-1047 (1991).

pixel sensors[4]. Texas Instruments (Japan) is using a bulk charge modulated device (BCMD) in a hexagonal packing format[5]. A further reduction in pixel size can be enabled if the current flow in the output transistor is vertical rather than horizontal so that the substrate acts as one of the transistor terminals. This approach is used by Olympus in its static induction transistor (SIT) APS device[6]. A vertical bipolar approach is used by Canon in its base-stored image sensor (BASIS)[7].

Each of these technologies has its own set of advantages and disadvantages. Fixed pattern noise is generally a common concern but can be eliminated through on-chip signal processing. The fixed pattern noise arises due to threshold voltage non-uniformities across a large area image sensor. Since output amplifiers track the threshold voltage of the output transistor, the APS is sensitive to this offset pattern. Clamp circuits can be used to nearly eliminate this phenomenon.

Applications for active pixel image sensors are numerous. High definition television (HDTV) is driving some of the work in APS since some signal gain prior to readout is desirable in this high bandwidth application. Electronic still cameras are another area of interest. The APS is more amenable to camera miniaturization and power minimization than the CCD. Imaging systems operating in high radiation environments represent another application area of APS technology. These include laboratory and spaceborne scientific cameras, medical instrumentation, nuclear instrumentation and space-based surveillance systems. Since the APS technology simplifies region-of-interest readout, machine vision and guidance and navigation sensors are another application area of APS technology. Imaging devices operating in extended spectral ranges may also benefit from the active pixel concept. Since CCDs are notoriously hard to implement in non-silicon materials, NIR/SWIR APS devices may be easier to achieve. UV sensors in materials such as SiC might also benefit from a APS approach.

It is difficult to displace a technology that has had nearly 25 years to mature such as the CCD and any incumbent technology has its own ardent supporters. Operating in the charge domain provides many interesting possibilities for low noise, low power signal processing, and operations such as time delay and integration (TDI) and pixel binning will be harder to achieve with APS. The APS concept has caused much discussion among domestic image sensor manufacturers and several have indicated an interest in exploring this emerging technology. Given the relative immaturity of active pixel sensors and the high level of performance they have already achieved, it is highly likely that active pixel sensors will have a profound impact on future imaging systems.

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[4]M. Ogata, T. Nakamura, K. Matsumoto, R. Ohta, and R. Hyuga, *A small pixel CMD image sensor,* IEEE Trans. Electron Devices, vol. 38(5) pp. 1005-1010 (1991).

[5]J. Hynececk, *BCMD--An improved photosite structure for high density image sensors,* IEEE Trans. Electron Devices, vol. 38(5) pp. 1011-1020 (1991).

[6]T. Mizoguchi, I. Takayanagi, E. Shimuze, H. Nakajima, S. Hashimoto, S. Yokoyama, J. Nakamura, and M. Imai, *A 250 k-pixel SIT image sensor operating in its high-sensitivity mode,* IEEE Trans. Electron Devices, vol. 38(5) pp. 1021-1027 (1991).

[7]Y. Nakamura, H. Ohzu, M. Miyawaki, A. Ishizaki, T. Kochi, and T. Ohmi, *Design of bipolar imaging devices (BASIS): analysis of random noise,* IEEE Trans. Electron Devices, vol. 39(6) 1341-1349 (1992).

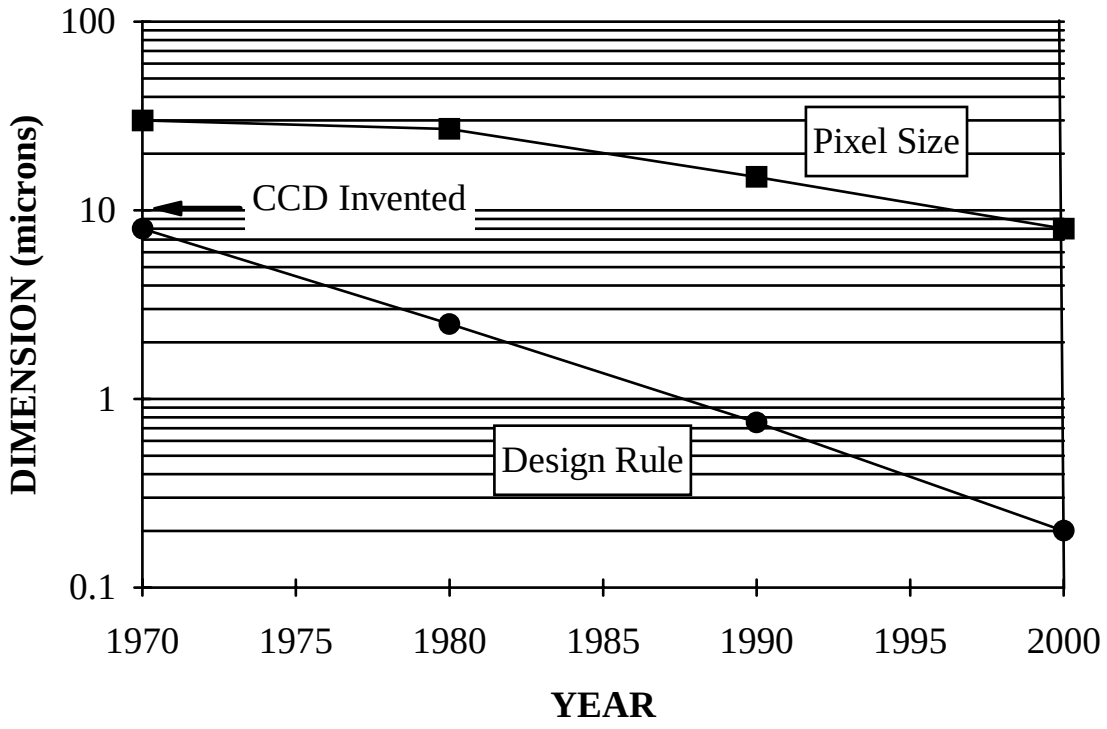

Fig. 1. Evolution of photolithographic feature size vs. pixel size.

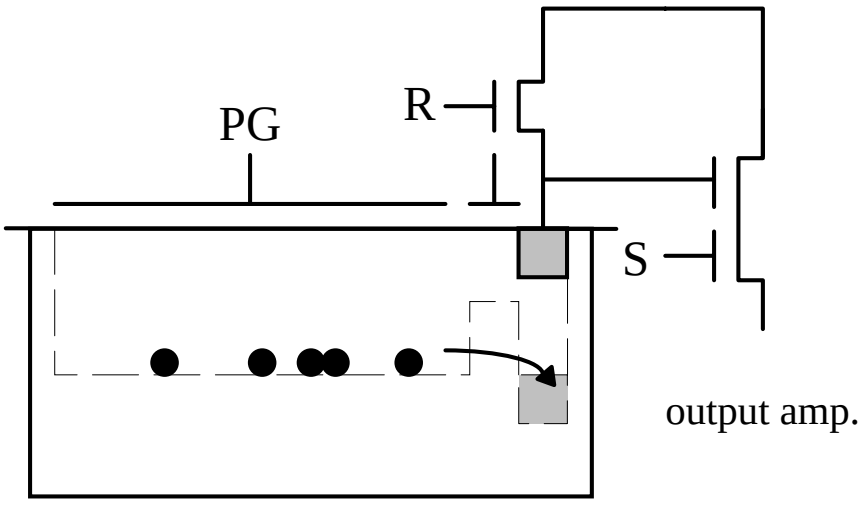

Fig.2. Schematic of a simple, CMOS-compatible active pixel.

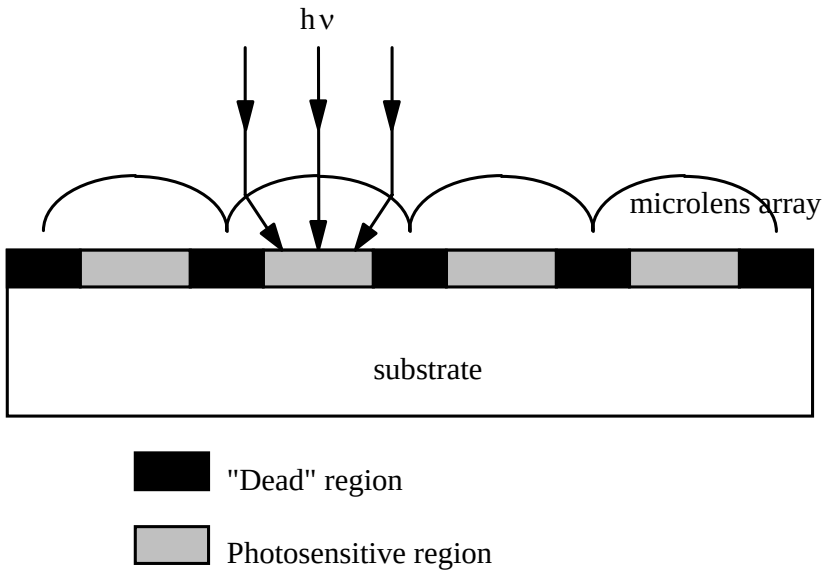

Fig. 3. Schematic illustration of on-chip microlens array to increase effective fill-factor.

Table Comparing Attributes Of Various APS Technologies

	DGFSPT	**CMD**	**BCMD**	**BASIS**	**SIT**	**CMOS APS**
Developer	Toshiba	Olympus	Texas Instr.	Canon	Olympus	JPL/Caltech
APS Type	Lateral	Vertical	Vertical	Vertical	Lateral	Lateral
Output	Lateral	Lateral	Lateral	Vertical	Vertical	Lateral
Pixel Size (μm)	13 x 13	7.3 x 7.6	10 x 10*	13.5 x 13.5	17 x 13.5	50 x 50
Sensitivity	200 μV/e-	250 pA/e+	15.4 μV/e-	3.5 μV/e+	3.0 μV/e+	0.6 μV/e-
Input-Referred Noise	0.8 e- rms	20 e+ rms	15 e- rms	60 e+ rms	69 e+ rms	11 e- rms
Dynamic Range	75 dB	70 dB	72 dB	76 dB	86.5 dB	60 dB
Fixed Pattern Noise (p-p)	10 %	5 %	2 %	0.03 %	1.1 %	< 1 %
Anti-blooming	vertical	vertical	vertical	none*	none*	lateral
Lag	0	0	0	<0.1 %	70 %	0
Comments	FPN may be reducible by read/reset/re-sample	Noise dominated by dark current. Improved by cooling.	*Hexagonal layout	*Can be reduced using clipping operation.	*SIT turns on	Projected performance. Uses 2 μm CMOS design rules.