Brief Papers

Analog Dynamic Random-Access Memory (ADRAM) Unit Cell Implemented Using a CCD with Feedback

B. Pain and Eric R. Fossum

Abstract—**A novel unit cell for analog, dynamic, random-access memory is described. The unit cell is implemented using a charge-coupled device (CCD) and features voltage-in/voltage-out operation with low power. The unit cell is essentially an algorithmic voltage sample-and-hold (S/H) circuit. It is sufficiently compact for imager frame memory application and may also find application in analog neural network circuits.**

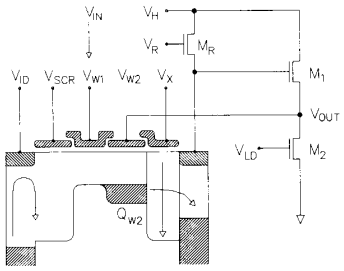

Fig. 1. Schematic illustration of ADRAM unit cell.

I. Introduction

A novel unit cell for analog, dynamic, random-access memory (ADRAM) devices is described. The cell operates in a voltage-in/voltage-out sample-and-hold (S/H) mode using a charge-coupled device (CCD). The CCD is operated as a voltage-controlled discrete time current source to pump charge to a storage node. The new memory cell structure uses feedback to control the amount of charge transferred to the storage node and thereby improve performance. Futher, it is of sufficiently low power and size to allow large-scale integration and the realization of 128 × 128 array single-chip imager frame memory. Such memory structures would find immediate applications in focal plane-image processing for machine vision [1] or analog neural networks. In contrast, a simple S/H circuit using a switched capacitor and source-follower is subject to offset, switch feedthrough, and nonuniformity due to threshold voltage variation. These problems could be compensated by use of an operational amplifier and feedback but at the unacceptable expense of speed, chip area, and power. A digital approach to an analog computing system would required both A/D and D/A converters, in addition to digital memory, resulting in an increase in system complexity and power.

II. Operation of the Unit Cell

The ADRAM unit cell operates in an algorithmic voltage S/H mode. During the write cycle, the cell operates in discrete time to generate an output voltage equal to the input voltage. Essentially, charge is added to the gate of a source-follower until the output voltage and the input voltage are balanced. In the read operation, the source-follower is enabled and the stored voltage is read out.

A schematic of the unit cell is shown in Fig. 1. The unit cell consists of charge-coupled device with a charge-domain fill-and-spill [2] input section (V_{ID}, V_{SCR}, V_{W1}, V_{W2}), a charge-domain output section (V_x), and a source-follower charge-to-voltage conversion section (M_R, M_1, M_2). Note that the output voltage V_{OUT} is fed back as V_{W2}.

The details of the write operation are as follows. The output floating diffusion and store bucket are reset to V_H by momentarily pulsing the reset transistor M_R high. The input voltage to be written into the cell (V_{IN}) is applied to V_{W1}. The input voltage is assumed to be constant during the entire write cycle. The screen gate V_{SCR} is dc biased to a voltage greater than V_{IN}. With the transfer gate V_x off, the input diode is momentarily pulsed low to perform a fill-and-spill operation. The charge captured under gate V_{W2} is simply

$$Q_{W2} = C_{W2} \cdot [V_{W2} - V_{W1}] \tag{1}$$

where C_{W2} is the bucket capacitance under V_{W2}. By momentarily pulsing the transfer gate V_x, the change is then transferred to the floating diffusion, causing the output voltage to change by an amount $\Delta V_{OUT} = g \cdot Q_{W2}/C_{OUT}$, where C_{OUT} is the total capacitance connected to the floating diffusion and source-follower input gate, and g is the gain of the source-follower circuit. Note that the charge transferred to the output is proportional to the difference between the output and the input voltage and that the change in output voltage is in a direction as to reduce this difference. Thus by repeating the fill-and-spill and transfer processes a few times, the output voltage can ideally be made to approach the input within any tolerance limit. In principle, no charge is transferred after the output voltage is equal to the input voltage.

From charge conservation considerations, it can be easily shown that the output voltage, after k fill-and-spill operations and charge transfers, is given by:

$$V_{OUT}(k) = V_{IN} + [1 - g \cdot C_{W2}/C_{OUT}]^k \cdot [V_H - V_{IN}]. \tag{2}$$

The capacitances C_{W2}, C_{OUT}, and the gain are chosen to provide rapid covergence of the output voltage to the input voltage. It is important to note that the convergence is independent of variations in source-follower gain, threshold voltage, and device geometry, and that the gain may be voltage-dependent, provided the quantity $R_c = g \cdot C_{W2}/C_{OUT}$ is less than unity. Variation in these parameters will, however, affect the convergence rate. Threshold voltage difference between V_{W1} and V_{W2} (expected to be minimal) is transferred as offset to the output.

In essence, the input structure operates as a voltage-controlled current source, except that the current is actually a discrete series of charge packets. With the added feedback, the unit cell acts as a damped integrator, thereby guaranteeing convergence of the output voltage to the input voltage.

III. Preliminary Results

An existing surface-channel CCD test circuit structure was used to confine the validity of the unit cell concept. The test structure consisted of a fill-and-spill input circuit and a two-stage source-

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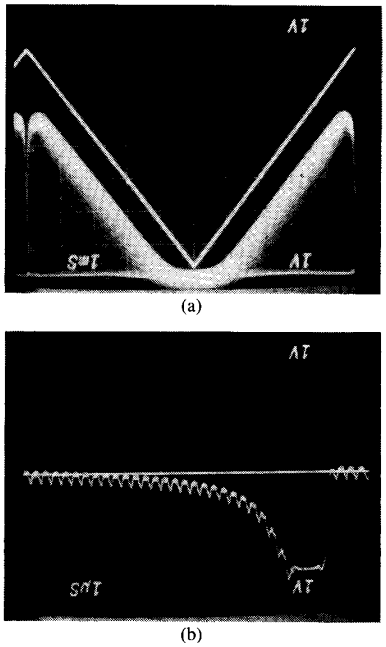

Fig. 2. (a) Oscilloscope photograph showing convergence of V_{OUT} (upper trace) to V_{IN} (flat trace). (b) Oscilloscope photograph showing same setup as Fig. 2(a) but with V_{IN} slowly modulated by a triangular wave. Note that the two traces were deliberately offset for clarity.

follower output amplifier. The feedback loop was completed externally and the covergence was monitored on an oscilloscope. Fig. 2(a) shows an oscilloscope trace demonstrating the convergence of the output to an applied input voltage. The input diode pulsewidth (fill period), spill period, and the transfer gate period were each 100 ns, making one complete cycle 300 ns long. As shown in the figure, the convergence time was less than 8 μs, consistent with the capacitances and gain of the circuit. The minimum clock period used in this test was limited by the probe station. A small transient feedthrough from the transfer gate is observed on the trace but does not affect the unit cell performance. In Fig. 2(b), the same setup was used, but the input voltage was slowly swept by a function generator. As indicated by the envelope of the output signal, excellent linearity was achieved over a wide voltage range.

For ADRAM structures, a tradeoff between cell size, access time, signal accuracy, and power must be achieved. Using state-of-the-art design rules, minimum clock periods of 20 ns can be readily obtained, leading to typical convergence times of 1.2 μs, (20 cycles) with an accuracy of better than 1 part in 256 (8 b). The output noise voltage $\langle V_n \rangle$ introduced by the fill-and-spill input is estimated as:

$$\langle V_n \rangle = (kT/2C_{W2})^{1/2} \cdot [g \cdot C_{W2}/C_{OUT}] \qquad (3)$$

and is generally insignificant. Holding time for the unit cell depends on leakage current so that refresh using a quantizer is required for long-term storage. However, most applications require storage for a duration of a few frames (e.g., 100 ms). This can be achieved without refresh at room temperature with less than 1% droop.

IV. Conclusion

A new unit cell for analog dynamic random-access memory has been introduced. The unit cell uses the differential input mode readily achieved with CCD's to eliminate the need for an operational amplifier. The resultant memory structure is independent of threshold voltage variations and output amplifier parameters and is of low power. Using commercially available CCD foundry design rules, we estimate the unit cell layout area to be 50 μm $\times$ 50 μm. The cell design is easily integrable for analog memory arrays for image processing or neural networks.

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An Improved Early Voltage Model for Advanced Bipolar Transistors

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***Abstract*—The Early voltage V_A of a bipolar transistor is conventionally treated as bias-independent, thus neglecting the details about the effect of the two junction voltages on the base-width modulation, which results in V_A. This effect becomes more prominent in advanced bipolar transistors because they possess very thin base regions. In this brief, a more accurate bias-dependent Early voltage model is developed. Early voltages calculated from the present model are found in good agreement with measured dependencies. SPICE simulation is also carried out in demonstrating the bias-dependent V_A effects on small-signal performance of bipolar transistor integrated circuits.**

I. Introduction

The base-width modulation in bipolar transistors (BJT's) was first investigated by Early [1] and then studied by many authors [2]-[6]. Conventionally, the base-width modulation has been treated independently at the collector-base (C-B) junction (Early effect) and at the emitter-base (E-B) junction (late effect), which results in a constant Early voltage V_A. For BJT's with relatively long base width, the independent treatment at the two junction yields a negligible error. For advanced BJT's fabricated from the double-poly process possessing base width below 0.1 μm, however, the coupling effect of the voltage variation at the two junctions on V_A becomes important. This constant V_A is used in the well-known Gummel-Poon bipolar transistor model employed in SPICE2 [7], thus making the advanced BJT circuit simulation less accurate.

In this brief, a more accurate bias-dependent Early voltage model is derived unifyingly from the base-width modulation due to the change of the emitter-base and collector-base applied voltages. Physical equations describing the base charge and junction capacitances, from which bias-dependent V_A is derived, are given in Section II. Early voltages calculated from the present model are then compared with experimental data, and simulation results based on SPICE employing the present V_A model for a differential amplifier are shown in Section III. Conclusions appear in Section IV.

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