# A RESISTIVE-GATE TWO-PHASE 2DEG CCD FOR III-V IR DETECTORS

J.-I. Song
Department of Electrical Engineering
Columbia University, New York, NY 10027

E.R. Fossum
JPL/CalTech MS 300-315
4800 Oak Grove Drive, Pasadena, CA 91109

## ABSTRACT

A device structure for two-phase operation of a two-dimensional electron gas charge-coupled device (2DEG CCD) has been demonstrated for the first time and exhibits a charge transfer efficiency (CTE) exceeding 0.999 at 26 MHz. The $Al_{0.3}Ga_{0.7}As/GaAs$ modulation-doped heterostructure utilizes a resistive cermet gate with recesses to achieve two-phase operation. The structure is compatible with advanced III-V infrared detectors for monolithic integration in future orbiting imaging systems.

## INTRODUCTION

The two-dimensional electron gas charge-coupled device (2DEG CCD) is an outgrowth of recent advances in 2DEG FETs for high speed digital logic circuitry and microwave devices. Features of 2DEG CCDs include high transfer speed, large charge handling capacity in excess of $1.0x10^{12}$ carriers/cm$^2$, fabrication compatibility with high-performance, low noise 2DEGFET circuitry, and finally possible monolithic integration with advanced III-V infrared detectors [1]. The latter is enhanced by the maturing of MBE and MOCVD technology.

The first 2DEG CCD fabricated on AlGaAs/GaAs employed a capacitive-gate structure, demonstrating a poor charge transfer efficiency (CTE) due to gap-related potential problems [2,3]. Resistive-gate 2DEG CCDs were fabricated by Song, et. al. [4-6] on uniform-doped and planar-doped AlGaAs/GaAs heterostructures. Utilizing a four-phase clocking scheme, a room temperature CTE of 0.9990 (10 MHz - 1 GHz) and 0.9997 (130 kHz - 1 GHz), respectively, was demonstrated. The low frequency operation of these devices was limited by gate leakage current, which was several orders of magnitude less in the planar-doped structure. The high frequency test limit was set by the test station, and no reduction in CTE was observed at the 'pre' frequency limit.

While the four-phase resistive-gate structure allows high CTE with large bandwidth, the two-phase structure has two primary advantages over the four-phase structure. First, during image signal integration, the four-phase device requires DC power dissipation in the resistive gate. In the two-phase device, no DC power is required during image integration, since the gate recess provides pixel isolation. This significantly reduces cooling requirements in a 65 K IR focal-plane array. Second, chip complexity and drive circuit requirements are significantly reduced by eliminating two phases. This represents additional savings in power and weight of CCD drive electronics. A more through discussion of the 2DEG CCD will be published separately [7].

## STRUCTURE AND FABRICATION

A schematic cross section of the resistive-gate two-phase 2DEG CCD is shown in Fig. 1. The major difference between the two-phase and four-phase device structure is that a recessed gate is defined and deposited prior to cermet deposition. The recess, used previously in MESFET-type GaAs CCDs [8,9], results in a potential barrier in the channel. In the two-phase device, the finger electrodes are spaced and connected as shown in Fig. 2, yielding the illustrated potential diagram.

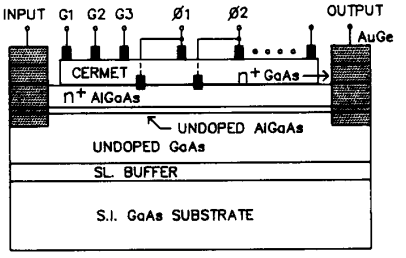



Fig. 1. Schematic illustration of the device structure of a resistive-gate two-phase AlGaAs/GaAs 2DEG CCD.



CH2865-4/90/0000-0267 $1.00 © 1990 IEEE

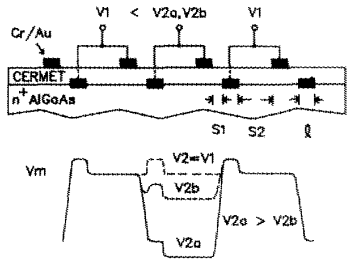



Fig. 2. Channel potential distribution of a resistive-gate two-phase 2DEG CCD with different clock bias levels (ℓ = 2μm, S1 = 1.5μm, S2 = 6.5 μm).

The material was grown at Columbia University with a Varian Gen-II molecular beam epitaxy (MBE) system on a <100> semi-insulating GaAs substrate. The structure, from bottom to top, consists of a AlGaAs/GaAs superlattice buffer, a 8000 Å thick undoped GaAs layer, a 30 Å thick undoped AlGaAs layer, a 350 Å thick AlGaAs layer doped with $3.6x10^{18}/cm^3$ Si atoms, and a 300 Å thick GaAs cap layer doped with $4.0x10^{18}/cm^3$ Si atoms.

After a 700 Å deep mesa etch, AuGe ohmic contacts were formed and annealed at 425 °C for 45 sec under a forming gas ambient. Using the AuGe ohmic contact pattern as a mask, the 300 Å GaAs cap layer and 100 Å of the $n^+$-AlGaAs layer were etched. A photolithography for first metallization was done and followed by a 100 Å deep recess of the $n^+$-AlGaAs layer to achieve a pixel isolation. The first Cr(35 Å)/Au(300 Å) metallization was done by e-beam and filament evaporations, respectively, self-aligned to the recessed gates to form underlying finger electrodes. A resistive layer (cermet) was e-beam evaporated on the CCD channel with an equal weight mixture of Cr and SiO powder sources [10], forming a Schottky contact to the underlying $n^+$-AlGaAs layer. The resistive layer was 4000 Å thick with a sheet resistance of 450 kΩ/□. A 3500 Å thick SiO layer was e-beam evaporated to serve as an inter-metal dielectric and lifted-off to form via holes. The second Cr(35 Å)/Au(3000 Å) metallization was used to form overlying finger electrodes and gate electrodes for the output amplifier. All deposited layers were defined by a standard lift-off process.

The CCD delay line is composed of 38 stages with a dual-electrode two-phase clocking scheme (152 electrodes). The finger electrodes are 2 μm long 24 μm wide spaced by $S_1$ = 1.5 μm and $S_2$ = 6.5 μm, resulting in a 24 μm by 24 μm pixel. Fig. 3 shows a photograph of the 2DEG CCD delay line and output amplifier after fabrication.

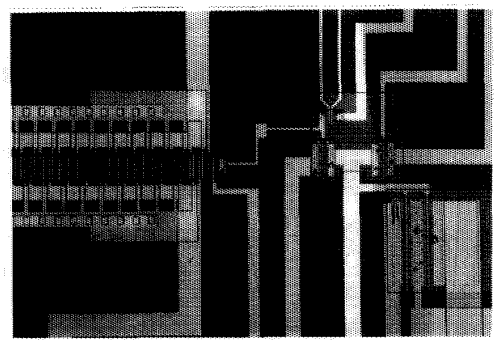


Fig. 3. Photograph of a resistive-gate two-phase 2DEG CCD after fabrication

## EXPERIMENTAL RESULTS

Basic device characterization was performed before the operation of the CCD delay line. The potential barrier was measured to be 1 volt, determined from the pinch-off voltages of a recessed gate 2DEGFET and an unrecessed counterpart, resulting in a charge handling capacity of $1.5x10^{12}$ electrons/$cm^2$ in the channel and thus 3.0 million electrons in a pixel. The transconductance of a 1.5 μm gate 2DEGFET was measured to be 100 mS/mm.

The operation of the CCD delay line was performed at clock frequencies up to 26 MHz which was the maximum available with the low frequency test station. The highest CTE obtained was 0.9993 at 26 MHz. Input and output waveforms of the CCD delay line with a 7.5 volt clock swing at this frequency is shown in Fig. 4.

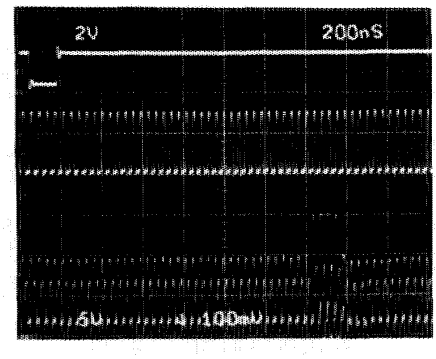



Fig. 4. Waveforms of the 38-stage CCD delay line operated at 26 MHz clock frequency with 7.5 volt clock swing. Upper waveform is the electrical input, middle is the clock signal, and lower is the delayed output signal.

As expected, degradation of the CTE was observed at clock frequencies lower than 20 MHz due to the dark current [6] and clock swings lower than 6 volts. The CTE dependence on clock frequency and clock voltage swing is shown in Fig. 5 and Fig. 6, respectively. Cooling the device at low frequency (16 MHz) improves the CTE, as shown in Fig. 7, confirming that the low frequency operation of this device is limited by gate leakage current. Experiment shows that a minimum 6 volt clock swing is required to stretch the 1 volt potential barrier induced by the recess.

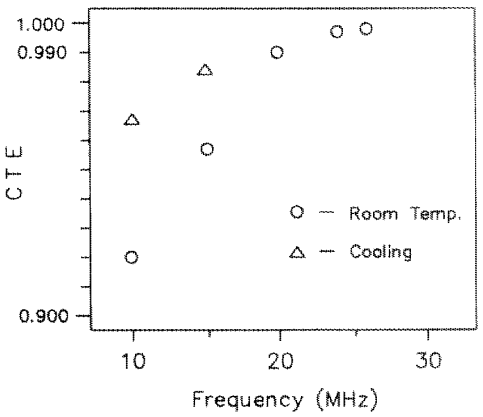



Fig. 5. Charge transfer efficiency vs. clock frequency at room temperature and lower temperature.

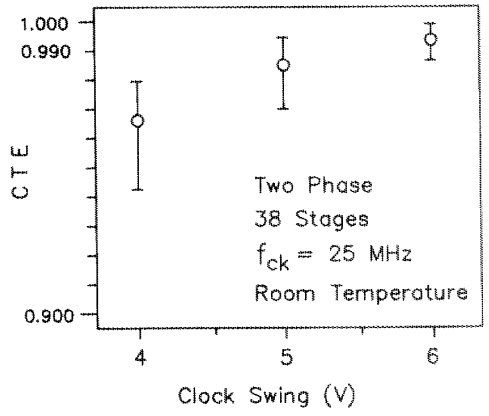
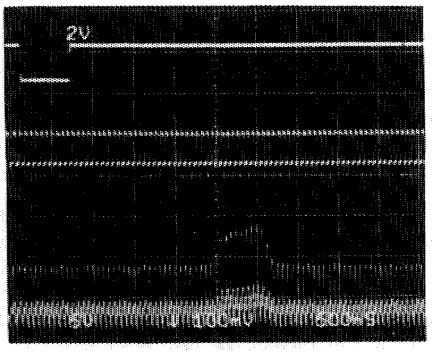
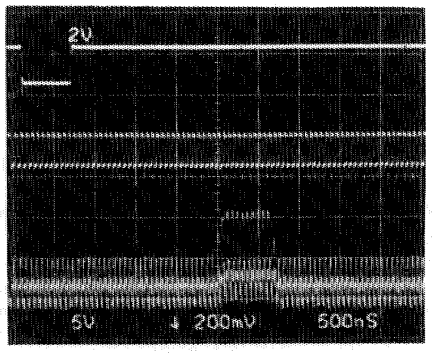



Fig. 6. Charge transfer efficiency vs. clock voltage swing at the clock frequency of 25 MHz.




a)




b)

Fig. 7. Operation of the CCD delay line at 16 MHz clock frequency. a) Before cooling. b) After cooling.

## DISCUSSION

A resistive-gate two-phase 2DEG CCD has been fabricated, demonstrating a high CTE (0.9993) and a large charge handling capacity (3.0 million electrons/pixel). The major obstacle facing the device is gate leakage current, which appears as dark current. While cooling the CCD to 65 K in an IR focal-plane will diminish the dark current, further reduction is anticipated by utilizing a planar-doped structure, as demonstrated previously [4,5], or a p-i-n gate structure. According to our gate leakage current model, the latter will have dark current reduced by more than 5 orders of magnitude at room temperature and more at lower temperatures, implying an extension of the low frequency operating limit by similar factors. The effect of potential barrier height and electrode spacings on the minimum clock swing and charge handling capacity is currently being examined.

Subsequent monolithic integration of this device with advanced III-V IR detectors such as multiple quantum well (MQW), heterojunction internal photoemission (HIP), and resonant tunneling structure detectors is anticipated.

## ACKNOWLEDGMENT

Authors would like to thank Dr. W.I. Wang and Mr. S. Xin of Columbia for material growth, Dr. J. Maserjian of JPL, Dr. J. Woodall of IBM, Dr. J. Cooper, Jr. of Purdue University, Dr. R. Colbeth of Varian, and Mr. D. Rossi of Columbia for valuable discussions, Dr. A. Warren of IBM for use of HETMOD device modelling program. This work was supported, in part, by the CalTech/JPL President's Fund and the ONR URI Program.

## REFERENCES

[1] See, for example, Proceedings of the Workshop on Innovative Long Wavelength Infrared Detectors, Pasadena, CA, 1990.
[2] R.A. Milano, M.J. Cohen, D.L. Miller, IEEE Electron Device Lett., EDL-3, 194 (1982).
[3] R.A. Milano, J.A. Higgins, D.L. Miller, and E.A. Sovero, in GaAs and Related Compounds 1982 (Inst. Phys. Conf. Ser. No. 65) 445 (1983).
[4] J.-I. Song, D.V. Rossi, and E.R. Fossum, Proc. SPIE, vol. 1308, p.39 (1990).
[5] J.-I. Song, D.V. Rossi, S. Xin, W.I. Wang, and E.R. Fossum, Presented at the 1990 Device Research Conference, June 1990, Santa Barbara, CA.
[6] J.-I. Song, D.V. Rossi, S. Xin, W.I. Wang, and E.R. Fossum, Submitted to Appl. Phys. Lett.
[7] E.R. Fossum, J.-I. Song, and D.V. Rossi, Submitted to IEEE Trans. Electron Devices.
[8] W. Keller, U. Ablassmeier, and H. Kniepkamp, IEEE Trans. Electron Devices, vol. ED-27, 1195 (1980).
[9] M. LeNoble, J.V. Cresswell, and R.R. Johnson, IEEE Trans. Electron Devices, vol. ED-37, 1796 (1990).
[10] J.-I. Song and E.R. Fossum, IEEE Trans. Electron Devices, ED-36, 1572 (1989).