A Resistive-Gate InAlAs/InGaAs/InP 2DEG CCD

D.V. Rossi, A.-N. Cheng[1], H.H. Wieder[1], and E.R. Fossum[2]

Department of Electrical Engineering, Columbia University, New York, NY
[1]Department of Electrical and Computer Engineering, Univ. of California, San Diego, CA
[2]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA

Abstract

The first two-dimensional electron gas (2DEG) charge-coupled device (CCD) fabricated in the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ materials system is reported. The device is implemented as a 31-stage, four-phase, resistive-gate delay line, and features an on-chip 2DEG-FET source-follower. The per-transfer efficiency is measured to be 0.995.

Introduction

InGaAs is an important short-wavelength infrared (SWIR) detector material. When lattice-matched to InP, it is responsive in visible through the near-infrared and into the SWIR spectral regime with a cutoff wavelength of approximately 1.65 microns. We are interested in InGaAs for space-borne image sensors and spectrometer instruments operating in this broad spectral range. Lacking in InGaAs technology has been a monolithic sensor readout (multiplexer). This has limited InGaAs-based sensor array performance and hence applicability. An InGaAs CCD technology could potentially bring sensor array performance in NIR and SWIR spectral regimes on a par with silicon visible detector arrays. It is the purpose of this work to investigate InGaAs CCDs.

CCDs broadly fall into two types of categories; surface-channel CCDs and buried-channel CCDs. We have previously investigated a buried-channel InGaAs CCD [1] with moderate results (room temperature charge-transfer efficiency (CTE) of 0.98 at 13 MHz and at 1 GHz clock rates). We have also investigated surface-channel-type CCDs using two-dimensional electron gas (2DEG) CCD structures in the AlGaAs/GaAs system [2] with excellent results (CTE $\geq$ 0.9997). A thin strained-layer InGaAs channel has been used for very high speed (14 GHz) GaAs-based 2DEG CCDs [3]. A resistive gate CCD (RGCCD) improves CTE by eliminating inter-electrode gap effects [4]. In this work, we report fabrication and measurement of the first InAlAs/InGaAs 2DEG RGCCD.

Device Structure and Fabrication

A schematic cross-section of the planar-doped 2DEG InAlAs/InGaAs RGCCD delay line is shown in Fig. 1. A corresponding energy band diagram for no signal charge is shown in Fig. 2. The material structure was grown at UCSD by MBE on a <100> oriented semi-insulating InP substrate and consists of a 250 nm undoped $In_{0.52}Al_{0.48}As$ buffer layer, followed by a

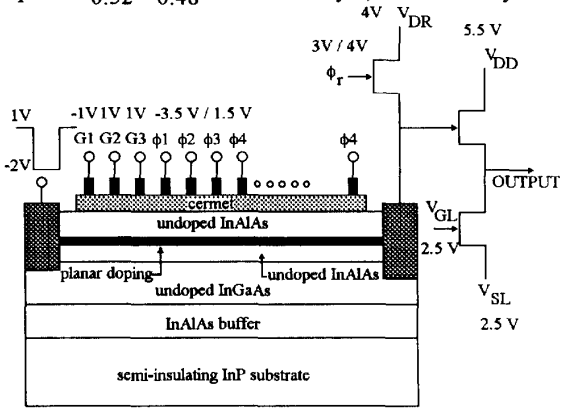

Fig. 1 Device cross-section including operating voltages.

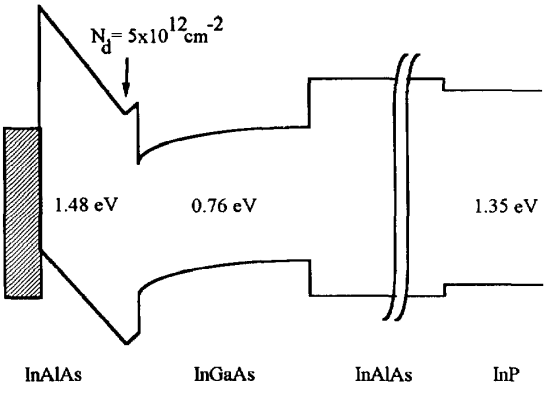

Fig. 2. Energy band diagram for InAlAs/InGaAs/InP 2DEG CCD.

0-7803-0817-4/92 $3.00 © 1992 IEEE

40 nm undoped $In_{0.53}Ga_{0.47}As$ channel/detector layer, a 4 nm undoped $In_{0.52}Al_{0.48}As$ spacer layer, a 4.8×10^{12} cm^{-2} Si planar doped layer, followed by a 30 nm undoped $In_{0.52}Al_{0.48}As$ barrier layer, and a 15 nm $In_{0.53}Ga_{0.47}As$ cap layer. The use of planar doping has been found to reduce leakage current in 2DEG CCDs by reducing the surface electric field at the gate [2]. In a visible/SWIR image sensor, the undoped InGaAs detector layer thickness would be increased to perhaps 1000 nm to improve detector quantum efficiency.

Device fabrication begins with mesa isolation by etching the MBE-grown layers down to the InP substrate using a 1:1:38 H_3PO_4:H_2O_2:H_2O etch. Ohmic contacts (AuGeNi) are then formed by lift-off and rapid thermal annealing at 400 °C for 15 sec under a forming gas ambient, and the subsequent removal of the InGaAs cap layer and recess of the InAlAs layer was performed using the AuGeNi contacts as a mask and H_2SO_4:H_2O_2:H_2O (1:1:90). During the recess etching the source-drain saturation current was monitored and the etching stopped at a current level determined to be optimal by previous device characterization on this material.

A 750 kΩ/□, 150 nm resistive layer (cermet) was electron-beam evaporated on the CCD channel using an equal weight mixture of Cr and SiO powder sources, forming a Schottky contact to the underlying InAlAs barrier layer. A high sheet resistance was used for the resistive gate since previous characterization indicated that the gate leakage could be reduced by evaporating higher resistivity films. This effect is probably related to the relative concentration of Cr to SiO at the interface. Improved compositional control during deposition and a combination of surface analytical techniques and electrical measurements are required to study this effect.

Electron-beam/thermally evaporated Cr/Au was patterned forming ohmic finger electrodes to the cermet and Schottky contacts to the FET's InAlAs barrier layer. Electron-beam evaporated SiO was used as an intermetal dielectric for the subsequently deposited Cr/Au interconnect metal.

The InAlAs/InGaAs 2DEG RGCCD is organized as a four-phase, 31 stage delay line with 1 μm by 100 μm finger electrodes spaced by 4 μm and features a source-follower output amplifier with on-chip load composed of a pair of 1 μm by 100 μm 2DEG FETs.

Experimental Results And Discussion

A. Device Parameters

Before operating the CCD delay line, basic device characterization was performed. As determined by a Hall effect measurement, the electron mobility was 6400 $cm^2/V{\cdot}s$ at 300 K and 12000 $cm^2/V{\cdot}s$ at 77 K with a 2.8×10^{12} cm^{-2} sheet carrier density. The transconductance of a 1 μm planar-doped 2DEG FET was 200 mS/mm. The CCD channel threshold voltage was -1.0 V as indicated by a capacitance-voltage measurement. The dark current density at this voltage ranged from 10 - 40 mA/cm^2 for typical devices and is likely dominated by mesa sidewall leakage [5].

B. Transfer Efficiency

The CCD was operated at both low and high frequencies. The test station limited the maximum low frequency testing to 26 MHz while high frequency testing was possible between 600 MHz and 1 GHz. For the low frequency testing, clock signals were generated by an HP 8016 word generator which triggered Pulse Instruments PI 458 programmable pulse drivers. The high frequency quadrature clock signals were generated by using microwave power dividers and 90° hybrid phase shifters to appropriately delay a voltage-controlled oscillator signal which triggered Colby Instruments CD5B clock drivers.

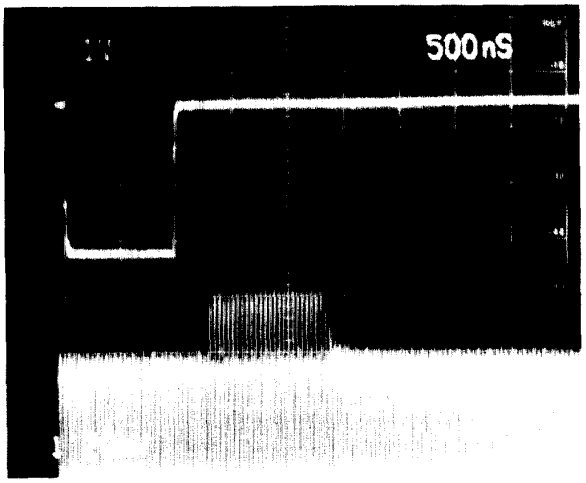

Fig. 3. Input and output waveform for the 31-stage (124 electrode) delay line operated at 23.6 MHz. Top trace shows input pulse and lower trace shows CCD output.

The input and appropriately delayed output pulse at 23.6 MHz is shown in Fig. 3. From the trailing edge one infers a per-transfer CTE of 0.995. The bias conditions for which this CTE was obtained are depicted in Fig. 1. Tuning the clock voltages proved to be crucial to achieving high CTE output characterized by sharp rise and fall times. It was observed that tuning the low clock level to about -3 V to -4V while maintaining a total clock swing of about 5 V was optimum. Running the clock levels between 0 V and about 5 V, for example, resulted in a CTE of about 0.95 and roughly twice the signal magnitude at the same frequency. It was also noticed that if the low clock level was not sufficiently low, the output exhibited smearing making it broader than the input pulse. This could not be attributed to clock feedthrough or overinjecting charge into the bucket since increasing the low voltage on the input pulse (eg. decreasing the charge injection level) did not negate the smearing. An explanation consistent with the above observations is that due to the floating potential of the backside substrate, running the positive clock voltages induces an enhancement mode operation. This results in a larger signal packet whose charge transfer efficiency is degraded by the increased leakage current and by carrier transport and trapping in the parasitic InAlAs potential well. In contrast, the negative clock signal operation maintains depletion mode operation relative to the substrate potential thus avoiding these deleterious effects. The dependence of the CTE on frequency for the low frequency operation is shown in Fig. 4. The CTE improved as the device was cooled, suggesting that the dark current sets the low-frequency limit. This is further supported by noting that the lower roll-off frequency corresponds to the point at which the integrated leakage current density approaches the bucket charge handling capacity. The mechanism by which the leakage current degrades CTE is not presently understood.

High speed operation was measured using only positive clock levels due to instrument limitations. Operation at 1 GHz indicated a poor CTE of 0.93. Decreasing the clock frequency down to 600 MHz did not improve performance. The measured electron mobility of the lattice-matched InGaAs should be sufficient to readily allow operation at 1 GHz. Based on this and the low-speed results, this poor performance may be attributed to enhancement mode operation caused by the clock levels.

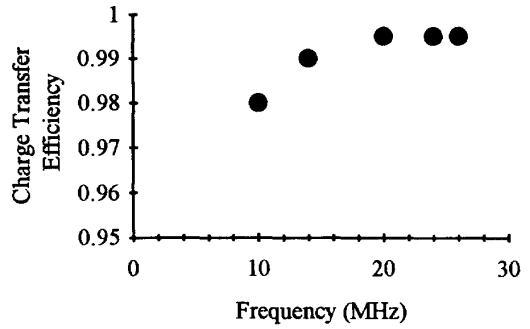

Fig. 4. Charge transfer efficiency as a function of delay line sampling frequency.

C. Optical Performance

The optical performance of the InGaAs 2DEG CCD was not evaluated due to the high leakage current which precluded significant integration periods. However, optical performance is expected to conform to the device structure and known absorption in the composite materials. For backside illumination, photons with energy above the InP bandgap will be filtered from the signal since they will be absorbed in the substrate. Thus, the detector will be responsive in the 0.9 to 1.6 micron range. For frontside illumination, cermet is transparent in the visible and NIR [4]. Absorption in the thin InAlAs layer will reduce visible response, though less than that occurring in polysilicon electrodes in silicon CCDs. The response in the SWIR will be limited by the thickness of the undoped InGaAs layer. While thin in this prototype device, increasing the thickness should not, in principle, affect device operation. For frontside illumination, the device should therefore have good responsivity from 0.4 to 1.6 microns.

Conclusion

Operation of the first InGaAs/InAlAs 2DEG RGCCD has been demonstrated. Low frequency testing demonstrated greater than 0.995 CTE at 23.5 MHz below which rapid CTE degradation was attributed to leakage current. High frequency operation resulted in very poor CTE which may be explained by the clock voltage levels. Future work will investigate adjusting the high-speed clock signal level as well as studying the effects of the backside bias level. Lower frequency operation may also be attained through the use of a double-planar-doped or p-i-n 2DEG device structure [2] to reduce leakage current. More sophisticated structures to avoid mesa sidewall leakage are also indicated. The

relatively high interface trap density (e.g., 10^{11} - 10^{13} cm^{-2} eV^{-1}) and corresponding time constants (e.g., 10^{-7} to 10^{-6} sec.) measured at the InAlAs/InGaAs interface [6,7] however, suggest that extending operation to lower frequencies will also require the use of alternate materials and structures to avoid trapping at the InAlAs/InGaAs interface.

Acknowledgments

The authors would like to acknowledge useful discussions with Dr. R.E. Colbeth, Dr. J.-I. Song, Dr. J.M. Woodall, and Dr. P.D. Kirchner. While not used in this device, the authors appreciate 2DEG material grown by Prof. W. Wang and Dr. S. Xin. This work was supported by the Office of Naval Research University Research Initiative Program, and by the National Aeronautics and Space Administration, Office of Aeronautics and Space Technology.

References

1. D.V. Rossi, J.-I. Song, E.R. Fossum, P.D. Kirchner, G.D. Pettit, and J.M. Woodall, "A Resistive-Gate $In_{0.53}$ $Ga_{0.47}As$/InP Heterostructure CCD," IEEE Electron Device Lett., vol. EDL-12(12) pp. 688-690 (1991).

2. E.R. Fossum, J.-I. Song, and D.V. Rossi, "Two-Dimensional Electron Gas Charge-Coupled Devices," IEEE Trans. Electron Devices, ED-38(5), pp. 1182-1191 (1991).

3. R.E. Colbeth, R.A. LaRue, G.A.Davis, C. Yuen, C. Webb, C. Shih, and R.E. Weiss, "Millimeter wave AlGaAs/InGaAs 2DEG-CCDS," 1991 IEDM Tech. Dig., pg 183-186.

4. J.I. Song and E.R. Fossum, "Characterization of Evaporated Cr-SiO Cermet Films for Resistive-Gate CCD Applications," IEEE Trans. Electron Devices, vol. 36 (9), 1575-1579 (1989).

5. S. Bahl, M. Leary and J. del Alamo, "Mesa sidewall leakage in InAlAs/InGaAs heterostructure field-effect transistors," IEEE Trans. Electron Devices, vol. 39(9) pp. 2037-2043 (1992).

6. W.-P. Hong, J.-E. Oh, P.K. Bhattacharya, and T.E. Tiwald, "Interface States in Modulation-Doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Heterostructures," IEEE Trans. Electron Devices, vol. 35(10), pp. 1585-1590 (1988).

7. P.-Z. Lee, C. Fan, L.G. Meiners, and H.H. Wieder, "Interfacial Properties of InAlAs/InGaS HIGFETs and MIS Capacitors," Semiconductor Science and Technology, pp. 716-720 (1990).