A Resistive-Gate $In_{0.53}Ga_{0.47}As/InP$ Heterostructure CCD

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Abstract—**The first InGaAs/InP charge-coupled device (CCD) is demonstrated, exhibiting a charge transfer efficiency (CTE) of 0.98 at 13 MHz and 1 GHz. Cooling the device improves the charge transfer efficiency to greater than 0.99 at 13-MHz clock frequency. The 0.76-eV $In_{0.53}Ga_{0.47}As$ bandgap makes this structure applicable to direct detection short-wavelength infrared (SWIR) imagers.**

I. Introduction

THE unstrained $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ system has been used in recent years to demonstrate high-performance two-dimensional electron gas field-effect transistors [1], [2] and heterojunction bipolar transistors [3], [4] based on the high mobility of InGaAs. Since high quantum efficiency can be obtained in $In_{0.53}Ga_{0.47}As$ photodetectors at 1.55 μm, this system has also been attractive for fiber-optic receiver applications. An InGaAs-based charge-coupled device (CCD) technology, however, has not been previously demonstrated, but would have two significant advantages over silicon. First, the high mobility and saturation velocity of InGaAs suggests the possibility of very high-speed charge transfer for analog signal processing implementations, with millimeter-wave operation having been simulated recently [5]. Second, since the smaller bandgap of $In_{0.53}Ga_{0.47}As$ (~ 0.76 eV) is comparable to germanium, a CCD would have application in short-wavelength infrared (SWIR) imaging and electro-optical systems.

In this paper, the first demonstration of an InAlAs/InGaAs/InP CCD is reported. The device is a heterostructure MESFET-type [6] resistive-gate CCD, whose study will serve as a basis for future investigation of both very high-speed CCD's and monolithic SWIR imaging arrays.

II. Device Structure and Fabrication

The material structure for the InGaAs-based CCD was grown by MBE on a ⟨100⟩ oriented semi-insulating InP substrate and consists of a 250-nm undoped $In_{0.52}Al_{0.48}As$ buffer layer, followed by a 150-nm 10^{17} n-type $In_{0.53}Ga_{0.47}As$ channel layer, a 60-nm undoped $In_{0.52}Al_{0.48}As$ barrier-height enhancement layer [6], and a 10-nm undoped $In_{0.53}Ga_{0.47}As$ cap layer.

Device fabrication begins with mesa isolation by etching the MBE-grown layers down to the InP substrate using a 1:1:20 $HF:H_2O_2:H_2O$ selective etch. Ohmic contacts (AuGe) are then formed by lift-off and rapid thermal annealing at 400°C for 15 s under a forming gas ambient, and the subsequent removal of the InGaAs cap layer and recess of the InAlAs barrier enhancement layer was performed using a phosphoric-based etchant. A 200-k$\Omega/\square$ 100-nm resistive layer (cermet) was electron-beam evaporated on the CCD channel using an equal weight mixture of Cr and SiO powder sources [7], forming a Schottky contact to the underlying InAlAs barrier layer. Electron-beam/thermally evaporated Cr/Au was patterned forming ohmic finger electrodes to the cermet and Schottky contacts to the FET's InAlAs barrier layer. Electron-beam evaporated SiO was used as an intermetal dielectric for the subsequently deposited Cr/Au interconnect metal. A schematic cross section of the completed CCD delay line is shown in Fig. 1.

The InGaAs CCD is organized as a four-phase, 33-stage delay line with 2-μm × 28-μm finger electrodes spaced by 5 μm and features a two-stage source-follower output amplifier to separately optimize detecting the charge packet and driving the oscilloscope. A resistive-gate structure [8] was chosen since it avoids possible interelectrode electrostatic potential inhomogeneities, which would inhibit efficient charge transfer in capacitive-gate CCD's (CGCCD's). Cermet also forms lower leakage Schottky barriers than conventional metallization [7], which is particularly important for the mesa sidewalls where the gate directly contacts the InGaAs channel layer. Thus, using a cermet resistive-gate structure efficiently mitigates the parasitic effects, allowing the performance of this first-generation InGaAs-based CCD to be assessed. Clearly, application-oriented analogous structures would be tailored. For example, in order to minimize power dissipation, low-speed imager readouts would likely be CGCCD's while high-speed analog signal processing implementations would employ a resistive-gate CCD (RGCCD).

III. Experimental Results

Before operating the CCD delay line, basic device characterization was performed. As determined by a Hall effect measurement, the electron mobility was 4200 $cm^2/V \cdot s$ at

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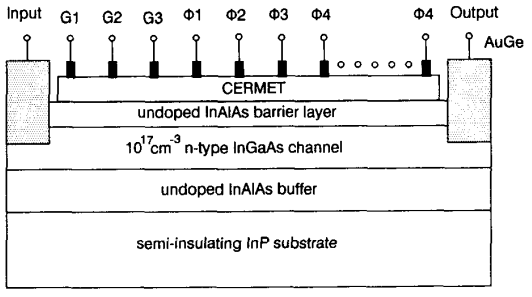
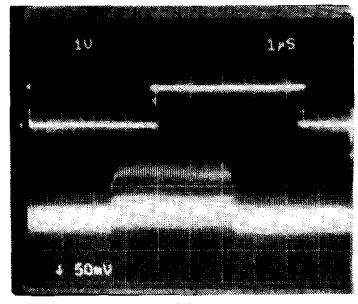


Fig. 1. Schematic cross section of the $In_{0.53}Ga_{0.47}As/InP$ resistive-gate CCD.

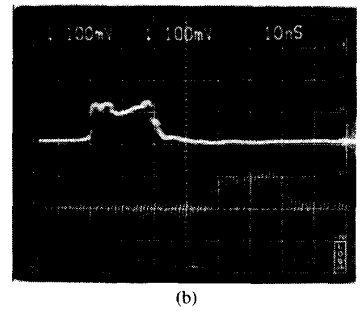
300 K and 5500 $cm^2/V \cdot s$ at 77 K. The transconductance of a 1.5-μm heterostructure MESFET was 100 mS/mm. The CCD channel threshold voltage was −3.5 V as indicated by a capacitance–voltage measurement and the dark-current density at this voltage was 40 mA/cm^2. Comparing the current–voltage characteristic of a cermet test diode which overlapped the mesa sidewall with one which was confined on the mesa, it was found that the CCD dark current density could be reduced by approximately two orders of magnitude by eliminating the sidewall leakage, which will be explored in future work.

The CCD was operated at both low and high frequencies. The test station limited the maximum low-frequency testing to 26 MHz while high-frequency testing was possible between 600 MHz and 1 GHz. By examining deferred charge [9], the room-temperature CTE's were determined to be 0.98 at both 13 MHz and 1 GHz. Cooling the device improved the CTE to 0.99 at 13 MHz and concomitantly increased the signal magnitude. Cooling was achieved using a liquid-nitrogen cold finger contacting the package's back side, and the temperature was estimated to be 200 K by measuring the current in a calibrated diode. Fig. 2 depicts the cooled low-frequency and room-temperature high-frequency CCD input/output signals while Fig. 3 depicts the CTE frequency dependence at room temperature.

Several possibilities exist for explaining the charge-transfer inefficiency, including dark current, bulk and interface traps, avalanche multiplication in the heavily doped, narrow bandgap InGaAs, and charge transfer beneath the 2-μm finger electrodes. Current–voltage measurements indicated breakdown at greater than 10-V reverse bias, ruling out avalanche multiplication in the channel. Bulk traps would give rise to a proportional loss characteristic; the observed asymmetric waveform, however, indicates a fixed or nonlinear mechanism [9]. The effect of interface traps, which can be a fixed loss mechanism, should have a frequency dependence and be eliminated by superimposing a signal charge packet that is small enough to avoid charge interaction with traps at the front-side InGaAs/InAlAs interface on a fat-zero charge to quench traps at the back-side InGaAs/InAlAs interface. Neither of these effects were observed, indicating that trapping effects are insignificant. The CTE improvement and increased signal magnitude at low temperature can be attributed to a reduction in dark current. For example, cooling the device resulted in a one order of magnitude dark-current reduction and an increase in CTE from 0.98 to greater than 0.99. It was also verified that the low-frequency operating limit was extended by a factor approximately equal to the leakage current reduction. In addition, calculating the integrated dark-current density properly predicts the low-frequency operating limit, suggesting that both the low-frequency limit and the corresponding CTE can be improved by reducing the dark current. Thus, reducing the dark current by two orders of magnitude by eliminating the sidewall leakage should yield direct CTE and low-frequency cutoff benefits. The specific nature of the interrelationship warrants further study and should consider the interaction between the dark current and the interface traps. The potential below the finger electrodes may explain the high-frequency charge-transfer inefficiency, since the relatively weak fringing field across this region limits the charge transport rate. Further



(a)



(b)

Fig. 2. Waveforms of the 33-stage (132 electrodes) delay line operated at (a) 13 MHz while cooled and (b) 1 GHz at room temperature. In both cases, upper and lower waveforms are the input signal and the delayed output signal, respectively.

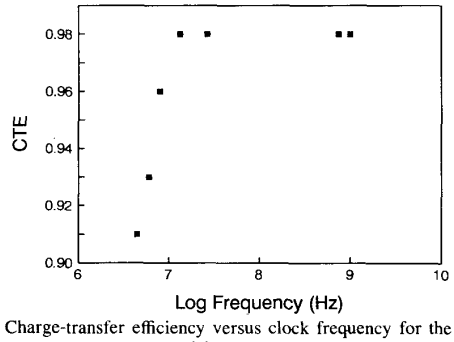


Fig. 3. Charge-transfer efficiency versus clock frequency for the 33-stage delay line.

characterization is necessary to determine the CTE limitations.

IV. Conclusion

The first InGaAs-based CCD has been demonstrated. Although only modest performance was achieved, immediate performance improvements and greater insight into the CTE limiting causes are expected by reducing the dark current. More importantly, this device sets precedent for InGaAs-based CCD structures separately optimized for speed and SWIR applications.

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