Briefs

A Resistive-Gate $Al_{0.3}Ga_{0.7}As/GaAs$ 2DEG CCD with High Charge-Transfer Efficiency at 1 GHz

J.-I. Song, D. V. Rossi, S. Xin, W. I. Wang, and E. R. Fossum

Abstract—**The fabrication and performance of an $Al_{0.3}Ga_{0.7}As/GaAs$ modulation-doped resistive-gate charge-coupled device is reported. The two-dimensional electron gas (2DEG) CCD, implemented as a 32-stage four-phase delay line, is tested at both low (1–13 MHz) and high (0.6–1.0 GHz) frequency. It exhibits a room-temperature charge-transfer efficiency (CTE) of better than 0.999 at clock frequencies from 10 MHz up to 1 GHz without a fat-zero signal, and is limited by dark current below 10 MHz. The charge-handling capability and minimum clock swing of the resistive-gate 2DEG CCD are calculated.**

I. Introduction

GaAs and related heterostructure CCD's are of interest because of their high speed analog signal processing capability and intrinsic radiation hardness. With the advent of new infrared detectors built from III-V materials, the potential integrability of the detector and III-V-based CCD has spurred interest in investigating GaAs CCD's for monolithic readout purposes. The use of an AlGaAs/GaAs modulation-doped structure for CCD's has several advantages over conventional GaAs buried-channel CCD's: a higher electron mobility at low electric field and temperature, a larger charge-handling capacity, reduced clock swing, and fabrication compatibility with high-speed, low-noise modulation-doped field-effect transistors (MODFET) for read-out amplifiers and supporting digital circuits.

A capacitive-gate charge-coupled device (CGCCD) using an AlGaAs/GaAs modulation-doped structure was reported by Milano *et al.* [1], [2], but it had a room-temperature charge-transfer efficiency of only 0.9 at 100 kHz. (The CTE was improved with both fat zero and cooling.) The CGCCD may suffer low CTE due to the potential trough caused by interelectrode gaps [3]. This deleterious effect is augmented by the material structure that is optimized for high-performance MODFET's: the proximity of the channel to the gate and the highly doped AlGaAs. Furthermore, the effect of the potential trough seems to be more detrimental to the CTE than in a GaAs buried-channel CCD since a calculation of charge-handling capability shows that a significant amount of charge can be trapped in a potential well as small as several hundred millivolts.

The resistive-gate CCD structure overcomes this problem by eliminating interelectrode gaps through the use of a continuous resistive layer and has been shown to yield high performance at gigahertz rates in conventional buried-channel GaAs CCD's [4]. The extension of the resistive-gate structure to the 2DEG CCD was suggested by Milano *et al.* [2] but not realized. In this work, the operation of the first resistive-gate 2DEG CCD is reported.

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The authors are with the Department of Electrical Engineering and the Microelectronics Sciences Laboratories, Columbia University, New York, NY 10027.

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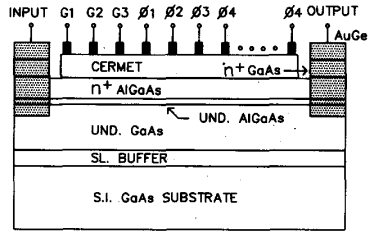

Fig. 1. Schematic illustration of the device structure of an AlGaAs/GaAs heterostructure resistive-gate CCD.

II. Device Structure and Fabrication

A schematic diagram of the resistive-gate 2DEG CCD is shown in Fig. 1. The material was grown at Columbia University with a Varian Gen-II molecular-beam epitaxy (MBE) system on a ⟨ 100 ⟩ semi-insulating GaAs substrate. The structure, from bottom to top, consists of a GaAs/AlGaAs superlattice buffer, a 5000-Å-thick undoped GaAs layer, a 30-Å-thick undoped AlGaAs spacer layer, a 350-Å-thick AlGaAs layer doped with $2 \times 10^{18}/cm^3$ Si atoms, and a 300-Å-thick GaAs cap layer doped with $4 \times 10^{18}/cm^3$ Si atoms. After a 4000-Å-deep mesa etch, AuGe ohmic contacts were formed and annealed at 425°C for 45 s under a forming gas ambient. Using the AuGe ohmic contact pattern as a mask, the 300-Å GaAs cap layer and 50 Å of the n^+-AlGaAs layer were etched. A resistive layer (cermet) was e-beam evaporated on the CCD channel with an equal weight mixture of Cr and SiO powder sources [6], forming a Schottky contact to the underlying n^+-AlGaAs layer. The resistive layer was 2500 Å thick with a sheet resistance of 350 kΩ/□. The first Cr(50 Å)/Au(2000 Å) metallization was done by e-beam and filament evaporations, respectively, to form finger electrodes on the resistive layer and gate electrodes for the output amplifier. A 3500-Å-thick SiO layer was e-beam evaporated to serve as an intermetal dielectric layer and lifted off to form via holes. The second Cr(50 Å)/Au(3000 Å) metallization was used to connect finger electrodes with the same phase. All deposited layers were defined by a standard lift-off process.

During the fabrication, the dc characteristics of FET were monitored. A degradation of transconductance and saturation current was observed whenever the AlGaAs layer between the gate and the source or the drain region was exposed to the developer for consecutive process steps. This was attributed to the etching of the AlGaAs layer in the developer (Shipley Microposit Concentrate mixed 1 : 1 with DI water). The inadvertent etching rate was measured to be about 10 Å/min.

The CCD delay line is composed of 32 stages with a four-phase clocking scheme (128 electrodes). The finger electrodes are 1 μm long, 100 μm wide, and spaced by 4 μm. An on-chip source follower composed of two MODFET's with 1-μm-long by 100-μm-wide gates with dual-gate reset is used to read out the signal from the CCD channel.

III. Charge-Handling Capability of the 2DEG CCD

Using a simple charge-control model [8] for the modulation-doped structure, the maximum charge-handling capacity for the trapezoidally shaped buckets can be derived. Neglecting the dif-

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fusion of carriers in the bucket, an approximate analytical expression for the maximum charge Q_{max} is given by:

$$Q_{max} = qn_{so}W[2l + (1 + V_{mcs}/V_{cs})L] \quad (1)$$

where n_{so} is the equilibrium 2DEG sheet carrier density, L is the interelectrode spacing, l is the finger electrode length, W is the channel width, V_{cs} is the clock swing, and V_{mcs} is the minimum clocks swing (with $V_{cs} \geq V_{mcs}$). The minimum clock swing V_{mcs} is given by

$$V_{mcs} = qn_{so}(d + \delta d)/\epsilon \quad (2)$$

where d is the total AlGaAs thickness, δd is the effective distance of the 2DEG from the heterointerface, and ϵ is the AlGaAs dielectric constant. It should be noted that the charge-handling capacity decreases with increasing clock voltage beyond the minimum clock swing, reflective of charge constriction by the electric field imposed by the resistive gate. This latter effect is characteristic of all resistive-gate structures. Note that the charge-handling capacity is derived assuming that the clock signal is a square-wave for low frequencies. A decreased charge-handling capacity is expected for high-frequency sinusoidal clock signals and is equal to $Q_{max} - qn_{so}WL$, since the critical time-dependent bucket shape is triangular rather than trapezoidal.

IV. Experimental Results

Before operating the CCD delay line, basic device characterization was performed. As determined by a Hall effect measurement, the electron mobility was 4300 $cm^2/V \cdot s$ at 300 K, 20 000 $cm^2/V \cdot s$ at 77 K, and the sheet carrier density n_{so} was 1.5×10^{12} electrons/cm^2. The pinchoff voltage of the normally-on CCD channel was -0.8 V determined by a capacitance–voltage measurement. The transconductance of a 1-μm-gate FET was measured to be 100 mS/mm. This relatively low transconductance is attributed to the source resistance since the amplifiers were not fabricated by a self-aligned process. The room-temperature leakage current density of the CCD channel was typically 2 mA/cm^2 at a reverse bias near the pinchoff voltage, and it is expected to be dominated by thermionic emission and/or tunneling from the gate electrode to the CCD channel.

The operation of the CCD delay line was performed at low and high frequencies. The low-frequency test was done at clock frequencies up to 13 MHz, which was the maximum available with the low-frequency test station. Fig. 2 shows the input and the delayed output signal at 13-MHz clock frequency at room temperature, corresponding to a CTE of better than 0.999, as evaluated using the method of Brodersen *et al.* [7]. The CTE at lower frequencies degraded rapidly; for example, at 1.5-MHz clock frequency the CTE was 0.98 and the output signal became smaller. Both results are attributed to the gate leakage into the CCD channel. A simple calculation shows that the dark current signal begins to exceed the maximum charge-handling capability of the bucket at this low frequency. The signal amplitude and the CTE improved as the device was cooled, suggesting that the dark current indeed sets the low-frequency limit.

The high-frequency test was done for clock frequencies between 600 MHz and 1 GHz (the range of the test station). The test result at 1-GHz clock signal at room temperature is shown in Fig. 3. Note that the output signal closely follows the ringing of the input signal. No degradation of the CTE up to 1-GHz operation was observed. The output signal amplitude increased compared with that of the low-frequency operation despite the decreased gain of the output amplifier due to 50-Ω loading by the sampling oscilloscope. Although not fully understood, it may be related to the dark current.

V. Conclusions

The first resistive-gate 2DEG CCD has been fabricated and operated at clock frequencies between 1 MHz and 1 GHz with high CTE at room temperature. The high-frequency test showed no CTE degradation up to 1-GHz operation. A higher speed test station will be necessary to measure the high-frequency limit of this device.

The CTE degraded at frequencies lower than approximately 5 MHz due to dark current. Optimization of the Al mole fraction of the AlGaAs layer to achieve a higher barrier at the Schottky contact or the use of a planar-doped heterostructure may help to reduce the leakage current, making lower frequency operation at room temperature feasible.

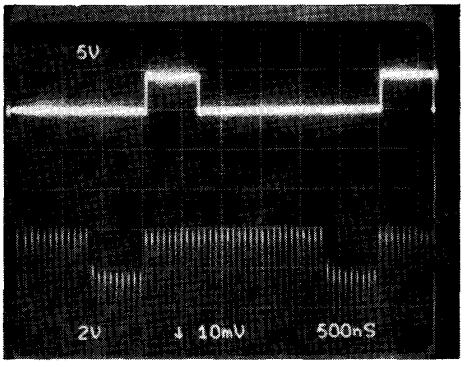

Fig. 2. Output of the 32-stage (128 electrodes) delay line operated at 13-MHz clock frequency. Upper and lower waveforms are the input signal and the delayed output signal, respectively.

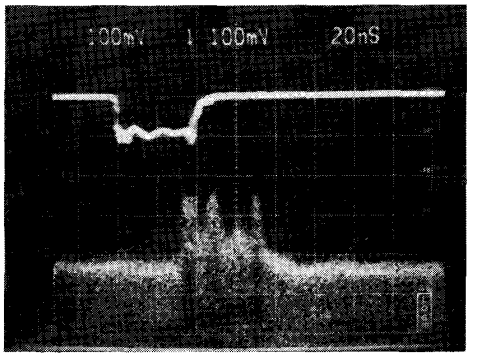

Fig. 3. Waveforms of the 32-stage (128 electrodes) delay line operated at 1-GHz clock frequency. Upper waveform is the input, and lower one is the output signal.

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High-Speed Noise-Immune AlGaAs/GaAs HBT Logic for Static Memory Application

W. Andre Hagley, Derek Day, Duljit S. Malhi, and J. M. Xu

***Abstract*—In this work we evaluate the performance of a new gate topology that gives large logic swings and high noise margin, at low power dissipation. The measured noise margin (43% of 3 V logic swing) and transfer characteristics for a hybrid inverter using an AlGaAs/GaAs heterojunction bipolar transistor are presented along with simulated data for an integrated device. These simulations lead to a modified structure demonstrating substantially improved transient response and reduced power dissipation (23 ps and 2.1 mW) while maintaining a large noise margin (45% of 3 V logic swing). Its performance is compared with emitter coupled logic (ECL).**

I. Introduction

Typically, bipolar logic families such as emitter-coupled logic (ECL) and current-mode logic (CML) use a small voltage swing to achieve high-speed operation. A new logic family and memory cell design providing abrupt voltage transitions, high noise margins, and large logic swing have recently been discussed by Gravrok and Warner (G & W) [1] in silicon. They proposed a concept that utilizes the large transconductance of bipolar transistors in series with a voltage shift and current limit function to produce logic gates with large logic swings, high noise immunity, and low power dissipation. In this work, we report a prototype hybrid inverter of this kind using GaAs diodes and depletion-mode FET's as the voltage regulator and current limiter, respectively. A high-gain AlGaAs/GaAs heterojunction bipolar transistor (HBT) was employed as the main switching element. Using these devices, the performance characteristics of this circuit architecture, shown in Fig. 1, were confirmed in GaAs. The threshold voltage of the diode regulates the input voltage while the current is limited by the FET to reduce the effects of HBT saturation, enhancing the high-speed performance and noise margin for logic low and high states. A modification to the original Noise Immune Logic (NIL) architecture is introduced to reduce the charge storage. The effect of various loading conditions such as capacitance and fanout is simulated and compared with an ECL gate.

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W. A. Hagley and D. Day are with Bell-Northern Research, Ottawa, Ont., Canada K1Y 4H7.
D. S. Malhi and J. M. Xu are with the Department of Electrical Engineering, University of Toronto, Toronto, Ont., Canada M5S 1A4.

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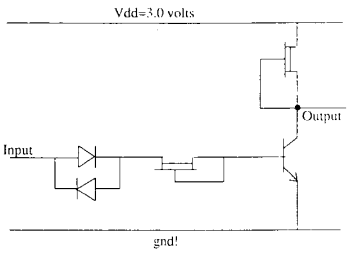

Fig. 1. The basic NIL circuit.

II. NIL Topology

A hybrid NIL gate was fabricated employing an n-p-n GaAs/AlGaAs HBT with current gain in excess of 1000. The fabrication and performance of these devices are described in detail elsewhere [2]. GaAs n^+ diodes and MESFET devices, produced by a GaAs foundry, were used as constant voltage and current elements and as pull-up devices. A primary gate circuit and measured transfer curve are shown in Figs. 1 and 2, respectively. The measured output high is within 1 mV of V_{DD} and the output low within 100 mV of ground. The noise margin, defined in [3] as the maximum spurious signal that can be tolerated by the device for correct operation, is measured by plotting the transfer characteristic rotated by 45° about the origin. This is shown in Fig. 2 where the voltage difference NM_H and NM_L are the noise margins for logic high and low states, respectively. We find that the measured noise margin for logic high is 54% and for the low state 40% for a 3 V logic swing, with a small temperature coefficient of 0.01%/K.

The transient response of the G & W hybrid NIL circuit was found to have a rise time exceeding 5 μs and a fall time of 80 ns while driving a 50-pF load. The slow rise time was attributed to stored charge in the base–emitter junction of the HBT which has no discharge path (other than recombination) once the input voltage falls below the threshold of the voltage-regulating element (diode). The prototype circuits, therefore, needed to be modified to prevent charge storage at this node. A second GaAs input diode was included in the circuit to provide a discharge path for this stored charge. This diode gave a factor of 60 improvement, and a measured rising and falling edge of 80 ns. Further scaling of this diode to improve the base–emitter discharge did not improve the transient response, so we conclude that our measurements were limited by the large loading capacitance (50 pF) of our simple wire-bonded circuit and apparatus. A further strategy to reduce the stored charge was to limit the current in the logic low state by gating the FET through a diode from the output node, as shown in Fig. 3. This reduces the power dissipation by more than 64% for little apparent change in the measured propagation delay. However, it was evident that simulation was essential to the understanding of the true limitations affecting the speed performance of these circuits.

III. Hspice Simulation for NIL and ECL

Hspice simulations were carried out using the standard level 1 diode, FET, and Gummel–Poon HBT models. The model [4], [5] details are listed in Table I. The modified circuit topology and simulated transfer characteristics are shown in Figs. 3 and 4, respectively. The calculated intrinsic noise margins for logic high and low states are 45% and 42%, resepectively for a 3 V logic swing. Fig. 5 shows the transient responses as a function of loading conditions, i.e., fanout (FO) = 0, 1, 5. It is observed that the logic high level has decreased by ≈400 mV while driving an FO of 5. This can be attributed to the low input impedance of a cascaded identical gate. This is in contrast to an ECL gate where the input impedance is very high. The gate delay was also studied by varying