A Recessed-Gap Capacitive-Gate GaAs CCD

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Abstract— **A new MESFET-compatible structure for GaAs capacitive-gate CCD's is presented that eliminates the necessity for submicrometer interelectrode gaps and simplifies device fabrication. This new recessed-gap structure solves the previous problems of low gate-channel-gate breakdown and large parasitic gate-to-gate capacitance associated with ultrasmall gaps. Dark current is also reduced. Modeling and experimental results are reported.**

I. Introduction

GaAs CCD's are important in many demanding signal processing applications because of their high speed and low-noise capability coupled with the electro-optic properties of GaAs and other III–V semiconductors. These attributes are a consequence of the high electron mobility and wide direct bandgap in this material system. Applications range from gigahertz transversal filters [1] to addressing schemes for bandgap engineered electro-optic devices [2]. In addition, because of their technological compatibility, GaAs CCD's are increasing in importance as a potential readout structure for emerging III–V heterostructure detectors.

Two CCD device structures based on Schottky barriers, rather than insulated gates, have found application in GaAs: capacitive-gate CCD's (CGCCD's) and resistive-gate CCD's (RGCCD's). CGCCD's rely on the proximity of adjacent gate electrodes to achieve efficient coupling between neighboring potential wells. The degree of coupling is a strong function of the active layer thickness and doping, as well as the interelectrode gap size. In order to avoid large potential troughs between adjacent potential wells, high charge transfer efficiency (CTE) CGCCD's have employed relatively thick, low-doped active layers [3]. We have previously reported results [4] demonstrating the strong correlation between potential trough depth and CTE and have obtained CTE exceeding 0.999 at 1 GHz on such material. However, the use of a highly doped channel layer is required for the integration of high-transconductance MESFET's, hence prior research in CGCCD's has focused on the use of submicrometer interelectrode gaps [5]–[7]. The undesirable result of these ultrasmall gaps is a decrease in gate-channel-gate breakdown voltage and an increase in gate-to-gate capacitance. RGCCD's eliminate the interelectrode gap entirely [8], [9]; however, the gates consume dc power and CGCCD-like structures remain necessary in serial–parallel–serial RGCCD multiplexers for the purpose of clock feedthrough isolation. In this letter a novel CGCCD structure exhibiting greater MESFET compatibility, while employing interelectrode gaps of 1 μm or greater, is presented.

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II. Device Structure and Modeling Results

A serious problem with GaAs CGCCD's is the existence of large potential troughs in the interelectrode gap region. The size of these troughs depends on the gap size, channel doping, and channel thickness. Fig. 1 shows a full two-dimensional solution to Poisson's equation in the interelectrode gaps between three gates. The simulation accounts for Fermi-level pinning at the GaAs surface, through the introduction of surface charge, and also the effect of the electrode thickness. Notice that in Fig. 1(b) the potential well depth in the channel under the interelectrode gaps is significantly greater than that under the gates and appears as a potential trough to electrons. The magnitude of the potential trough increases with increasing doping and decreasing active layer thickness. The interelectrode potential trough has the effect of reducing the CTE and dynamic range of the device, while increasing the minimum usable clock swing and therefore the dynamic power used by the CCD.

The origin of the potential troughs in the interelectrode gap can be qualitatively understood by considering the superposition of two one-dimensional solutions to Poisson's equation. A one-dimensional solution to Poisson's equation in the active layer, normal to the gate, indicates that for an empty potential well the channel potential is more positive than the gate by the pinch-off voltage of the active layer. If the same analysis is applied along the surface in the interelectrode gap, ignoring surface charge, the center of the gap is found to be more positive than the gates by an amount proportional to doping and gap size. The superposition of these two analyses suggests that the interelectrode potential trough can be reduced by two means: 1) reduction of the gap size, or 2) reduction of the channel thickness in the gap region which reduces the pinch-off voltage in the gap. Thus, proper recessing of the active area within the gap region can be used to eliminate the trough problem. Fig. 1(c) shows the potential wells under the three gates for recessed gaps. The potential trough has been nearly eliminated between the equally biased gates, and is nonexistent between the second and third gates. Such recessing does not significantly affect transfer speed. Overetching can yield potential barriers, but typically sufficient process latitude exists to avoid this situation.

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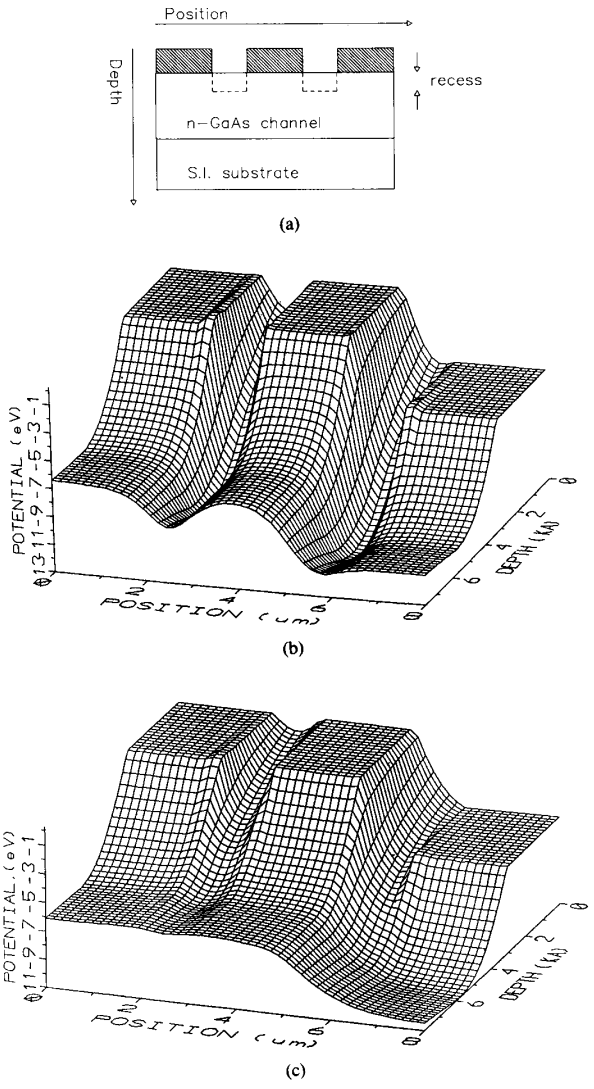

Fig. 1. Potential wells under three gates obtained by two-dimensional solution to Poisson's equation for a fully depleted channel. Channel region is toward viewer. (a) Schematic cross section of simulation structure (b) with no recess and (c) with gap recess of 1300 A. Channel is n-type, 0.285 μm thick, and doped at $1.2 \times 10^{17}/cm^3$. Electrodes (rear flat regions) are 0.3 μm thick, 2 μm long, and spaced 1 μm apart. The first two gates are biased at 0 V, and the third gate (right) is biased at +5 V.

III. Experimental Results

Experimental verification of the recessed-gap concept was conducted by characterization of CCD delay lines with various recess depths. The n-GaAs active layers were grown by MOCVD on an undoped buffer, which was grown on an undoped AlGaAs layer to facilitate backside fiber-optic coupling in future experiments [10]. Mesa isolation is used with Au–Ge alloyed ohmic contacts. Schottky-gate metal is e-beam deposited Cr followed by thermally evaporated Au. All metallizations are defined by lift-off. E-beam evaporated SiO is used as an interlayer dielectric, with contact vias also formed by lift-off. A second level of metal (Cr–Au) is used for interconnects. The CCD is organized as a four-phase, 50-stage (200 electrode) delay line. The transfer gates are 100 μm wide by 2 μm long, separated by 1-μm gaps. FET gate lengths are 1 μm. Fig. 2 is a photograph of the 1-μm gap delay line.

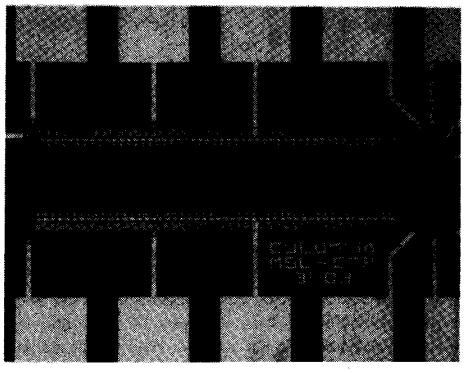

Fig. 2. Photograph of 50-stage four-phase delay line. CCD gates are 100 μm wide by 2 μm long with 1-μm interelectrode gap spacing. FET gate lengths are 1 μm.

The interelectrode gaps were recessed by wet etching with a weak 1:1:2000, $NH_4OH:H_2O_2:H_2O$ solution. The etch rate is approximately 100 A/min and etch depth is monitored using an Alpha Step surface profiler. Post-processing electrical measurements confirm the accuracy of the surface profiling, but indicate that the small geometry gaps may etch slightly faster than the larger structures where profile measurements are taken. Note that the on-chip MESFET output amplifiers are masked from the recessing etch.

Table I shows the experimental results for CCD delay lines fabricated from three different wafers, in four different batches. The value of the potential trough depth is determined by two-dimensional simulation. Note that DO3-9, DO3-2, and DO3-11 are devices from the same piece, and underwent identical processing. All of the data shown in Table I were obtained with a 12-MHz clock speed. For devices fabricated from the same wafer, recessed gap devices exhibited a dramatic increase in dynamic range. The results for dynamic range and CTE are not comparable for samples from different wafers because of the variation in material properties. The CTE for the experimental devices ranged from 0.92 to 0.9999. However, the minimum clock swing (MCS), which can be used without degradation in CTE, is largely independent of material properties. The MCS must overcome the effect of the potential trough and establish sufficient fringing fields to insure complete charge transfer. The MCS was determined by direct obsevation of the onset of output signal degradation. As Table I shows, independent of starting material, the MCS is significantly reduced for the recessed-gap devices. Simulation of an unrecessed 4-μm gap device indicates that the fully depleted potential trough depth should be approximately 40 V, suggesting that without recessing the CCD should be nonfunctional. However, with recessing, the 4-μm gap device was found to be operational with an MCS of 3 V.

The recessing etch also reduces the gate leakage current by minimizing the high fields at the gate periphery and allowing lower clocking voltages. The reduced dark current in combi-

TABLE I
EXPERIMENTAL RESULTS FOR RECESSED AND NONRECESSED GAP DEVICES

sample / wafer	Doping (cm^{-3})	Epi Thickness (A)	Pinch-off Volt. (volts)	Gap Size (um)	Recess Depth (A)	Pot. Trough Depth (volts)	Min. Clock Swing (volts)	Dyn. Range dB at 12 MHz
RC31-1 JIS#2	$2x10^{17}$	1350	1.7	1	0	4.1	2	53
RC32-7 JIS#3	$2x10^{17}$	1350	1.7	1	300	2.0	1	40
N04-1 JIS#3	$2x10^{17}$	1350	1.7	1	500	0.4	1	63
D03-9 REC#4	$1.2x10^{17}$	2850	6.0	1	0	4.9	4	30
D03-2 REC#4	$1.2x10^{17}$	2850	6.0	1	1300	0.4	1	52
	$1.2x10^{17}$	2850	6.0	4	0	40		
D03-11 REC#4	$1.2x10^{17}$	2850	6.0	4	1300	11.8	3	27

nation with the improved dynamic range permitted DO3-2 to be run at 100 times slower clock speed than that possible with the unrecessed counterpart DO3-9. Slower clock speeds are important for imager applications.

IV. CONCLUSIONS

A new recessed-gap, MESFET-compatible, GaAs CGCCD structure with large electrode spacing has been presented. Experimental confirmation of reduction of the interelectrode potential troughs has been obtained, with the benefits of increased dynamic range and lower minimum usable clock swings and frequencies. The recessed gap should significantly improve high-frequency CTE for devices fabricated on optimized, thin, highly doped active layers.

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