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A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor

A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, E.R. Fossum

Photobit Corporation
135 N. Los Robles Avenue, 7th floor, Pasadena, CA 91101, USA
(626) 683-2200 *www.photobit.com*

Abstract

The paper presents a high-speed (500 f/s) large-format 1Kx1K 8 bit 3.3V CMOS active pixel sensor (APS) with 1024 ADCs integrated on chip. The sensor achieves an extremely high output data rate of over 500 Mbytes per second and a low power dissipation of 350 mW at the 66 MHz master clock rate. Principal architecture and circuit solutions allowing such a high throughput are discussed along with preliminary results of the chip characterization.

Introduction

CMOS sensors emerged in the early 1990s as a low-cost low-power alternative to CCDs [1]. Today, CMOS APS is challenging CCD technology in mainstream applications such as Digital Still Cameras (DSCs). However, there are niches where CMOS APS seems to have little competition. One of these niches is in high-speed, large-format imaging for machine vision and motion analysis. CMOS sensor designs enable the use of parallel pixel readout and digitizing, as well as easy ways of multiplexing/demultiplexing data - techniques required for high speed large format sensors.

Our progress in high-speed large-format CMOS sensors is occurring rapidly. This paper presents an innovative CMOS sensor that is already an order of magnitude improvement in throughput compared to our recently reported CMOS APS [2].

Achieving high speed and high performance

A. Architecture.

The principal architectural solutions which have enabled the high output data rate were the following: column-parallel ADCs (1024 in total), 2 row high speed dual-port RAM, and data demultiplexing (there are total 8 of 8-bit outputs).

The sensor core consists of a 1024x1024 photodiode active pixel array with 10 μm pitch. The array of pixels is accessed in the standard row-wise fashion so that all pixels in the row are read out into the column ADCs in parallel [3]. It was difficult to lay out a high performance ADC in one column pitch, so the odd/even column circuits were split between the top and bottom of the array (Fig.1). Although this separation presented a potential fixed pattern noise (fpn) issue, no measurable odd/even nonuniformity has been found.

The column ADC front-end circuit (Fig.2) is simple. There are 2 source-followers between the photodiode and the ADC. Each draws about 15 μA. The time budget is 1μs for sampling

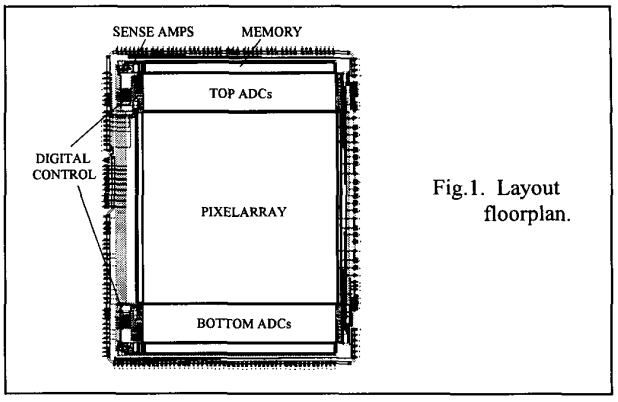

Fig.1. Layout floorplan.

data into ADC, and 1μs for conversion.

One of the concerns when using multiple ADCs is fpn between the channels. Considerable attention was paid to optimize the ADC operation. A careful comparator layout resulted in ~30 mV offset (a good value for a simple dynamic comparator, the only low-power option for usage in such an architecture) which has been further corrected using a calibration capacitor bank. During calibration, the signal is sampled from a circuit that mimics the pixel-reset level.

ADC timing was optimized as well. Regular successive-approximation sequence includes 3 stages: a preset (trial of a new binary voltage), comparison, and latching the result. In the implementation, the stage 3 was combined with the stage 1 for the next bit.

Another innovation which made it possible to read the digital data of one row during the conversion of the next row was the addition of a 16Kb column-parallel dual-port 2 row SRAM

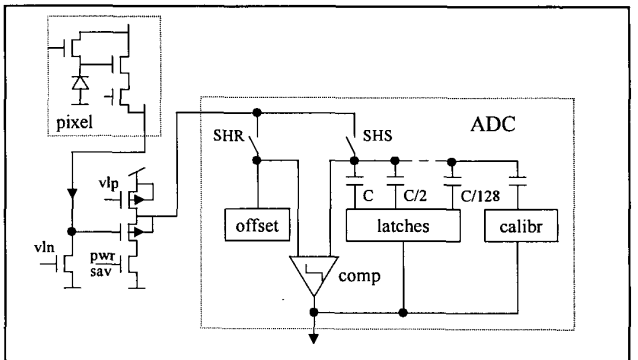

Fig.2. Schematic of ADC and column read circuit.

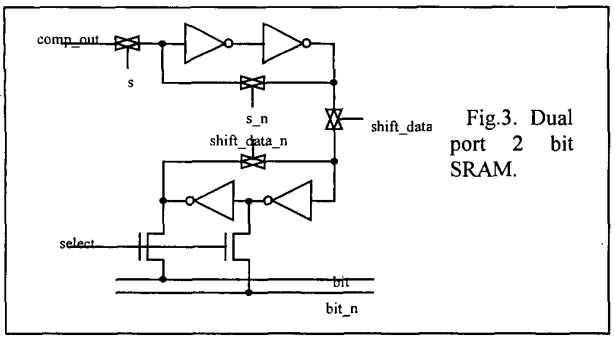

Fig.3. Dual port 2 bit SRAM.

into the sensor. The data is sequentially sampled into the front-end SRAM cell (Fig.3.) as soon as it is available from the ADC during digitization, and is shifted into the back-end cell for readout when the digitization is complete. The separation of the readout site from the ADC allows doubling the sensor speed by supporting simultaneous conversion and readout. The ADC also gains better isolation from noisy data read paths.

The readout from the SRAM is done by high speed differential sense amplifiers. Eight columns of 8-bit data are read in one clock cycle. The data are demultiplexed so that the columns 1,3,5,7 in the bottom and 2,4,6,8 at the top go to separate pads. Output pads were designed to drive a 15pF load at 66 MHz & 3.3V and are the dominant power consumers.

The sensor has an on-chip digital block, which runs the row processing, ADC conversion, and readout. It allows flexibility in selecting rows and columns as well as defining the start time for row processing or read.

B. Results.

Several boards has been designed and the sensor has been successfully run at different speeds: 15 f/s, 60 f/s, 474 f/s, and 574 f/s. At 574 f/s some very minor artifacts appeared, which we believe could be removed by proper synchronization of multiple outputs. The results of the sensor characterization at 15 f/s are presented in the following table and drawings.

Table 1.

Technology	0.5 um 2P 3M CMOS
Pixel array size	1024 x 1024
Pixel pitch	10 um
Conversion gain	11 uV/e
Noise	50e
QE * Fill factor	45 %
Dark signal	30 mV/s
Saturation	1V
Fixed pattern noise	0.2 % Vsat rms, or 3mV p-p
Column ADC	8 bit (7bit accuracy)
Power supply	3.3 V
Number of outputs	64 or 8 x 8 bit
Data rate	up to 500 Mpix/s
Power consumption	350 mW at 474 f/s
	Or 95 mW at 60 f/s

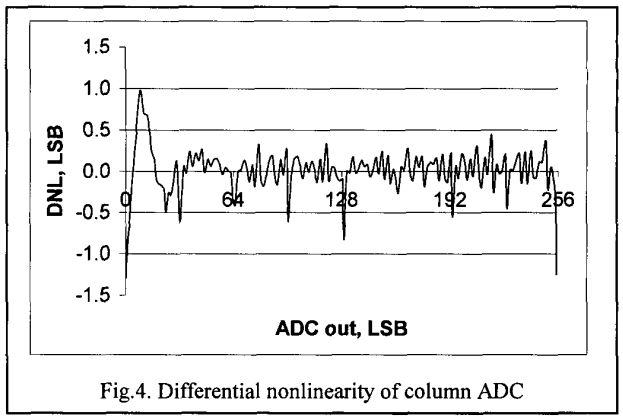

Fig.4. Differential nonlinearity of column ADC

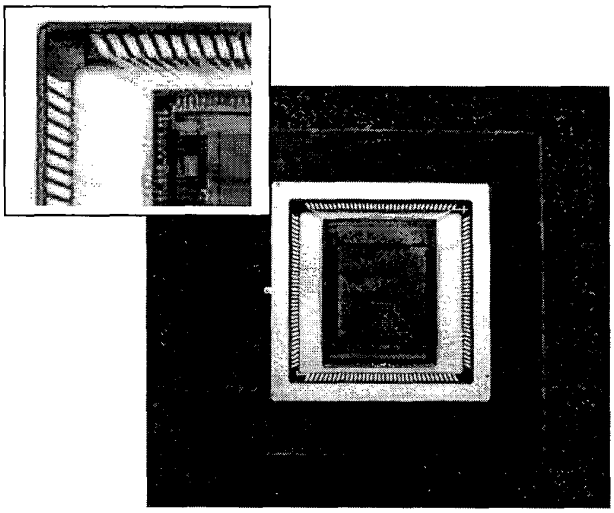

Fig.5. A self portrait snap shot taken by the 1024x1024 sensor. Inset shows enlarged portion of image.

Acknowledgment

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References

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