A DIGITAL CMOS ACTIVE PIXEL IMAGE SENSOR FOR MULTIMEDIA APPLICATIONS

Zhimin Zhou, Bedabrata Pain*, Jason Woo, and Eric R. Fossum*

Electrical Engineering Department
University of California, Los Angeles
405 Hilgard Ave.
Los Angeles, CA 90095

Tel. 818-354-3292
Fax 818-393-0045
E-mail zhou@icsl.ucla.edu

* Center for Space Microelectronics Technology
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

ABSTRACT

Two charge-scaling successive approximation A/D converters for on-focal-plane column-parallel data processing in CMOS active pixel image sensors (APS) are presented. The converters are designed in a thin but long fashion to fit a pitch size of 40 μm for 2.0 μm technology and 24 μm for 1.2 μm technology. Designed for multimedia and other commercial and industrial applications, each in column A/D converter achieves 8 bit resolution and accuracy with a signal swing of 1 V. Maximum conversion rate exceeding 200 kHz enables high speed digital readout beyond 200 frames/sec for large format 1K x 1K CMOS image sensors. A prototype device of 64 X 64 APS image array with 8 bit digital output was demonstrated up to 1 kHz frame rate, and with column-wise non-uniformity less than 2 LSBs.

KEWWORDS: CMOS active pixel image sensors, on-focal-plane A/D conversion, digital image sensor, column-parallel ADC

I. INTRODUCTION

CMOS active pixel image sensors (APS) have recently emerged as a low cost alternative to charge-coupled devices for many applications [1,2]. The CMOS APS features good quantum efficiency, low read noise, high dynamic range, random accessibility, and 100% compatibility with on-chip CMOS circuits for control, timing [3] and analog-to-digital conversion. This technology enables digital camera-on-a-chip which requires on-focal-plane A/D converters. Column-parallel single slope [4, 5], and Σ–Δ [6] A/D converters have been previously reported. These architectures are relatively slow. This paper presents the first application of faster column-parallel successive approximation A/D converters to CMOS APS sensors.

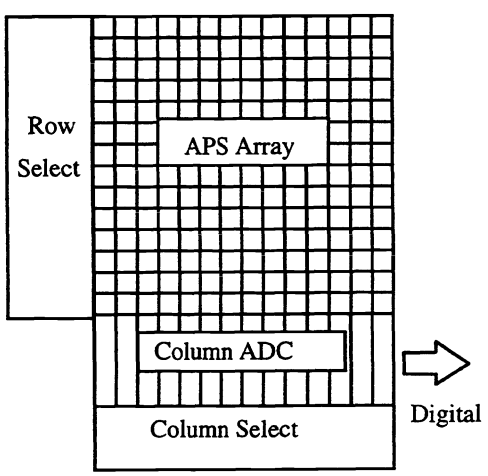

Fig. 1. Chip configuration of a CMOS digital APS, semi-parallel scheme with one ADC per column.

Figure 1 illustrates the chip configuration of the digital sensor. It is a semi-parallel structure featuring one A/D converter in each column. On-focal plane A/D conversion eliminates the necessity for on-chip large analog drivers,

0-8194-2295-9/96/$6.00

reducing chip power consumption and total system noise. The semi-parallel A/D conversion scheme further alleviates the problem compared with a fully serial scheme (one A/D converter per chip) because of much lower operating bandwidth of the converters [7] . For instance, a 1K x 1K sensor operating at typical video frame rate requires a 30 MHz conversion rate for single converter per chip. On the other hand, employing the column-parallel architecture, the ADC conversion rate can be reduced to 30 kHz while maintaining the data output rate at 30 MHz. The semi-parallel scheme is thus suitable for many higher frame rate, low noise and low power applications, especially in interfacing with on chip digital signal processing and computation necessary for smart sensing techniques.

Two different successive approximation A/D conversion algorithms are discussed in Section II, and designs based on them are presented in Section III. The performance of these converters is compared in Section IV. A CMOS imager array incorporating one of the A/D converter implementation was build. The test results on the digital imager is presented in Section V.

II. A/D CONVERSION ALGORITHMS

Figure 2 shows a typical photogate CMOS active pixel sensor. It consists of a photogate (PG), a transfer gate (TX), a reset transistor and a source follower buffer between the floating diffusion (FD) and the column bus. Typical CMOS APS employs a correlated double sampling readout [1]. Once a row in the array is addressed, the floating diffusion is first reset, a reset level is sampled at the column bus. The photogate is then pulsed to dump the accumulated charge to the floating diffusion, a signal level is then sampled at the column bus. The difference of this two sampled measurements is the signal that is proportional to the intensity of the incident light. As a result of this readout, reset and signal levels of a given pixel are sampled consecutively on two separate column capacitors. Successive approximation A/D conversion is then performed by making the two levels progressively converge towards each other in a binary-scaled fashion. There are two different ways to make them converge. The graphic illustration using the progression of the signal and reset levels in the two different approaches are shown in Figure 3. In the single sided approach, the voltage on the reset bus is held constant while the signal bus is successively charged up by binary-weighted voltage. The

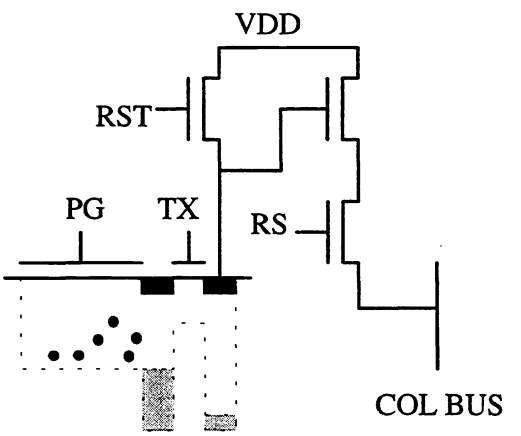

Fig. 2. Photogate APS pixel design, a mini-CCD stage buffered by a source follower.

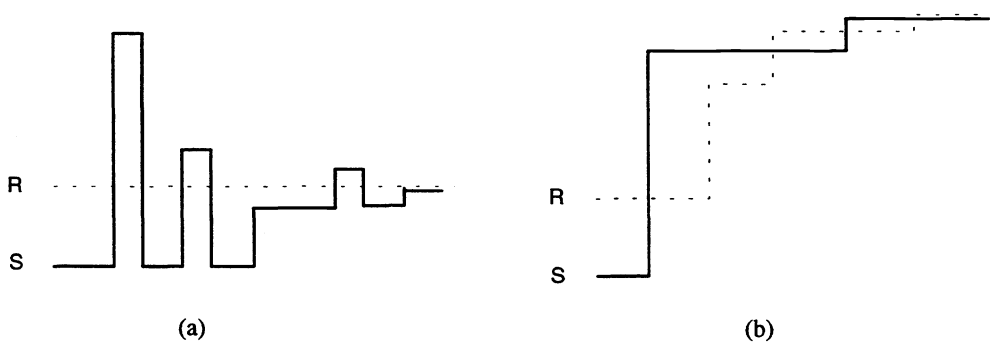

Fig. 3. Voltage progression in (a) single-sided converter, signal level charged and discharged while reset level held constant, (b) doubled-sided converter, lower voltage charged up in each step of conversion.

voltage reduces back to its previous level every time it exceeds the reset level. The algorithm is mathematically expressed as the following:

$$V_{S,i} = V_{S,i-1} + b_i \frac{V_{ref}}{2^i}$$

$$V_{R,i} = V_{R,0}$$

$$b_i = 0 \qquad \text{if } V_R - V_{S,i-1} < \frac{V_{ref}}{2^i}$$

$$= 1 \qquad \text{if } V_R - V_{S,i-1} > \frac{V_{ref}}{2^i}$$

Where i = 1 to 10 for a 10 bit converter. In the double sided approach, the progressively smaller weights are added to whichever bus has the lower voltage. Voltage on both bus lines increase while they are converging. The algorithm is mathematically represented by the following:

$$V_{S,i} = V_{S,i-1} + b_i \frac{V_{ref}}{2^i}$$

$$V_{R,i} = V_{R,i-1} + \overline{b_i} \frac{V_{ref}}{2^i}$$

$$b_i = 0 \qquad \text{if } V_{R,i-1} < V_{S,i-1}$$

$$= 1 \qquad \text{if } V_{R,i-1} > V_{S,i-1}$$

III. DESIGN AND OPERATION OF THE A/D CONVERTERS

Figure 4 is the schematic block diagram for the single sided successive approximation A/D converter. It is similar to the charge redistribution A/D converter first introduced by J. L. McCreary and P. R. Gray [8]. It is designed to have 10 conversion unit cells for 10 bit resolution, although it is possible to operate at a lower resolution. A single capacitor, which holds the reset level, and a bank of binary-weighted capacitors, which hold the signal level, are connected to the input of the comparator. The digital word from the comparator is fed back to the bit cells, B1 through B10, progressively as they are scanned through BS1 to BS10 by a shift register. The comparator is a nominal cross-coupled differential pair that performs reset and comparison in a strobed fashion. A single bit cell consists of a

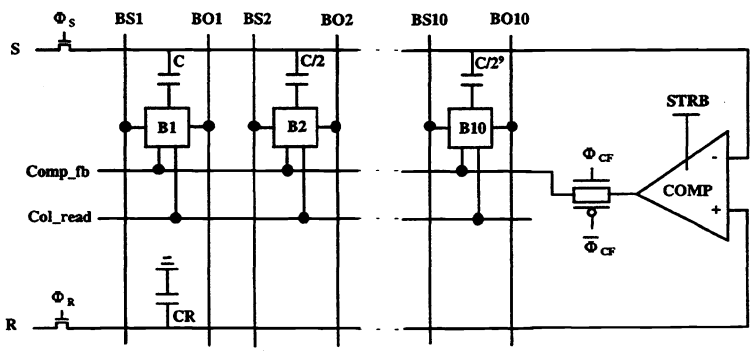

Fig. 4. Schematic diagram of the single sided A/D converter, single capacitor onreset side and binary-scaled capacitors on signal side connected to the input of the comparator.

latch and a pair of switches that connect the bottom of the capacitor to either GND or the reference voltage (V_{ref}) depending on whether the latched word is "0" or "1". At the beginning of the conversion, all bit cells are reset and the bottom of the capacitors are connected to GND. Sensor reset and signal level are then sampled on the capacitors. Switching the bottom plate of the capacitor of value C charges the signal level up by a binary-weighted voltage of $V_{ref}(C/C_{tot})$. The following strobe feeds back a "1" if the comparator determines the signal level to be still lower than the reset level, and the signal level is retained at the increased voltage. Otherwise a "0" is fed back and

the signal level is restored to its previous value. This bit word is latched in the bit cell and the conversion proceeds to the next MSB. Two strobe cycles are needed for one bit conversion in this operation.

In the double sided implementation (Figure 5), both signal and reset capacitors are binary-weighted. Two latch cells instead of one as in single sided design are used for each bit cell. At each strobe of the comparator, the comparator output is fed back to the sequentially selected bit cell so that the bottom plate of one capacitor is connected to V_{ref} and that of the other to GND. The voltage at the lower voltage bus is then raised up by the binary-distributed amount of V_{ref}, while that at the other bus remains the same. The latched digital data on both sides are complementary and data from either side can be used as the digital representation of the original analog signal.

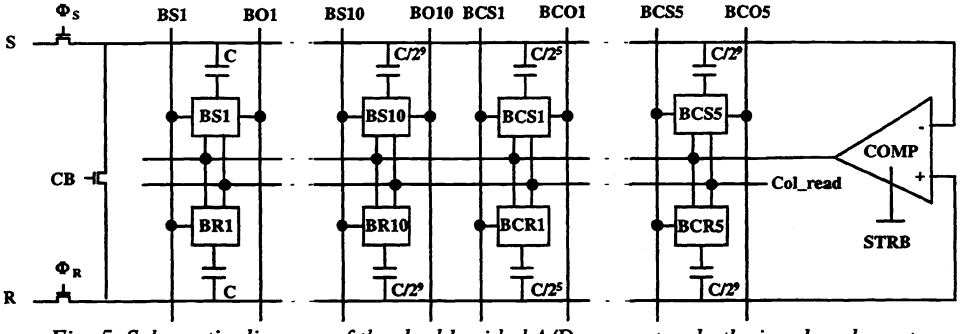

Fig. 5. Schematic diagram of the double sided A/D converter, both signal and reset capancitors are binary-scaled.

Five correction bit cells, which are the same sizes as the five LSBs, are implemented in the double sided design. After a crowbar (CB) short between the signal and reset buses, the similar conversion process stores the converted comparator offset voltage as the correction bits. The first bit serves as a sign bit which determines an addition or subtraction of the correction bits relative to the original digital words. The DC offset of the comparator is the major contribution to the column-wise fixed pattern noise (FPN) and is compensated to a first order by using this offset correction method.

Double sided converter needs only one strobe cycle for each bit of conversion. It operates much faster than single sided design. On the other hand, it needs much more chip area because an equal amount of capacitance has to be connected to the reset bus and each unit cell consists of two latches. Furthermore, it requires extra component matching between the capacitors connected to the two bus lines in order to get the same conversion accuracy.

III. EXPERIMENTAL RESULTS OF THE CONVERTERS

Two different converters have been fabricated using different technology. The double sided design used 2 μm n-well double poly technology and has a 40 μm pitch. The single sided design used 1.2 μm n-well single poly technology and has a 24 μm pitch. In these long, thin designs, special caution has been taken to minimize the chip area in the limited pitch space available for routing.

The converters are characterized using static linearity testing technique in which the converters operate as in typical image sensor readout. A ramp signal of 1 V magnitude from a 16 bit PC DAC board is fed to the input of the A/D converter. The digital word from the A/D converter is converted back to analog signal and read into a computer by a 16 bit ADC board. The performance of the two design is summarized in Table 1 along with their design parameters. All the measurement are taken at the conversion rate of 50 kHz, corresponding to over 40 Hz frame rate for a 1024 x 1024 sensor array. The maximum conversion rate quoted is that at which the A/D converters are operational to 5 bit accuracy. Measurement indicates that at the same conversion rate below 200 kHz, accuracy of the single sided design is better than that of the double sided design as theoretically predicted, since the component matching dominates the settling time in limiting the conversion accuracy at lower speed. For commercial video applications at lower conversion rate, the single sided design is a better choice because of higher accuracy and smaller chip area. The double sided design is the better choice for higher speed readout applications in which a

conversion speed beyond 200 kHz is required. Figure 6 shows the linearity test results for the single sided design at 50 kHz data rate. Both the DNL and INL are less than ±1 LSB. Figure 7 shows the transfer curve of the doubled sided converter at 500 kHz conversion rate. 6 bit accuracy is retained at this speed.

Table 1 - Summary of the test results of the A/D converters

	Max. DNL (LSB)	Max. INL (LSB)	RMS Noise (LSB)	Max.* Power (μW)	Max. Speed (kHz)	Size (μm x mm)	Design Rule
Single	0.8	1.0	1.2	149	230	24 x 2.1	1.2μm
Double	1.0	2.0	1.6	87	800	40 X 4.8**	2.0μm

* simulated maximum power with most frequent capacitor switching

** area for correction bit subtracted

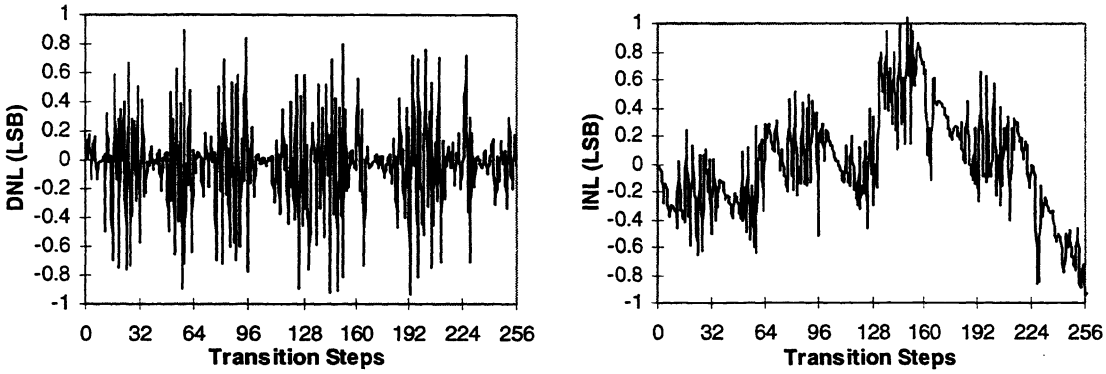

Fig. 6. Nonlinearity test results of the single sided A/D converter at 50 kHz conversion rate, DNL is about 0.8 LSB and INL 1 LSB.

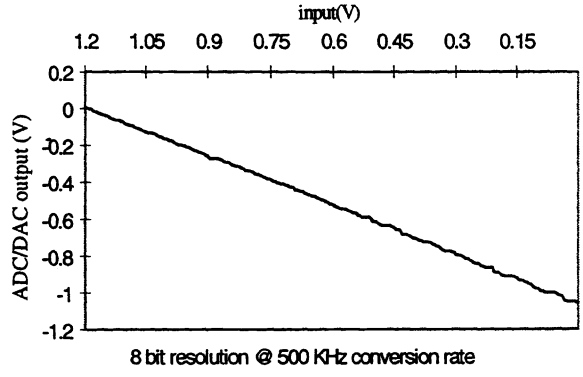

Fig. 7. Tranfer curve for the double-sided converter at 500 kHz conversion rate, 6 bit accuracy is ratained.

IV. 64 X 64 CMOS DIGITAL IMAGE ARRAY

A prototype digital sensor using single sided A/D converters was implemented. It is a 64 x 64 element array fabricated through MOSIS using standard 1.2 μm n-well CMOS technology. The photomicrograph of the chip is shown in Figure 8. It consists of a photo gate pixel array [2], a column A/D converter array with shift register control circuit, and sensor row and column addressing circuits. The column A/D converters occupies about 58% of the chip

core area in this small array. This percentage will drop dramatically to 8% as the array size increases to 1024 x 1024. The total dye size of the fabricated array is 3 mm x 5 mm.

The sensor chips were tested at up to 1 kHz frame rate. Eight bits parallel digital output were fed into a DAC that converts the digital data into an analog image. The acquired images were monitored using a TV monitor driven by a scan converter. Quantitative measurements were taken at 100 kpixels/sec (24 full frames/sec) readout rate. Figure 9 shows a raw image of 32 x 64 elements captured at 100 kHz pixel rate. There is no visible degradation in image quality compared to a similar sized CMOS APS with analog output. The sensor demonstrates random access and windowing capabilities. The image data retains 8 bit resolution up to 1 kHz full frame rate. The column-wise FPN is measured to be less than 2 LSBs.

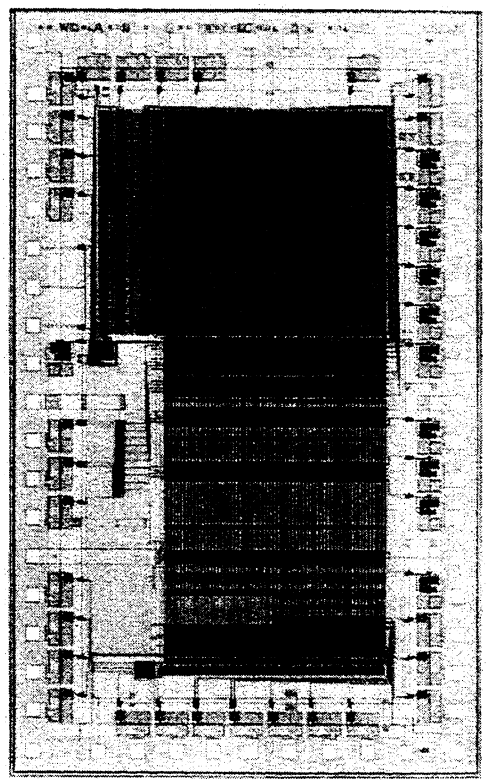

Fig. 8. Photomicrograph of the digital imager, 64 x 64 APS array with 1 x 64 ADCs.

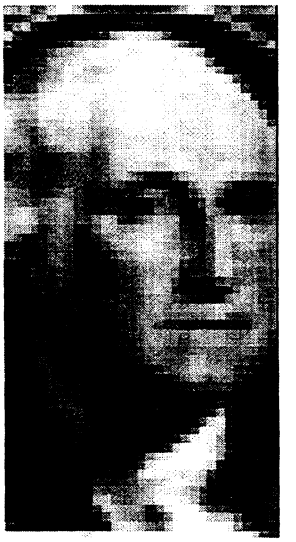

Fig. 9. Raw Image taken at 100 kPixels/sec. 8 bit resolution achieved.

V. CONCLUSION

Two different implementation of column-parallel charge-scaling successive approximation A/D converters were designed, fabricated and tested. The single sided design has advantages on accuracy and chip area, while the double sided design on speed. They are both suitable for regular video applications while the double sided implementation has special use for high speed imaging, possibly up to 1 kHz frame rate for a 1K x 1K sensor.

A prototype CMOS APS with on-focal-plane column A/D converters has been demonstrated. Images with 8 bit accuracy were achieved up to 1 kframes/sec (4 Mpixels/sec) readout rate. Column-wise non-uniformity of the sensor is within 2 LSBs (0.8% of the 1 V sensor saturation). It is possible to digitally correct the FPN to under 1 LSB using the on-chip offset correction.

VI. ACKNOWLEDGMENTS

The authors would like to thank S. Kemeny, J. Kohler , R. Nixon, R. Panicacci and C. Staller at the Jet Propulsion Laboratory for their technical assistance in this work. The research presented in this paper was carried out at the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology,

and was supported in part by the Defense Advanced Research Projects Agency and the National Aeronautics and Space Administration, Office of Advanced Concepts and Technology.

REFERENCES

[1], S. K. Mendis, S. E. Kemeny, and E. R, Fossum, "A 128X128 CMOS Active Pixel Sensor for Highly Integrated Imaging Systems," IEEE IEDM Technical Digest, pp. 583-586, Dec. 1993.

[2], E. R. Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," IEEE IEDM Technical Digest, pp. 17-25, Dec. 1995.

[3], R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "256X256 CMOS Active Pixel Sensor Camera-on-a-chip," IEEE ISSCC Digest of Technical Papers, pp. 178-179, Feb. 1996.

[4], B. Ackland and A. Dickinson, "Camera on a Chip," IEEE ISSCC Digest of Technical Papers, pp. 22-25, Feb. 1996.

[5], C. Jansson, P. Ingelhag, C. Svensson, and R. Forchheimer, "An Addressable 256 x 256 Photodiode Image Sensor Array with an 8-Bit Digital Output," Analog Integrated Circuits and Signal Processing, vol. 4, pp. 37-49, 1993.

[6], S. Mendis, B. Pain, R. Nixon, and E. R. Fossum, "Design of a Low-light-level Image Sensor with an On-chip Sigma-delta Analog-to-digital Conversion," Proceedings of SPIE, vol. 1900, pp. 31-39, CCD's and Optical Sensors III, 1993.

[7], B. Pain, E. R. Fossum, "Approaches and Analysis for On-focal-plane Analog-to-digital Conversion," Proceedings of SPIE, vol. 2226, Aerospace Sensing-Infrared Readout Electronics II, Apr. 1994.

[8], J. L. McCreary and P. R. Gray, "All-MOS Charge Redistribution Analog-to-digital Conversion Techniques - Part I," IEEE J. Solid State Circuits, vol. SC-10, pp. 371-379, Dec. 1975.