# Regular Brief Papers

## A Current Memory Cell with Switch Feedthrough Reduction by Error Feedback

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*Abstract*—**A new switch feedthrough suppressing current memory cell, capable of accurately memorizing low current levels is presented. The scheme operates by feeding back a fraction of the error current to the storage node whose voltage is adjusted so that the error is reduced to zero. Using the feedback compensation scheme, absolute current error of less than 0.1% was achieved even at ultra-low current levels of 10 nA. The negative feedback circuit consumes negligibly low power and can be laid in a very small area. With this scheme, memory accuracy is traded for error correction speed, a feature common to all feedback-based switch feedthrough reduction schemes. The feedback compensated current memory cell can be used for low-power high-background infrared focal-plane readout electronics featuring in-pixel background suppression.**

### I. Introduction

CURRENT memory circuits have been widely used in analog sampled-data signal processing applications [1], [2] since they exhibit superior tolerance to MOSFET parameter variations. Current memory arrays have achieved less than hundred parts per million relative error [3], when operated at relatively high currents (>1 $\mu$A). However, their absolute error (defined as the difference between the memorized and the read out current) can be significantly large due to switch feedthrough, finite output impedance, and parasitic capacitive coupling. Typically, switch feedthrough is the dominant source of error, increasing for lower operating currents. For ultra-low currents (less than 100 nA), this error can be greater than 25%, severely limiting its use in low power applications.

A high absolute accuracy will be beneficial in many situations. An efficient dynamic range management can be achieved in infrared focal-plane readouts by using accurate current memory cells for estimation and subtraction of the background current. In such applications, current memory arrays are required to operate at ultra-low current levels (<200 nA) and with very low absolute errors (<0.1%) [4].

Several techniques exist for reduction of error caused by switch feedthrough. Feedthrough reduction using dummy transistor compensation is not practicable for achieving low errors, since accurate feedthrough cancellation is achieved only for a narrow range of voltage levels, and is dependent critically on the switching transistor sizes and capacitive loads [5]. Even with a slow switch turn-off, reduction of feedthrough-related errors to less than 1% requires a large cell capacitance, resulting in prohibitively large cell sizes [6]. Other switch feedthrough reduction schemes include use of capacitive feedback [7], adaptation of clock swing [3], and use of algorithmic techniques [8]. None of these approaches has been used in conjunction with current memory cells operating at ultra-low memorizing currents. Further, these approaches are not suited for low-power, high-density focal-plane applications.

A current memory cell, capable of operation at ultra-low currents with high absolute accuracy, is presented in this paper. The feedthrough reduction scheme is explained. Noise in the circuit is estimated and experimental results relating to absolute error reduction are presented.

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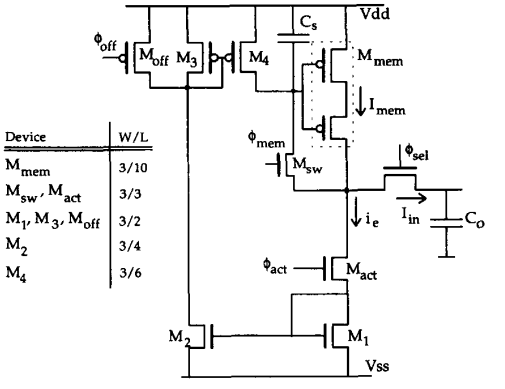


Fig. 1. Circuit diagram of the error feedback compensated current memory cell.

### II. The Switch Feedthrough Suppression Scheme

The circuit diagram of a new switch feedthrough reducing current memory cell capable of ultra-low current operation is shown in Fig. 1. The circuit consists of a self-cascoding [4] composite memory transistor ($M_{\text{mem}}$), a storage capacitor ($C_s$), a feedback network consisting of current mirrors ($M_1, M_2, M_3, M_4$), and single-FET switches ($M_{\text{act}}, M_{\text{off}}, M_{\text{sw}}$).

The switch feedthrough as a result of turning off $M_{\text{sw}}$ causes the current through $M_{\text{mem}}$ to be larger than the memorizing

current. This causes an error current $i_e$ to flow through $M_1$. Mirrored by $M_1$-$M_2$ and $M_3$-$M_4$ pairs, only a fraction a of this error current flows through the output transistor ($M_4$) of the composite current mirror. The current flowing through $M_4$ is determined by $W/L$ ratios of the current mirror transistors, and is proportional to the error current $i_e$. $M_4$ is directly connected to the storage capacitor $C_s$, completing the feedback loop. Once the feedback network is activated, the drain current of $M_4$ starts to integrate on $C_s$, causing a change in the gate voltage of $M_{\text{mem}}$. This change is in a direction which reduces the current flowing through it, causing a reduction in the error current. The negative feedback process continues until $i_e$ goes to zero. Ideally the current flowing through $M_4$ stops, once the error is reduced to zero. The switch $M_{\text{off}}$ can be pulsed low to restrict the amount of residual tail current in $M_4$, after the error has been reduced within a given accuracy limit. No feedthrough is added as a result of this operation, since there is hardly any channel-charge left in $M_4$, and because the $M_4$ gate voltage change is minimal.

The feedback circuit consists mainly of minimum-sized transistors, and therefore can be laid out in a relatively small silicon area. Most of the area is actually taken up by the storage capacitor. The circuit uses only one additional switching transistor compared to the switch feedthrough reduction circuit using a dummy transistor, and consumes very little extra power, since the feedback circuit operates with a fraction of the actual memorizing current.

Assuming that the main time constant of the memory is associated with the capacitance of the storage node and output conductance $g_{\text{out}}$ of $M_4$, time dependence of $i_e$ can be determined by solving the differential equation describing the feedback behavior, and is given by:

$$i_e(t) = I_e \exp\left(-\frac{g_{\text{out}} + \alpha g_{\text{mm}}}{C_{\text{store}}} t\right) \cong I_e \exp\left(-\frac{\alpha g_{\text{mm}}}{C_{\text{store}}} t\right) \quad (1)$$

where $i_e(t = 0) = I_e$, $\alpha$ is current mirror ratio, $g_{\text{mm}}$ is the transconductance of $M_{\text{mem}}$, and $i_e(t)$ is the instantaneous value of the error current. Equation (1) shows that the error current depends exponentially with error compensation time duration. Further, for small memorizing currents, required compensation time (and hence memory write-time) increases due to a decrease in $g_{\text{mm}}$. The time constant of the feedthrough compensation process is given by $C_{\text{store}}/\alpha g_{\text{mm}}$, and is dependent both on the current mirror ratio and actual current memorized. Thus, there is a trade-off between the speed of feedthrough reduction and the magnitude of residual error. The problem is accentuated by the fact that the feedback operates only in one direction. The feedback circuit was designed with $\alpha = 0.16$, so as to strike a compromise between accuracy of the memory cell and speed of feedthrough suppression. For a current of 50 nA, and for $\alpha = 0.16$, this feedback time constant is about 4 $\mu$s.

Noise is added to the memory cell both during write and read operation. Data-write operation adds reset noise that appears as a random offset during the memory read operation. Noise is also added during read operation by $M_{\text{mem}}$ and the load. The main component of reset noise is due to channel noise in $M_{\text{mem}}$, while noise in the feedback loop is suppressed due to feedback. The mean square variation at the storage node at the end of the write cycles is approximately given by:

$$\langle v_n \rangle^2_{\text{rst}} \cong \frac{2}{3}\frac{\alpha kT}{C_s} \quad (2)$$

The result is similar to that obtained for a conventional current memory [9], with the exception that the reset noise due to the memorizing transistor is suppressed by the current ratio $\alpha$. For $\alpha = 0.15$, and $C_s > 0.35$ pF, the absolute error due to reset noise is estimated to be smaller than 0.1%.

The effect of MOSFET channel noise during readout can be estimated by assuming that the current memory cell is connected to an integrator, a loading condition frequently encountered in the focal-plane readouts. The noise voltage at the output of the integrator depends on the integration time, and is approximately given by:

$$\langle v_n \rangle^2_{\text{read}} = \frac{8}{3} kT \frac{g_{\text{mm}}}{C_o^2} \Delta t \quad (3)$$

where $C_o$ is the integration capacitor, and $\Delta t$ is the integration time. For $\Delta t = 100$ $\mu$s, $C_o = 3$ pF, and bias current of 100 nA, the rms noise voltage at the output is only 0.3 mV, or less than 0.01% error in the readout current. This indicates that the memory error due to noise is insignificant in comparison to the error due to switch feedthrough.

## III. Experimental Results and Discussion

In order to test the performance of the switch feedthrough suppressing current memory, a 32 × 1 linear array of current memory cells was fabricated using a 2-$\mu$m double-poly CMOS process. The current memory cells were designed for operation at current levels ranging from 10 nA to larger than 500 nA. Self-cascoding transistors [4] were used in order to ensure that error due to output conductance is smaller than that due to switch feedthrough. The error due to junction leakage was also found to be insignificant. The total storage capacitance was 0.4 pF, and the unit cell area was 50 × 45 $\mu$m$^2$.

The current was measured indirectly by integrating the current on a 3.05 pF capacitor, and measuring the voltage on the capacitor. Test setup resolution was limited to 0.1%. Fig. 2 is the oscilloscope photograph of the current readout process. The first and the third sawtooth waveforms represents integration of the current to be memorized, and the second waveform indicates integration of the current output from the memory cell. In Fig. 2 the memorized current was 31.28 nA, and the feedback compensation time was 50 $\mu$s. No discernible absolute error between the current read out and the current memorized can be detected from Fig. 2, indicating that error has been reduced to a negligibly small value.

The error in the current was measured both with and without feedback. Without feedback, errors as high as 35% at a current of 100 nA were measured. The error reduced to about −0.1%, irrespective of memorizing current levels, when feedback was established. Fig. 3(a) is a plot of the error in the output of a memory cell as a function of the time duration for which the feedback network was activated. The required error

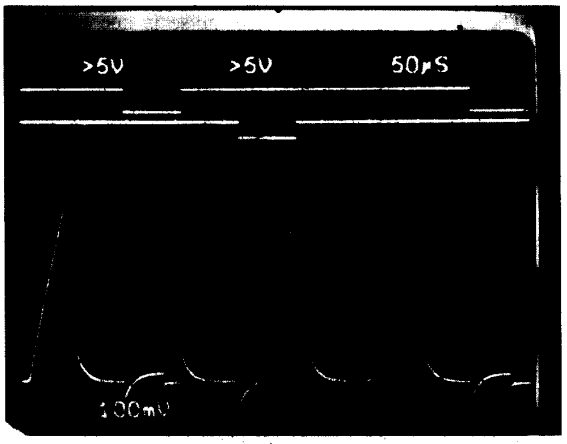


Fig. 2. Oscilloscope photograph showing integration of input and output current from a single memory cell.

compensation time is dependent upon the magnitude of the current memorized, and is generally smaller for larger current levels. The error convergence is found to be approximately exponential as predicted by (1). The rate of convergence was also slower for smaller currents, since the time constant depends inversely on the transconductance. The difference between the predicted and the measured compensation time is due to the presence of a large bus capacitance in the test structure.

Fig. 3(b) indicates convergence of the error towards the end of the memorization time, showing that current error settled to $-0.1\%$, irrespective of current level memorized, for compensation times greater than 70 $\mu$s. An unexplained undershoot of the absolute error is also evident in this figure. Array measurement showed that the relative error was negligibly small (less than $0.1\%$), a result in conformity with the expected performance of current memory arrays.

## IV. Conclusion

A current memory circuit with built-in switch feedthrough reduction scheme is presented. The switch feedthrough is reduced by using an error current feedback circuit. The memory cell is capable of operation over a wide range of currents and is measured to have achieved $0.1\%$ absolute error operating even for current levels as low as 10 nA. The relative error of the current memory array was below the measurement limit of the test set up. The circuit is of sufficiently low power and small size to be used for in-pixel background suppression in infrared focal-plane arrays.

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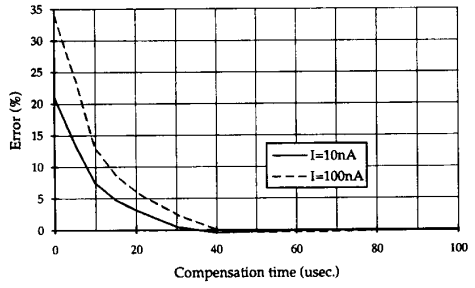
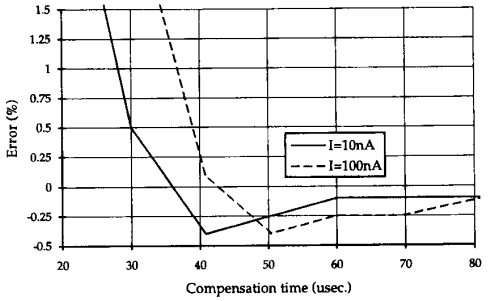



(a)




(b)

Fig. 3. (a) Measured error characteristics of compensated current memory as a function of compensation time for memorizing currents ($I_{\mathrm{mem}}$) of 10 nA and 100 nA. (b) Expanded view ofmeasured error convergence as a function of compensation time(test setup accuracy was $0.1\%$).

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