A Review of Infrared Readout Electronics for Space Science Sensors

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ABSTRACT

A review of infrared readout electronics for space science sensors is presented. General requirements for scientific IR FPA readout are discussed. Specific approaches to the unit cell electronics are described with respect to operation, complexity, noise and other operating parameters. Recent achievements in IR FPA readout electronics are reviewed. Implementation technologies for realization of IR FPA readout electronics are discussed. Future directions for addressing NASA and other scientific users' needs are suggested.

1. INTRODUCTION

Infrared focal-plane array (IR FPA) development has been driven historically by defense applications including IR search and track, forward looking infrared sensors, missile guidance, and other strategic and tactical applications [1,2]. Scientific applications of state-of-the-art infrared focal-plane arrays provide a second important development area for IR FPA technology, but have been funded at a significantly lower level. Consequently, most scientific applications represent a best-fit match between science needs and existing technologies, though some specialized technologies for scientific applications have been developed.

Scientific applications for IR FPAs include astronomy, astrophysics, atmospheric science, geology, planetology and oceanography. Both imaging and spectroscopy sensor systems utilize IR FPAs. The performance requirements for scientific IR FPAs are highly varied with respect to photon background, noise, dynamic range, readout rate, operating temperature, and wavelength.

In general, the IR FPA can be subdivided into the detector array (e.g. HgCdTe, InSb, InGaAs, Si:As IBC, etc.), and the readout electronics. These components are often realized in different materials and mated together using the hybrid IR FPA technology illustrated in fig. 1. The readout electronics, typically realized in silicon CMOS, integrate the photoelectrons generated by the detector,

and then permit multiplexing of individual detector outputs in the voltage mode. The readout electronics thus consist of unit cell electronics that provide the detector bias, photocurrent integration (i.e. charge-to-voltage conversion) and pixel selection, and peripheral electronics for addressing the unit cell electronics, external interfacing and additional output buffering. Monolithic Schottky-barrier IR FPAs with CCD readout [3] are seldom used for scientific applications due to low quantum efficiency (~ 1 - 2 %), and are not discussed in this paper.

For many mature IR FPA detector technologies, it is now the readout electronics that limit scientific performance rather than the detector itself. In this paper, the requirements for scientific IR FPA readout electronics are examined. Circuit approaches for readout electronics are then discussed. Technologies for implementing the readout electronics are reviewed. Selected examples of industry state-of-the-art IR FPA readout ICs are presented. Future directions for scientific sensor readout are suggested.

2. REQUIREMENTS FOR SCIENTIFIC IR FPA

Each scientific application of IR FPAs tends to have its own unique requirement set. In general, the requirements fall into broad categories of charge storage capacity, integration time, noise, dynamic range, readout rate, operating temperature, power dissipation, radiation hardness, detector bias control, array size and pixel pitch. These requirements are often driven by the sensor cutoff wavelength and background photon flux level. As a general rule, readout electronics noise is critically important only for low background photon fluxes where the photon shot noise is small. This is also true for narrow-band spectroscopy applications where the photon flux on an individual detector may be low, despite an overall large background photon flux. Low background SWIR and MWIR IRFPAs for scientific applications usually require a combination of low noise, low power, large format, and possibly high data rates. High background LWIR or longer wavelength scientific applications present the need for detector bias control, large charge capacity, and dynamic range management schemes.

We have attempted to summarize some of the requirements for scientific IR FPAs below, but an exception can be found for almost every situation.

2.1 Charge Storage Capacity

Charge storage capacity is often not an issue in low background scientific applications since the signal levels are small. However, several scientific IRFPAs, such as those to be operated in 20-24 μm band at the ground-based IR telescope at the National Optical Astronomy Observatories (NOAO) [4], or are in use in meteorological satellites [5], require relatively high charge storage capacity of larger than $1x10^7$ electrons/pixel to accommodate bright objects in the field of view, diffuse background signals, or large dark current. To accommodate all the integrated photoelectrons, larger integration capacitances are needed. Since capacitance is directly related to pixel size and the readout electronics technology, alternative background suppression or dynamic range management circuitry are desirable for these applications.

2.2 Integration Time

Typical integration periods in IR FPAs usually range from a few tenths of a millisecond for high background imaging to as long as hundreds of seconds for ultra low background applications. For applications involving long cutoff wavelength IR detectors or high background, the integration time is generally smaller because of finite integrating capacitances and operating voltages. For low background applications, the tendency is to operate the IR FPA with increased integration time. In order to maximize integration time, the saturation frequency and 1/f noise must be reduced. The saturation frequency is defined as the frequency below which the unit cell integrator becomes susceptible to leakage effects, and is dependent on the detector resistance (R_O) and choice of unit cell circuitry. While the simplest unit cells leaves the saturation frequency unchanged, more sophisticated unit cell circuits can actually reduce the saturation frequency by employing feedback.

2.3 Noise

Temporal noise in an IR FPA consists of fundamental photon shot noise that varies as the square root of the number of integrated photoelectrons, detector noise, and noise introduced by the readout electronics. Background limited performance (BLIP), where the temporal noise is dominated by photon shot noise, is typically achieved in high background applications. In low background applications, readout electronics noise must be minimized so that the total IR FPA noise is as close to BLIP as possible. Readout electronics noise is often expressed in terms of input-referred noise electrons, defined as the equivalent number of electrons at the input required to generate the total r.m.s. noise voltage or current at the output. Many future generation scientific applications, such as NASA's MOI and NGST missions require sub-electron read noise. Other highest priority large infrared astronomy projects, such as NASA's Space Infrared Telescope Facility (SIRTF) and NOAO's 8 meter IR telescope for ground-based astronomy, require less than 10 electrons read noise for the detectors operating in SWIR and MWIR bands [1]. At present, 30-50 electrons of input-referred noise is typically obtained in state-of-the-art low background IR FPAs. Lower noise levels have been reported in a few papers discussed below. As a rule of thumb, for a given focal-plane power dissipation, readout noise increases with readout rate.

There are several noise processes introduced by the readout electronics [6]. The 1/f noise (sometimes called excess or flicker noise, and whose power spectrum is given by $1/f^{\alpha}$, $\alpha \sim 1\text{-}2$) in readout unit cell electronics is an important issue for low background applications involving long integration times (greater than 100 milliseconds). For most unit cell circuits used in IR FPAs, the input-referred noise electrons due to the 1/f noise is directly proportional to integration time, making the IR FPA noise significantly larger for longer integration times.

Other temporal noise sources that are of concern for readout electronics are transistor white noise (or channel thermal noise), and reset noise. The effect of transistor white noise can be minimized by reducing the integration capacitances. Reset noise is introduced whenever a switch is used to preset a voltage on a capacitor, and has a voltage r.m.s. value equal to $(kT/C)^{1/2}$, where C is the

capacitor value, and T is the temperature. This so-called kTC noise can be eliminated by correlated double sampling discussed later.

Fixed pattern noise (FPN) is associated with randomly distributed, time-invariant offsets in unit cell circuits (in addition to FPN associated with detector arrays). FPN due to gain non-uniformity and non-linearity can ultimately lead to less-than-BLIP performance [7]. FPN and temporal noise can also be introduced by on-chip clocking signals used to drive the IR FPA readout electronics. Careful layout and separation of digital and analog circuits are required to minimize clocking noise. Low FPN is desirable for scientific sensor readout electronics.

2.4 Dynamic Range

Dynamic range is defined as the ratio of the maximum signal that can be integrated to the r.m.s. noise floor. If this ratio is R, then dynamic range is in decibels (dB) is 20 log R. The required dynamic range is determined by the application, and is typically the ratio of the brightest feature to be observed to the weakest. Users prefer the largest possible dynamic range, but are often limited by either available analog to digital (A/D) converters to under 16 bits (96 dB), by the readout electronics unit cell storage capacitor technology to a lesser value, typically 70-80 dB, or by requirements of linearity, which can be very stringent for scientific applications (e.g. less than 1% integral non-linearity).

2.5 Readout Rate

Readout rate is typically related to the allowed on-focal-plane power dissipation for high readout rates, array format, integration time, and by practical system considerations for low read out rates. For large format ($\geq$ 256x256) staring arrays, simple integrate and readout IR FPAs often require data rates in excess of 100 kpixels/sec. The data rate can also be high for IR FPAs operating at LWIR band, where the integration time can be short. Usually, for simple integrate and readout IR FPAs, readout rates of the order of 10-100 kpixels per second are utilized. For IR FPAs with multiple, non-

destructive sampling, and for high background applications, higher readout rates are required. Typically, scientific IR FPA readout does not exceed 1 Mpixel/sec.

2.6 Operating Temperature

The operating temperature of the IR FPA is typically set by the detector cutoff wavelength. Longer cutoff wavelengths require colder operating temperatures to reduce detector dark current. Detector dark current introduces additional shot noise and increases the dynamic range requirement since the dark current integration is summed with the photosignal and the total charge must be accommodated by the unit cell capacitance. A practical lower bound on the operating temperature of the readout electronics is set by the increase in readout electronics noise and appearance of several device anomalies (such as hysteresis, kinks etc.) at the onset of carrier freezeout. In conventional silicon CMOS, this takes place at temperatures below approximately 50 K. SIRTF and many LWIR scientific sensors require operation at sub-10K temperatures, posing a challenge in the design and realization of low noise readout electronics. In general, users trade operating temperature for IR FPA performance since a lower operating temperature increases system cost.

2.7 Power

Most users would prefer to have no power dissipated on the focal-plane. The allowed power dissipation is determined by the cryogenic cooling apparatus. Typical power levels range from sub-milliwatt to a few tens of milliwatts. Most of this power is dissipated by the final output amplifier stage in the readout electronics since it must drive a large cabling capacitance at a relatively high data rate. (Loral has demonstrated a low power highly linear output buffer amplifier using signal dependent adaptive biasing techniques. The buffer amplifier is reported to have achieved less than 0.1% integral nonlinearity and 900 kHz unity gain frequency while dissipating only 125 μW of power [8]). Additionally, if the readout electronics is operated warmer than the detector, heater power required to maintain the electronics at a warmer temperature must be included as well.

2.8 Radiation Hardness

Two types of radiation hardness are considered. These are total dose hardness and ionizing radiation hardness. Total dose causes threshold voltage shifts and a possible increase in noise ultimately resulting in FPA readout electronics failure. Cosmic rays and other high energy particles and photons result in "salted" images that are a problem for long integration periods in space-based IR FPAs. Since defense applications generally require higher radiation hardness levels than scientific applications, the scientific radiation hardness requirement is not often a limiting one.

2.9 Detector Bias Control

The detector bias during photocurrent integration can affect the dark current, injection efficiency, detector 1/f noise, and responsivity. The dynamic resistance R_O, and device area A product (R_OA) is used to measure the susceptibility of the detector array to dark current and injection efficiency effects. R_OA values typically decrease at longer cutoff wavelengths, causing a reduction in the injection efficiency and introducing non-linearity in the response of IR FPA [9]. To alleviate the problem of reduced injection efficiency and concomitant increased non-linearity, a tight control of detector bias is required during integration. LWIR detectors typically benefit from a constant bias during integration with control of the order of millivolts. For less mature detector technologies, detector 1/f noise can be affected by bias voltage so that constant bias is desired. In photoconductors, including superlattice devices, the bias voltage can affect the responsivity of the detector so that constant bias is also desired for these detectors.

2.10 Array Size and Pitch

As a rule of thumb, scientific users generally prefer high resolution leading to large arrays sizes and small pixels. Array size and pixel pitch is often limited by the hybrid IR FPA technology. This limits detector pitch to approximately 30 microns due to bump bond size, and array size to 512x512 for practical yield considerations. Larger array sizes (1024x1024) are under development and smaller

pixel pitches have been demonstrated in limited quantity. In general, the array size tends to decrease with increasing wavelength of operation mainly due to an absence of large detector array formats in less mature materials used for longer cutoff wavelengths. Larger pixel pitches are desirable for integrating more sophisticated unit cell electronics. Larger pixels are also required at longer wavelengths due to the increase in the diffraction limit with increasing wavelength.

3. CIRCUIT APPROACHES FOR READOUT ELECTRONICS

IR FPAs are operated both in staring mode and scanning mode. With the maturing of an IR detector technology now capable of yielding large format detector arrays, staring mode IR FPAs have become common. However, scanning IR FPAs are often used in several applications such as earth observing satellites in which the sensor is airborne and moving with respect to the earth. We will attempt to describe state-of-the-art performance of both types of arrays used in scientific applications.

Microelectronics feature size has steadily decreased over the past few decades enabling increasingly sophisticated unit cell electronics design. Simple unit cell electronics, such as the source-follower per detector (SFD) approach, continue to be attractive because of the achievable small pixel pitches and low power dissipation. More complex unit cell electronics utilizing high gain amplifiers are gaining in acceptance and provide excellent bias control, linearity and noise performance. A comparison of the performance characteristics of different types of unit cell circuits is shown in table 1. We now attempt to summarize some of the more common approaches to unit cell design.

3.1 Source-Follower Per Detector (SFD)

The source follower per detector unit cell is shown in fig. 2. The unit cell consists of an integration capacitance (C_{int}), a reset transistor (M_{rst}) operated as a switch, the source-follower transistor (M_1), and one or more selection transistors. The integration capacitance may just be the detector capacitance and source-follower input capacitance. If A is the gain of the source-follower (A

< 1), the photoelectron charge-to-voltage conversion is $A(q/C_{int})$ measured in volts per electron. The cell dissipates no active power during integration. The integration capacitance is reset to a reference voltage by pulsing the reset transistor. The photocurrent is then integrated on the capacitance during the integration period. As the signal is integrated, the detector bias changes since the signal is integrated directly on the same node as the detector. For large detector capacitances, the voltage-dependent integration capacitance of the detector can result in non-linear charge-to-voltage conversion limiting the usable dynamic range for scientific applications. Readout is achieved by selecting the cell and reading the output of the source-follower. The cell is susceptible to threshold voltage non-uniformities leading to fixed-pattern noise (FPN), and to kTC noise unless correlated double sampling (CDS) is used. Since SFD consumes very small real estate, SFD readout is often designed to include a CDS circuit in the unit cell.

The main source of white noise in the SFD unit cell is the source-follower transistor itself. The input-referred white noise electrons is given by:

$$\left\rangle N^2 \right\langle_{white} \cong \frac{kT}{q^2}\left[\frac{C_{\text{int}}}{C_L}C_{\text{int}} + \frac{2T_{\text{int}}}{R_o}\right]$$

where C_L is the load capacitance which the source-follower is required to drive, T_{int} is the integration time, and the saturation frequency (f_{sat}) is given by: $f_{sat}=1/(2\pi R_o C_{int})$. Since SFD is used in applications where the detector resistance (R_o) is extremely small, the detector white noise contribution to the readout noise is negligible. If the load capacitance is much larger than the integration capacitance (usually the case, since it is dominated by the multiplexer bus capacitance), low noise performance is possible by allowing C_{int} to be small. However, SFD topology is particularly susceptible to 1/f noise. This is due to the fact that, unlike other unit cell readout circuits, the time period for which the source-follower transistor is turned on during multiplexing is longer than the response time of the source-follower. The effect of this is to enhance the low frequency noise contribution, an effect that has been reported by various authors [10].

SFD has been used as the unit cell for several IRFPAs such as NICMOS3, IR FPAs to be used for MWIR and LWIR SIRTF applications as well as for MWIR ground-based telescopes. Cincinnati

Electronics, Hughes and Rockwell have demonstrated 256x256 SFD readouts [11,12,13]. The Hughes SFD readout is designed to operate both with InSb and Si:As impurity band conductor (IBC) detectors operating at sub 10K over a spectral range of 5-28 μm. Since the Hughes readout is designed for background charge as high as 14,000 electrons (required by SIRTF at 12 μm band), the integration capacitance cannot be made very small. However, the required data rate is low, allowing the use of multiple sampling techniques to reduce broad band noise. The noise performance of the Hughes readout has been shown to be stable at low temperature (< 10K) [14]. The Cincinnati Electronics SFD readout uses an InSb detector and is capable of operation from 4K - 77K, with the noise increasing rapidly below 15 K [15]. A maximum data rate of 400 kHz has been achieved in these IR FPAs.

The Rockwell SFD readout (NICMOS3) has been used in several SWIR and MWIR astronomy applications and operated at 77 K with PV HgCdTe detectors. Rockwell has also operated IR FPAs at 175 K using SWIR InGaAs/InP detectors and a SFD unit cell [16]. Work is underway in Rockwell to increase the NICMOS3 array size to 512x512 with a 25 μm pitch and a predicted read noise of less than 4 electrons [7]. NICMOS3 uses an off-chip CDS to reduce the reset noise and the 1/f noise [17]. The relevant operating characteristics of SFD readouts built by Cincinnati Electronics, Hughes and Rockwell are summarized in table 2.

3.2 Direct Injection (DI)

A typical direct injection unit cell is shown in fig. 3. The unit cell consists of an integration capacitor (C_{int}), an injection transistor (M_i), a reset transistor (M_{rst}), and an output selection transistor. The cell is operated by first resetting the integration capacitor by pulsing the reset transistor. Photocurrent from detector is then integrated on the integration capacitor through the injection transistor. Since the photocurrent is input through the injection transistor, the DI scheme yields somewhat better bias control during integration compared to SFD. Following integration, the capacitor is selected and its integrated charge dumped on to the column selection line. The photoelectron charge-to-voltage conversion is simply q/C_{int}, measured in volts per electron. The cell

dissipates no active power during integration as in the case of the SFD. An important performance parameter in this circuit is injection efficiency (η). Injection efficiency measures the fraction of the detector photocurrent that is coupled to the readout circuit and is defined as the ratio of photocurrent integrated on C_{int} to the total detector photocurrent. Low η is caused by low detector impedance (R_o), providing a parasitic path for current flow. From the definition of the injection efficiency, it can be expressed as:

$$\eta = \frac{g_{mi}R_o}{1 + g_{mi}R_o}$$

where g_{mi} is the transconductance of the injection transistor and R_o is the small signal resistance of the detector. Since the magnitude of the photocurrent is small, the injection transistor is biased in weak inversion, making its g_m relatively small. For detectors with longer cutoff wavelengths, R_o reduces drastically (R_o can be as low 1 MΩ for a HgCdTe PV detector with cutoff wavelength of 12 μm), reducing the injection efficiency as well as making the injection efficiency photocurrent dependent. As a result, this circuit is less desirable for unit cell readout in IR detection in LWIR or beyond. Further, the injection efficiency is a function of frequency with a relatively small cutoff frequency, thereby limiting the circuit's ability for high frequency (small integration time) operation [3].

One of the problems of using injection-transistor-based readout circuits is that their performance degrades severely in applications with low backgrounds. The transconductance of the injection transistor decreases in proportion with the background photocurrent, causing a degradation of injection efficiency, and making the injection transistor noise substantially large. The problem is further exacerbated by the increased demands on the d.c. bias stability of the injection transistor. Therefore, a DI circuit is not preferred for operation in ultra-low background applications, as well as with detectors having longer cutoff wavelengths (exhibiting small detector resistance).

The maximum integration time is limited by the saturation frequency (f_{sat}) related to the integration capacitance (C_{int}) and resistance (R_o) and is given by: $f_{sat}=1/(2\pi C_{int}R_oA_{vm})$, where $A_{vm}=g_{mi}/g_{dsi}$, and g_{dsi} is the output conductance of the injection transistor. The saturation frequency is lower than in SFD due to a certain degree of bias control offered by the injection transistor.

Compared to SFD, this cell is less susceptible to FPN, but still suffers from reset noise unless external double correlated sampling is used. Ignoring the reset noise, it can be shown that the input-referred noise electrons is given by:

$$\left\rangle N^2 \right\langle_{white} = 2\frac{kT}{q^2}\left(\frac{T_{\text{int}}}{R_o}\right)\left[1+\frac{1}{g_{mi}R_o}\right]$$

$$\left\rangle N^2 \right\langle_{1/f} = \frac{2T_{\text{int}}^2}{q^2}\left[S_{\text{fd}}+\left(\frac{1}{g_m R_o}\right)^2 S_{fm}\right] ln\left(\frac{1}{\pi T_{\text{int}} f_{sat}}\right)$$

where S_{fd} and S_{fm} are the respective detector and injection transistor current 1/f noise power spectral densities at 1 Hz. Larger values of the integration capacitance (C_{int}) results in a larger input-referred noise for a given output noise power, while the output noise power itself is inversely related to C_{int} (since a larger C_{int} increases the noise bandwidth), thereby making the noise independent of C_{int}, as indicated by the equation shown above.

During multiplexing, the charge integrated on C_{int} is shared with the bus capacitance. Therefore, DI circuits are usually designed with large integration capacitors to prevent degradation of signal due to charge sharing, at the cost of reduced charge sensitivity of the input circuit. Further, the presence of a large bus capacitance makes input-referred downstream noise (such as multiplexer noise, output driver noise, and clocking noise) large, since input-referred noise electrons due to downstream noise is given by:

$$\left\rangle N^2 \right\langle_{white} = \frac{v_{nout}^2}{q^2}\left(C_{\text{int}}+C_{bus}\right)^2$$

where v_{nout} is the r.m.s. downstream voltage noise, and C_{bus} is the bus capacitance. For a typical r.m.s. downstream noise of 25 μvolts, fig. 8 indicates that the downstream noise is dominant in DI, especially for smaller integration capacitance sizes, limiting the minimum noise floor to a higher value compared to SFD or CTIA.

DI circuits are usually not used for scientific applications since a slightly modified circuit, called buffered direct injection circuit, exhibits much improved injection efficiency, and higher frequency operation capability.

3.3 Buffered Direct Injection (BDI)

Buffered direct injection [18] is similar to direct injection except that inverting gain is provided between the detector and the injection transistor gate, as shown in fig. 4. The gain can achieved, for example, by using a simple inverter circuit. The inverted gain provides feedback to yield better control over the detector bias at different photocurrent levels. As the photocurrent increases, the input impedance of the injection transistor is decreased to maintain constant detector bias. The photoelectron charge-to-voltage conversion is still q/C_{int} measured in volts per electron. The cell now dissipates active power in the amplifier during integration. The injection efficiency (η) is improved compared to the direct injection case to:

$$\eta = \frac{g_{mi}(1+A_{vo})R_o}{1+g_{mi}(1+A_{vo})R_o}$$

where A_{vo} is the low frequency gain of the inverting amplifier. Further, compared to a DI circuit with the same R_o, C_{int} and C_d, the cutoff frequency of the injection efficiency in BDI increases by $(1+A_{vo})$, allowing much higher frequency operation of the unit cell.

Apart from an improvement in the injection efficiency, the inverting gain also helps to reduce the saturation frequency compared with the DI circuit, thereby allowing longer integration times. The saturation frequency of a BDI circuit is given by: $f_{sat}=1/(2\pi A_{vm}A_{vo}R_oC_{int})$, and is much smaller compared to the saturation frequency of DI and SFD. In BDI, improved injection efficiency, reduced saturation frequency and tighter bias control is achieved at the cost of increased power dissipation and added unit cell complexity. However, the inverting amplifier can be designed to operate at sufficiently low power, since it is required to drive only a small capacitance (approximately the gate capacitance of the injection transistor).

In spite of the increased injection efficiency achieved by BDI, it shares the same limitation with DI in terms of its use in ultra low background applications, since the injection transistor has to operate at extremely low drain currents. The input-referred noise electrons of a BDI circuit (neglecting downstream noise and reset noise) is given by:

$$\rangle N^2 \langle_{white} = 2\frac{kT}{q^2}\left(\frac{T_{\text{int}}}{R_o}\right)\left[1+\frac{1}{g_{mi}R_oA_{vo}^2}+\frac{1}{g_{ma}R_o}\right]$$

$$\rangle N^2 \langle_{1/f} = \frac{2T_{\text{int}}^2}{q^2}\left[S_{\text{fd}}+S_{\text{fm}}\left(\frac{1}{g_{mi}R_oA_{vo}}\right)^2+\frac{S_{fa}}{R_o^2}\right]ln\left(\frac{1}{\pi f_{sat}T_{\text{int}}}\right)$$

where g_{ma} is the transconductance of the amplifier, and S_{fa} is the amplifier input-referred 1/f noise power spectral density at 1 Hz. Due to the tighter bias control achieved by feedback in BDI, BDI unit cell white noise is smaller than that of DI. However, typically, similar to a DI circuit, the input-referred noise is dominated by bus capacitance. BDI is most suited for high background applications, that require larger charge storage capacity, larger integration bandwidth, and moderate readout noise.

Westinghouse has built scanning MWIR IR FPA for high background applications, using wide bandwidth BDI unit cell coupled to high dynamic range CCD with an additional blooming control circuit [2]. The unit cell pitch is 50 μm, and the array consists of 92 column and 30 TDI stages. For 312.5 μsec. integration time, the unit cell read noise has been measured to be less than 80 electrons. The maximum charge storage capacity of each unit cell is less than $1x10^5$ electrons.

3.4 Gate Modulation Input (GMI)

A gate modulation input circuit [19,20] is shown in fig. 5. A load device, typically a load transistor (M_i), is placed in series with the detector. The bias voltage developed across the load is used to modulate the gate voltage of an output transistor (M_o). The output transistor and the load transistor are usually connected in current mirror-like configuration, with the respective source voltages V_{ss} and V_{bias} adjusted for setting the current gain. The input transistor discharges a capacitor previously reset to a reference level. The photoelectron charge-to-voltage conversion in volts per electron is given by $\frac{q}{C_{\text{int}}}\frac{g_{mo}R_o}{1+g_{mi}R_o}$, where g_{mo} is the transconductance of the output transistor, and g_{mi} is the transconductance of the load transistor. Since the detector current flowing through the load transistor is much smaller than that in the output transistor, GMI circuit yields a large charge-to-voltage conversion gain compared to DI and BDI circuits. The increased current gain leads to higher charge

detection sensitivity and reduced input-referred noise levels. The input-referred noise electrons for GMI is given by:

$$\left\rangle N^2 \right\langle_{white} = 2\frac{kT}{q^2}\left[\frac{T_{\text{int}}\left(1+g_{mi}R_o\right)}{R_o}\right]\left[\frac{1+g_{mi}R_o}{g_{mo}R_o}\right]\left[1+A_{vo}^2\frac{1+g_{mi}R_o}{g_{mo}R_o}\left(\frac{C_{\text{int}}}{C_d}\right)^2\right]$$

$$\left\rangle N^2 \right\langle_{1/f} = \frac{2T_{\text{int}}^2}{q^2}\left(\frac{1+g_{mi}R_o}{g_{mo}R_o}\right)^2\left[\left(S_{\text{fd}}+S_{fm}\right)A_{vo}^2\left(\frac{C_{\text{int}}}{C_d}\right)^2+S_{fo}\right]ln\left(\frac{1}{\pi T_{\text{int}}f_{sat}}\right)$$

where S_{fo} is the output transistor drain current flicker noise power spectral density at 1 Hz, $A_{vo}=g_{mo}/g_{dso}$, and $f_{sat}=(1+g_{mi}R_o)/(2\pi R_oC_d)$. The saturation frequency of GMI is higher than that achieved with DI and BDI for a given C_d and R_o, thereby limiting the integration time. GMI can potentially yield very low input-referred noise due to the intrinsic current gain that can easily be as high as 10^4 in medium to low background applications. Because of the large unit cell current gain, GMI can operate with a larger integration capacitance compared to DI and BDI, and still obtain low noise performance and high charge sensitivity. Fig. 8, which illustrates the dependence of the input-referred noise electrons on the integration capacitance, indicates that GMI has the best white noise performance for a wide range of integration capacitance size (1 fF - 1 pF). The noise floor is limited by the detector noise to about 3 electrons r.m.s., for an integration time of 10 msec. and detector dynamic resistance of $10^{14}\ \Omega$.

The GMI is susceptible to FPN due to threshold voltage variations in the input transistor causing the current gain to vary from one cell to another. Further, for low noise operation of GMI, source biases of both the load transistor and the input transistor require excellent bias control within 1 p.p.m. (to be provided externally) [21]. In spite of these stringent operating requirements, excellent noise performance has been demonstrated by Rockwell using a 128x128 format GMI readout mated to a InGaAs detector with 1.7 μm cutoff wavelength under low background [10]. The current gain was greater than 47000 and input-referred noise was measured at 4.8 electrons for a 22 msec. integration time and 40 fF of detector capacitance.

One unique feature of GMI is that the current gain self adjusts depending upon the background flux, since the current gain is approximately proportional to the detector current level. The self adjusting gain feature can be used for background pedestal suppression leading to higher dynamic ranges, and has been used by Rockwell to obtain dynamic range greater than 200 dB, albeit at the cost of increased non-linearity and fixed pattern noise [22].

3.5 Cascode Amplifier Per Detector (CAD)

Like the gate modulation input circuit, the cascode unit cell amplifier provides for increased photoelectron charge-to-voltage conversion, thus raising the unit cell output signal above a system noise floor, and making it much easier to avoid system noise degradation from subsequent stages. Conversely, for a given downstream noise level, integration time is smaller than SFD, yielding better bias control, required for longer cutoff wavelength detectors. The cascode unit cell amplifier is shown in fig. 6. The unit cell consists of an integration capacitance (C_{int}), a reset transistor (M_{rst}) operated as a switch, the cascode amplifier transistors (M_i, M_{casc}, M_L), and one or more selection transistors. The cascode amplifier is an inverter with a cascode transistor (M_{casc}) inserted to reduce the Miller capacitance and keep the input capacitance low (required to maintain high detection sensitivity). The load of the cascode inverting amplifier consists of a transistor (M_L). If silicon CMOS is unavailable, M_L is of the same type as M_i, so that the voltage gain, A, of the cascode amplifier circuit is given by the ratio of the input transconductance (g_{mi}) to the load transconductance (g_{mL}) and is expressed as:

$$A = \frac{g_{mi}}{g_{mL}} = \frac{\sqrt{\left(\frac{W}{L}\right)_i}}{\sqrt{\left(\frac{W}{L}\right)_L}}$$

where W is the gate width and L is the gate length. The voltage gain is relatively small (limited to about 10) since it is dependent on the ratio of the transconductances, but is independent of threshold voltage and bias current variations. Apart from providing voltage gain, SFD and cascode amplifier unit cell are remarkably similar in performance, and the comments made earlier about the performance of SFD holds for the cascode amplifier unit cell as well.

Amber Engineering has constructed and fabricated a 1x32 cascode readout and multiplexer (AE-152) for use in SIRTF far-infrared (50-120 μm) instruments with Ge:Ga photoconductor detector arrays [23]. In order to cancel the offset introduced by threshold shifts in the unit cell, the unit cell also includes a DC restore circuit with a 20 pF coupling capacitance from the cascode unit cell to the unit cell source follower. Typical power dissipation is low, since each unit cell conducts current only 1/32 of the frame time, and is measured to be 156 μW for all the 32 channels. Operated above 20 K, AE-152 has a read noise of 10 electrons for a large integration capacitance of 2.2 pF. The low noise performance was achieved by constructing the signal with multiple slope sampling technique using 4 samples per channel, and 10 sec. long integration times. Since only 32 unit cells occupy the focal-plane, the transistors are designed with large dimensions, thereby reducing 1/f noise. However, the heater power is an additional heat burden, since AE-152 operates at 20 K, while the photoconductor detector arrays requires to be operated at less than 2 K [24].

3.6 Capacitive Transimpedance Amplifier (CTIA)

The capacitive transimpedance amplifier is shown in fig. 7. The CTIA consists of an inverting amplifier with a gain of A, an integration capacitance (C_{int}) placed in a feedback loop, a reset transistor (M_{rst}) in parallel with the integration capacitance, and one or more selection switches. The inverting amplifier is usually a cascode amplifier implemented in a single input or differential input topology. While a single CMOS inverting amplifier is attractive because of real estate reasons, the differential amplifier topology offers superior power supply noise rejection and bandwidth control, which is important for power and noise optimization.

At the outset of photocurrent integration, the integration capacitance is reset to a reference voltage (generated by the amplifier) by pulsing the reset transistor. During the integration mode of operation, the photocurrent is integrated almost solely on the integration capacitance, while the feedback and the large gain of the amplifier holds the input at the virtual ground, thereby almost entirely preventing any charge integration on the detector capacitance. Since the input is pinned to the

virtual ground, a tight control on the detector bias is maintained, facilitating its use with detectors having relatively small R_o (detectors with longer cutoff wavelengths). Since the output of the unit cell is connected to a low impedance node (the amplifier output), the integration capacitance of CTIA, unlike that of DI, BDI and GMI, can be made extremely small, yielding excellent low noise performance. However, the high detection sensitivity and low noise is achieved at the cost of increased power dissipation and unit cell pitch. The photoelectron charge-to-voltage conversion is $\frac{q}{C_{int} + \frac{C_{int}+C_d}{A_{vo}}}$ measured in volts per electron, with A_{vo} being the amplifier gain. As a result of the feedback, the effective saturation frequency of CTIA is decreased compared to that of SFD, and is given by:

$$f_{sat} = \frac{1}{2\pi A_{vo} R_o \left(C_{int} + \frac{C_{int}+C_d}{A_{vo}} \right)}$$

CTIA is used for low noise, large bandwidth applications since the smallest integration time is limited by the unity gain frequency of the amplifier. However, there is a trade-off between operating with a small integration time and focal-plane power dissipation.

Ignoring the reset noise and the downstream noise (small for a low value of integration capacitance), the input-referred noise electrons of CTIA is given by:

$$\left\rangle N^2 \right\langle_{white} = \frac{kT}{q^2} \left[\left(\frac{2T_{int}}{R_o} \right) + \left(\frac{C_{int} + C_d}{C_L + \frac{C_{int} C_d}{C_{int} + C_d}} \right) \left(C_{int} + \frac{C_{int} + C_d}{A_{vo}} \right) \right]$$

$$\left\rangle N^2 \right\langle_{1/f} = \frac{2T_{int}^2}{q^2} \left[S_{fd} ln \left(\frac{1}{\pi f_{sat} T_{int}} \right) + \left(\frac{f_s}{f_a} \right)^2 S_{fa} \left(\frac{C_{int} + \frac{C_{int}+C_d}{A_{vo}}}{C_L + \frac{C_{int} C_d}{C_{int} + C_d}} \right)^2 ln \left(\frac{11.8 f_a}{f_s} \right) \right]$$

where S_{fa} is the amplifier 1/f noise drain current power spectral density at 1 Hz, f_a is the cutoff frequency of the amplifier, and typically limits the shortest integration time. CTIA input-referred noise is independent of amplifier gain, provided the gain is large. The input-referred noise can be made small by making the integration capacitance small, while increasing the load capacitance at the same time to decrease the amplifier noise by reducing the noise bandwidth. Fig. 8 indicates that CTIA white noise performance is slightly inferior to that of GMI for a given capacitance. However, GMI integration capacitance cannot be made very small in practice because of the limitations imposed by

bus charge sharing, while CTIA integration capacitance can be made as small as 1 fF, leading to ultra low noise performance.

CTIA unit cells have been applied in a wide variety of circumstances and both in staring and in scanning modes. In early efforts, 10 electron read noise was reported by Rockwell and Amber using a CTIA unit cell that was operated at 92 K [25]. Honeywell reported obtaining 70 electron read noise using CTIA unit cell and integration times as high as 100 seconds [26] for SWIR applications. With further advancements in IR detector technology, some of the lowest noise performance have been achieved with CTIA as the readout unit cell, especially by incorporating a unit cell CDS circuit.

Rockwell has demonstrated a SWIR IR FPA with an ultra low noise CTIA-CDS unit cell operated at very low backgrounds (< 10^6 photons/cm^2/sec) in 128^2 format [10]. The CTIA was biased at subthreshold in order to reduce power. With a 4 fF integration capacitance, 23 fF detector capacitance, 1.5 pF load capacitance, and a nominal integration time of 20 msec., the read noise was measured to be 3.4 electrons. Rockwell has also demonstrated a high performance SWIR 10x132 scanning IR FPA with a "sidecar" architecture. The unit cell consists of CTIA and CDS, and the "sidecar" TDI stage is implemented with a (10x3)x132 CCD. The unit cell dimensions are 25x75 μm^2. A novel feature of the CTIA is that no explicit integration capacitance was added to the unit cell. The integration capacitance consisted of the parasitic capacitance, contributed by the gate to drain of capacitance of the input FET and was smaller than 1 fF, resulting in a high CTIA charge sensitivity of 200 μV/electron, and enhanced low noise performance. Because of the increased charge sensitivity, the downstream noise (e.g. in the CCD) was insignificant. The readout noise was measured to be 9.4 electrons per TDI stage with 10 transfers, which translate to input-referred noise of less than 3 electrons per CTIA unit cell [27].

Cincinnati Electronics is in the process of delivering an IR FPA for low background Visible and Infrared Mapping Spectrometer (VIMS). The IR FPA uses CTIA unit cell and is expected to achieve < 250 electrons read noise with CDS and for integration times ranging between 1 msec. to 10 sec. [28]

Santa Barbara Research Center (SBRC) has demonstrated MWIR scanning IR FPAs were operated with less than 100 electron read noise with 300 μsec. integration time and under relatively high backgrounds of 10^{12} photons/cm^2/sec [29]. Recently, it has also demonstrated a high performance scanning IR FPA for MWIR earth resource monitoring and spectroscopic chemical analysis [30]. The readout was designed for high speed operation (line rate < 24 kHz, data rate 3.2 MHz), large dynamic range, high sensitivity, and excellent stability (< 0.5% drift nonuniformity). The unit cell consists of 32x134 CTIA and CDS unit cells coupled to InSb detectors. The output of a CTIA-CDS is connected to column amplifier than drives a bank of "sidecar" TDI stages consisting of CCDs. Each column consists of 26 high sensitivity (small integration capacitance) CTIAs and 6 low sensitivity CTIAs. This allows dynamic range management to greater than 90 dB. The CTIA-CDS was laid out in a 50 μm pitch. For an integration time of 167 μsec., the input-referred noise was measured at 34.5 electrons per TDI channel (consisting of 26 high gain stages), translating to 6.77 input-referred electrons for each CTIA-CDS unit cell. The input-referred noise was even lower for smaller integration times, reaching as low as 1.88 electrons for the smallest integration time of 42 μsec. SBRC LWIR low background, high speed, high sensitivity IR FPA was built as linear array with 260 elements and 25 μ m pitch [31]. Using a 30 fF integration capacitance, and for an integration time of 42 μsec., less than 120 electrons input-referred noise was obtained at 65K operating temperature. The performance characteristics of a few selected CTIA readouts are presented in table 2.

4. NOISE REDUCTION STRATEGIES

In this section, we present various noise reduction schemes that are used with IR FPAs. Most of the noise reduction schemes are complicated in implementation, and are usually carried out digitally off-chip.

4.1 Correlated Double Sampling (CDS)

Correlated double sampling virtually eliminates kTC reset noise by measuring the output after the reset, and the output with the integrated signal, and computing the difference between the two [32], as shown schematically in fig. 9a. CDS can be implemented in the unit cell as a clamp-and-sample circuit. A clamp-and-sample circuit uses an a.c. coupled capacitor in the unit cell to remove the amplifier offset (including reset noise) level. CDS is also implemented off-chip by collecting two digital samples from the sense node, one representing the reset level and another, the level after the photocharges have been integrated. Since the signal is generated by computing the difference of two data samples, CDS can also reduce 1/f noise and FPN, albeit at the cost of increased white noise contribution.

The performance of the CDS circuit depends on the product of the correlation time (τ_c), defined as the time interval between the collection of two data samples, and the output amplifier cut-off frequency (f_o) [33]. For a large $\lambda=\tau_c f_o$, cross-talk and reset noise is reduced but the white noise and 1/f noise is increased. Since the correlation time is the same as the pixel integration time for most IR FPAs, the CDS scheme used in IR FPAs is constrained to operate with large λ values in low background applications. Therefore, the 1/f noise reduction potential of CDS in IR FPAs is somewhat limited, especially when the integration time is long, while the data rate is high.

A modified CDS is often used to improve the 1/f noise reduction characteristics of a CDS circuit used in low background IR FPAs. In the modified CDS circuit [34], two sets of closely spaced double samples are collected as shown in fig. 9b. Prior to photocurrent integration, the reset noise and the offset is measured by computing the difference between the reset level before and after the reset transistor is shut off. The signal, corrupted by the reset noise and offset, is measured at the end of the integration period by computing the difference between the data level before and after the unit cell is reset. Since the resultant correlation times are much smaller, superior 1/f reduction is achieved, while the white noise approximately doubles compared to simple integrate and read approach, and the power dissipation increases due to increased data rate. The modified CDS has been used by Cincinnati

Electronics in their 256x256 InSb IR FPA operating between 4 -77 K, in order to reduce the excess noise [9].

4.2 Multiple Correlated Sample Read (MCS)

The analog multiplexer in the IR FPA readout can sometimes become a major contributor of noise, resulting from spurious capacitive coupling. The multiplexer noise which is also dependent on the clocking scheme, can be as high as 400 noise electrons even for a small 58x62 array [35]. For reduction of this clocking noise, multiple correlated sampling (MCS) technique has been suggested. In the MCS technique (illustrated schematically in fig. 9c), the signal is non destructively sampled multiple times both at the beginning and at the end of the integration time. If a total of 2N samples are collected, the signal to noise ratio improvement is approximately square root of N. For a 200 sample MCS, 10 electron read noise has been achieved [24]. One obvious disadvantage of this method is the vastly increased data rate, limiting its use for large format, high data rate IR FPAs.

4.3 Non-Uniformity Calibration (NUC)

IR FPAs, like most other scientific sensors, require pixel by pixel calibration to eliminate the effects of both detector and readout electronics non-uniformities. For example, both signal offset and gain vary from pixel to pixel. Unlike many DoD applications where one or two-point non-uniformity correction is performed in real-time, non-uniformity calibration in scientific applications is often performed with many data points both on the ground and sometimes in flight. The calibration is applied to the sensor data on the ground to minimize on-board data processing requirements. Future missions may benefit from on-board non-uniformity calibration to enhance the compressibility of the data and to enable on-board feature extraction.

4.4 Chopper-Stabilized Input Circuits (CSI)

Chopper-stabilized unit cell circuits offer two significant improvements over conventional linear amplifiers: effects of MOSFET threshold mismatch is vastly reduced and 1/f noise performance

of the amplifier is improved. The chopper stabilized unit cell consists of a modulator that translates the input signal to higher frequency where the 1/f noise is low. Since the carrier amplifier is a.c. coupled, d.c. offset components are removed. The output of the unit cell is then downconverted in frequency by using synchronous demodulation. Amber Engineering has demonstrated operation of a chopper-stabilized focal-plane readout in a 100 μm pitch, dissipating < 0.3 μW/cell power, and exhibiting ten times improvement in noise performance [36].

5. TECHNOLOGIES FOR READOUT ELECTRONICS

In this section, the choice of readout electronics implementation technology is discussed. In general, one would prefer to use silicon CMOS for all applications, but concerns of operating temperature, noise, thermal expansion effects, speed and radiation hardness cause the consideration of alternative technologies such as GaAs.

The major problem with using silicon CMOS for scientific IR FPAs is that the FPA operating temperature tends to be lower than 77 K, making carrier freezeout an issue. In a semiconductor, carriers (e.g., electrons) are thermally ionized from a donor impurity atom. The probability of being ionized and participating in the conduction process is exponentially related to the temperature, being essentially unity at room temperature. In silicon below 150 K, the probability begins to drop rapidly, depending on the donor species and its concentration. The emission and recapture of carriers by the donors is a time dependent process, leading to a time dependent conductivity that appears as noise. By increasing the donor concentration (using more heavily doped layers), the temperature at which the noise grows to an unacceptable level can be decreased. (The freezeout can be eliminated by doping with high enough donor concentration such that the semiconductor becomes semi-metallic, but electrical control of such highly doped semiconductor layers is often difficult). The resultant device technology is no longer commercial CMOS, and is referred to as cryogenic CMOS.

Other semiconductor material and donor combinations can allow operation at substantially lower temperatures before freezeout related anomalies become a concern. These include germanium

(Ge) and gallium arsenide (GaAs). Unfortunately, noise in these materials is dominated by other effects, such as defect-trapping. Technologies involving these materials are less mature than present day silicon technology, and much less total effort worldwide is applied to perfecting Ge or GaAs compared to silicon. Thus, while physics may favor GaAs for reducing freezeout effects, the momentum associated with silicon technology makes for a competitive relationship at temperatures below 10 K.

For scientific IR FPAs, both large signal performance that is free from kinks and hysteresis, and small signal performance that is free from excess noise (e.g., 1/f noise) is required. Transistor 1/f noise is generally inversely related to device area, so that large transistors have better noise performance than small transistors, leading to large pixel pitches for low noise performance. Scientific IR FPAs with long integration times require low noise at low frequencies, exacerbating the effect of 1/f noise. A typical scientific readout electronics input transistor is required to have an input-referred noise less than 100 $nV/Hz^{1/2}$ at 1 Hz.

5.1 Silicon CMOS

The major technology used for the readout of scientific infrared focal-plane arrays is silicon CMOS. CMOS is a well understood device technology. Many computer-aided design tools have been developed to support digital and analog CMOS integrated circuit design for room temperature (300 K) operation. Operation down to 77 K has also been explored using conventional CMOS processes. Higher speed, lower leakage currents and higher subthreshold slope are the major benefits of operating CMOS at 77 K. Thus, there has been recent commercial interest in operating CMOS at 77 K, irrespective of any need to operate an IR FPA at low temperature.

The smaller the design rule, the more circuits can be implemented within a given pixel pitch, or conversely, the smaller the pixel pitch can be for a given circuit design. Several CMOS foundries offer processes at design rules down to approximately 0.8 μm, though many FPA readout circuits are designed with 2 μm or 1.2 μm CMOS. One reason is that radiation-hard CMOS circuit technology

tends to lag behind mainstream CMOS and generally has larger design rules. Another reason is that CMOS foundries catering to the needs of the aerospace community have a lower production volume than commercial foundries, and are thus undercapitalized and understaffed for state-of-the-art fabrication. It should be noted that a 512x512 readout electronics IC with 40 μm pitch utilizing CTIA circuits is over 2 cm x 2 cm in size, and contains over 2 million transistors and thus requires VLSI fabrication capability.

At temperatures lower than 77 K, carrier freeze out becomes increasingly important. A transition in process technology from conventional CMOS to cryogenic CMOS must be made for temperatures below approximately 50 K. Conventional CMOS begins to exhibit some excess noise at these temperatures, but more importantly, hysteretic behavior and kinks dominate in large signal performance. Improved processes are required to overcome these limitations for operation at lower temperatures.

5.2 Cryogenic CMOS

Cryogenic CMOS refers to a silicon CMOS technology that is optimized for low temperature operation. Only one or two foundries offer a cryogenic CMOS process. The major changes involve a combination of higher doped substrates and wells, and a lower doped epitaxial layer. An excellent review of cryogenic CMOS was given recently by TRW [37]. Unfortunately, TRW recently dropped its cryogenic CMOS fabrication foundry. Hughes Carlsbad Technology Center (HTC) is presently developing a low noise cryogenic CMOS foundry service that promises to restore a national cryogenic CMOS capability. Orbit Semiconductor has also indicated an interest in providing this service.

Reasonable results have been reported for cryogenic CMOS operating down to 20 K. In the 20 K to 10 K range, some good results have been sporadically reported. Below 10 K, noise reduction is an intense area of research. HTC reports achieving 70 $nV/Hz^{1/2}$ at 10 Hz and 5 K [12], presently believed to be a silicon record. Exploration of this technology for SIRTF application is underway.

5.3 Germanium

Germanium technology predates silicon. The lack of a stable, native oxide (such as that afforded by silicon as SiO_2) has relegated discrete germanium devices to niche markets. Germanium JFETs built more than a decade ago by Texas Instruments, and no longer being produced, are desired for many discrete low noise readout circuit designs for the 50 K - 80 K temperature range. Noise as low as 60 nV/Hz$^{1/2}$ at 10 Hz for 4 K operation was reported by Ames [38]. Some limited activity at SBRC and JPL has transpired, but a modern Ge JFET technology remains unavailable.

5.4 GaAs

GaAs is interesting as a potential FPA readout technology for three reasons. First, the thermal expansion coefficient of GaAs is a much better match to that of HgCdTe, compared to silicon, potentially permitting large hybrid FPAs to be reliably fabricated. Second, GaAs is a much more radiation-hard technology than silicon. Third, n-type GaAs devices have a donor level closer to the conduction band edge than silicon, making GaAs devices more immune to freezeout effects at 4 K. There are several GaAs technologies that can be considered for readout application. These include metal-semiconductor field effect transistors (MESFETs), junction FETs (JFETs), and two-dimensional electron gas (2DEG) devices, also known as high electron mobility transistors (HEMTs), or heterostructure FETs (HFETs). Due to the relative immaturity of GaAs, the full potential of GaAs readout is impeded by a lack of demonstration of VLSI circuits, and/or a lack of engineers familiar with the details GaAs circuit design. Here, the potential of GaAs for low temperature readout is examined.

Commercially available GaAs MESFETs have been extensively measured by Kirschman [39,40]. Noise levels of approximately 50 nV/Hz$^{1/2}$ at 10 Hz for 4 K operation were reported. A 2x64 multiplexer was demonstrated by Rockwell [41]. Measured noise at 78 K was approximately 1 μV/Hz$^{1/2}$ at 10 Hz. The major problems facing MESFET readout electronics are gate leakage current and power dissipation in integrated circuits. Unlike a silicon device that has a large oxide barrier to gate leakage, GaAs MESFETs have a 0.8 eV barrier that permits some measurable currents even at

cryogenic temperatures. However, improvement of the leakage current to levels acceptable for practical application is considered feasible. The lack of a true complementary circuit technology makes power levels in the readout circuits an issue for scientific applications though complementary enhancement/depletion mode MESFET circuits are being explored for readout application [42].

GaAs n-JFETs were fabricated by Aerojet and measured by Ames [43]. These devices were reported to have a very low noise level of 10 $nV/Hz^{1/2}$ at 10 Hz for 4 K operation, comparable to silicon JFETs at 55K. While potentially an excellent front end for silicon readout electronics or GaAs CHFET electronics (see below), GaAs n-JFET technology by itself suffers the same high power dissipation problem as GaAs MESFETs. However, the gate leakage current of a JFET technology is expected to be low enough to be of practical use in low background IR applications since the gate barrier is greater than 1 eV.

GaAs complementary heterostructure FET (CHFET) technology is a demonstrated LSI circuit technology for high speed digital circuits at 77 K and above [44]. JPL has explored this technology for possible application to scientific IR FPA readout [45,46]. The CHFET technology has noise levels of the order of 2 $\mu V/Hz^{1/2}$ at 10 Hz for 4 K operation -- a value too large to be of practical use in low background applications. The CHFET technology also has a gate leakage current that is considered still too high for use in the same application.

5.5 Other Technologies

Other technologies that have been explored for readout of IR FPAs include silicon bipolar devices [47], InP HBT devices [48] and superconducting circuits [49,50]. The bipolar devices have low input impedance and higher noise. The superconducting circuits are of interest to low temperature, low background applications due to their low power and noise, and intrinsic compatibility with low temperature IR detector operation. However, the extremely low input impedance (intrinsic to superconducting circuits) makes it difficult to interface these circuits with semiconductor detectors.

6. FUTURE DIRECTIONS

Scientific IR FPA readout electronics will continue to benefit from continued DoD investment in IR FPAs. However, the technology is rapidly reaching a branch point. DoD IR FPAs are clustered in the atmospheric window wavelengths (3-5 μm, 8-12 μm), and are aimed at convenient operating conditions. These include 77-80 K operating temperature and NTSC video formats such as 640x480 for tactical applications. Some work continues in the longer wavelength, 20 K LWIR detector area for space applications. However, scientific sensors require increasingly lower noise floors, with sub-electron read noise desired by the turn of the century. The need for large formats with long integration times increases the disparity between DoD-funded development and scientific requirements. To some extent, DoD is becoming more interested in infrared spectroscopy as a surveillance and reconnaissance technique, so that some leverage might be expected in the future for the development of scientific infrared imaging spectroscopy instruments. These will be low noise, high data bandwidth instruments.

NASA's current needs in sensor electronics were identified during the Astrotech '21 Workshop series [51]. These needs include sub-electron read noise, cryogenic 4 K readout electronics for SIRTF, low noise discrete transistors for 80K, advanced packaging techniques (e.g. thermal compartmentalization), advanced interfaces such as analog-to-digital converters and optical links, and advanced architectures such as event-driven readout. Some technical areas that are emerging as future directions are described briefly below.

6.1 On-Chip A/D Conversion

Analog-to-digital (A/D) conversion circuit technology has progressed rapidly in the past few years. In particular, low power circuit technologies for audio bandwidth A/D conversion, similar to the bandwidth for IR FPA readout, have routinely reached the 16-bit level, with resolution as high as 20 bits reported. For example, a 4th order incremental A/D converter with 18-bit resolution at 50 kHz has been proposed for space applications [52].

The advantages of on-chip A/D conversion are simplified system design, reduced susceptibility to system and cabling noise, including electromagnetic interference (EMI), reduced cable count,

reduced IC count, and reduced system mass and volume. However, for many applications, the additional power dissipation on the focal-plane negates the advantages. For low background linear arrays for spectroscopic applications, reduction in focal-plane cable count can be a significant reliability advantage. For cryogenic systems, the additional power dissipation on the focal-plane can be offset by reduction in the parasitic heat load of cabling, and the power required on-chip to drive the high cabling capacitance at sufficient voltage to allow 16 bit resolution to be realized at the system level. Thus, a realistic trade-off at the system level must be performed before the advantages of on-chip A/D are fully assessed.

6.2 Photon-Counting

Photon counting in an IR FPA can be achieved two ways. One is to amplify photoelectrons prior to the readout, and the second is to count individual photoelectrons using high gain in the unit cell electronics. Solid-state photomultiplier (SSPM) devices have been developed for some specialized low background, long wavelength application, but similar amplification in a broad range of wavelengths would be very useful.

In the area of readout electronics, preliminary work by JPL has indicated that it may be possible to achieve sufficient gain and noise rejection with advanced unit cell electronics to permit the detection of individual photoelectrons [53,54]. In this case, one or more bits representing the photon count must be stored in the unit cell. Practical application of this approach to area arrays will be possible for design rules below 0.8 microns. In this approach, multiplexing of the unit cells is noiseless, but the noise process is transferred to the unit cell amplifier and discriminator circuits.

6.3 Background Suppression

Pedestal removal in tactical IR FPA readout has been approached in several ways. Scientific sensors can also benefit from the suppression of the background signal, provided that suppression of the background does not introduce significant additional noise into a nearly BLIP signal. Without background suppression, large charge integration must be accommodated within the unit cell, implying

a large integrating capacitor -- a problem facing present IR FPA circuits. Typical pedestal removing circuits require integrating the complete signal prior to background suppression and would thus not alleviate the present problem. If done in the charge domain, the background suppression must thus be performed on a short time basis compared with the total integration time.

A unique background suppression circuit was proposed by JPL that operates in the current domain. Utilizing a high accuracy current memory device in the feedback loop of a CTIA circuit, background and FPN can suppressed, resulting in an orders of magnitude larger effective dynamic range and improved FPA performance [52].

6.4 Optical Readout

The capacitance and parasitic heat load associated with typical dewar cabling has initiated an exploration of optical readout of focal-plane arrays. Aerojet has proposed using optical signals to provide timing and power to a cryogenic FPA [55]. JPL has been investigating the use of on-focal-plane optical modulators for analog optical readout of an FPA [56]. In this configuration, a laser diode outside the dewar is optically connected by fiber to an analog optical modulator on the focal-plane. The modulated optical signal is then received via optical fiber outside the dewar and processed. Significant reduction in heat load and on-focal-plane power dissipation is achieved. Additional benefits can be attained by converting the FPA signal to digital format prior to utilizing the optical link, but at the likely expense of additional power dissipation.

6.5 Smart Focal-Planes

Increasing the amount of on-focal-plane processing can, in principle, reduce the data transmission requirements of a remote spaceborne science sensor. In general, the science community is not appreciative of altering the raw detector array signal on the focal-plane [57]. However, some future spectroscopic mapping missions may benefit from integrating feature extraction circuitry either in the instrument, or on the focal-plane itself to reduce deep space communications bandwidth requirements. Neural network circuits might be used efficiently on the focal-plane to recognize certain

spectral signatures and classify or tag particular data in order to reduce transmission bandwidth or initiate other higher level functions. Such spectro-cognitive neuroprocessing for imaging spectrometers was recently proposed by JPL.

Other "smart" functions that could be performed on the focal-plane include event-driven readout, where the readout is driven by the data itself, not by scanning circuits. Additional processing could include on-chip cosmic-ray circumvention, on-chip multiple sampling for read noise reduction, non-uniformity correction and micromotion stabilization. The latter might be achieved by integrating a fine guidance sensor function on same FPA as the detectors to actuate "adaptive" optics or piezoelectric transducers.

7. SUMMARY

This paper has attempted to summarize the major issues associated with infrared readout electronics for space science sensors. For many mature IR detector technologies, it is now the readout electronics that limit scientific performance rather than the detector itself. The general requirements for scientific IR FPA readout electronics were discussed. The state-of-the-art has been reviewed for both circuit approaches and technologies. The paper has reviewed source-follower per detector, direct injection, buffered direct injection, gate modulation input, cascode amplifier per detector, and capacitive transimpedance amplifier circuits. Noise reduction strategies were identified. Future directions for continued R&D have been suggested.

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TABLE I

Comparison of Performance Characteristics of Different types of Readouts used in IR FPAs

	SFD	DI	BDI	GMI	CTIA
Number of Transistors per Unit Cell	3	2	4 for ordinary inverter in cell; 5 for cascode	3	7 for diff. amp.; 4 for cascode amp.
Max. Intg. Time	R_oC_{int}	$R_oC_{int}A_{vm}$	$R_oC_{int}A_{vm}A_{vo}$	$R_oC_d/(1+g_{mi}R_o)$	$A_{vo}R_oC_{int}$
Min. Intg. Time		$R_oC_d/(1+g_{mi}R_o)$	$R_oC_d/$ $A_{vo}(1+g_{mi}R_o)$	C_{int}/g_{ds}	$1/2\pi f_a$
Operating Frequency	limited by power dissipation and data rate	low, for $\eta<<1$	high	moderate	high, limited by power dissipation
Integration cap.	smallest C_d~ 20 fF	~ C_{bus}	~C_{bus}	C_{int}/A_I; reduced by current gain (A_I)	C_{int} for $A_V>>1$ smallest < 1 fF
Noise	low-medium noise	minimum limited by a large C_{bus}		low noise	low noise
Bias Control	none	minimal	very good	minimal	very good
FPN	moderate due to V_T nonuniformity	low	low	high due to bias instability and V_T nonuniformity	low
Power	low	low	medium	low to medium	medium to high

TABLE II

Performance of Selected Readout ICs for Scientific Applications

Type	Format	Pitch (μmxμm)	C_{int} (fF)	T_{int}	Noise (e^-)	Data Rate (kHz)	Company	Comments
SFD	256x256	30x30	?	10-100 s	55 @ 10K 48 @ 50K	> 6.5	Hughes	MCS used
SFD	256x256	30x30	270	> 150 ms	700 @ 4K 186 @ 77K 60 @ 77K	< 400	Cincinnati	60 e^- noise with MCDS
SFD	256x256	40x40	60-85	10 ms	19-40 @ 7K	< 300	Rockwell	off-chip CDS used
CAD	1x32	?	2200	10 sec	10 @ 20K	?	Amber	MCS used
BDI	30x92	50x100	?	312 μs	80 @ 67K	300	Westing-house	TDI
GMI	128x128	60x60?	40	22 ms	4.8 @ 200K	?	Rockwell	Current gain > 47000
CTIA	260x1	25x?	30	42 μs	120 @ 67K	< 6500	Hughes	in-pixel CDS
CTIA	32x134	50x50	10	42 μs 167 μs	1.9 @ 67K 7 @ 67K	< 3200	SBRC	in-pixel CDS; TDI
CTIA	10x132	25x75	4	25 μs	3.3 @ 145K	< 5000	Rockwell	in-pixel CDS; TDI
CTIA	128x128	50x50	4	20 ms	3.4 @ 78K	?	Rockwell	in-pixel CDS

FIGURE CAPTIONS

Fig. 1 Schematic of an infrared focal-plane array.

Fig. 2 Schematic of a source-follower per detector unit cell. The detector capacitance is often the integration capacitance.

Fig. 3 Schematic of a direct injection unit cell circuit.

Fig. 4 Schematic of a buffered direct injection unit cell circuit.

Fig. 5 Schematic of a gate modulation input unit cell circuit.

Fig. 6 Schematic of a cascode amplifier per detector unit cell. The detector capacitance is often the integration capacitance.

Fig. 7 Schematic of a capacitive transimpedance amplifier unit cell circuit.

Fig. 8 Input-referred noise electrons as a function of integration capacitance.

Fig. 9a Schematic of CDS readout data construction.

Fig. 9b Schematic of a modified CDS readout data construction.

Fig. 9c Schematic of a multiple correlated sampling readout data construction.

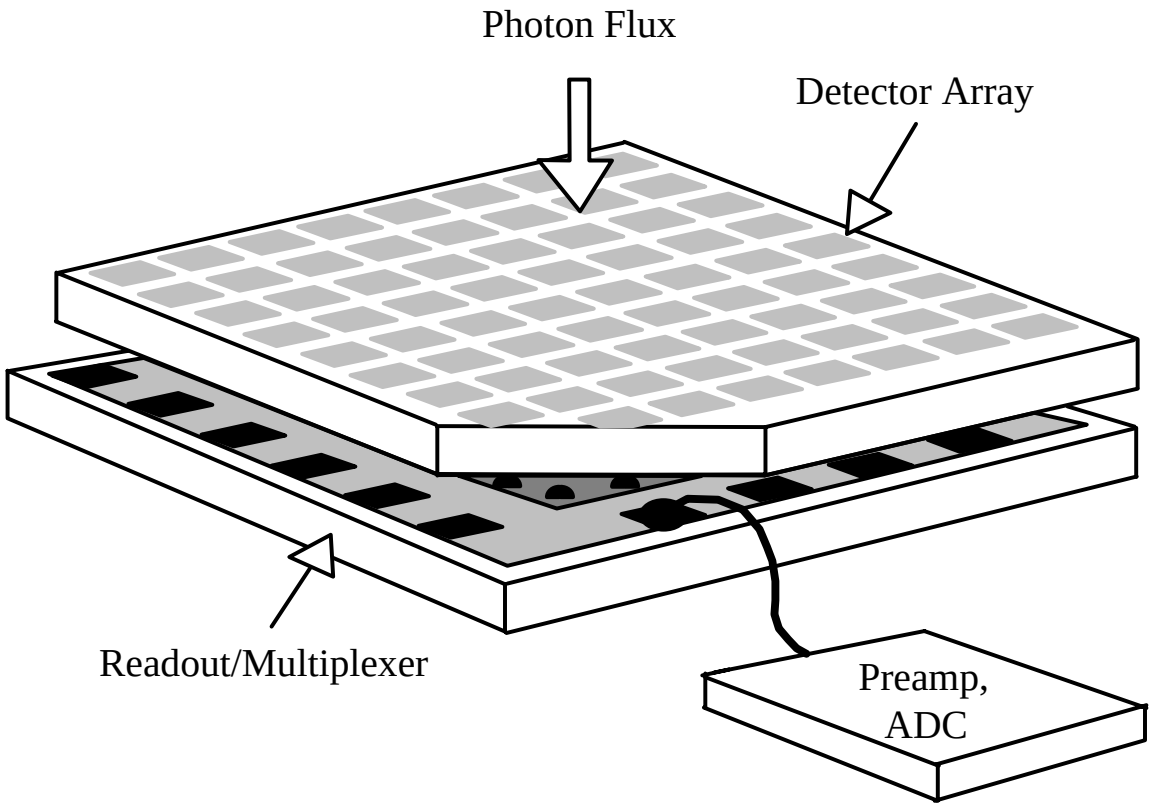


Fig. 1 Schematic of an infrared focal-plane array.

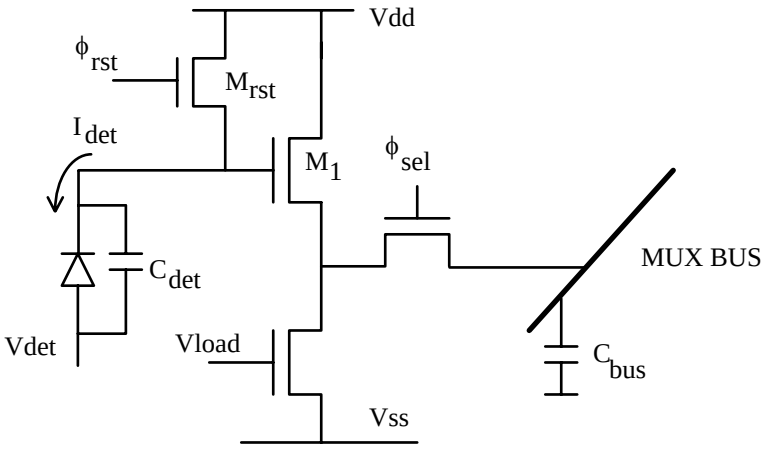


Fig. 2 Schematic of source-follower per detector unit cell.

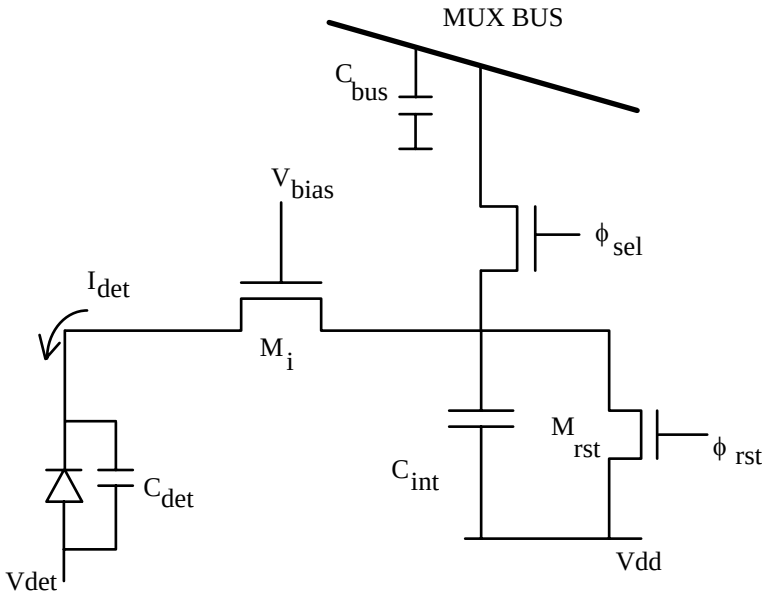


Fig. 3 Schematic of a direct injection unit cell circuit.

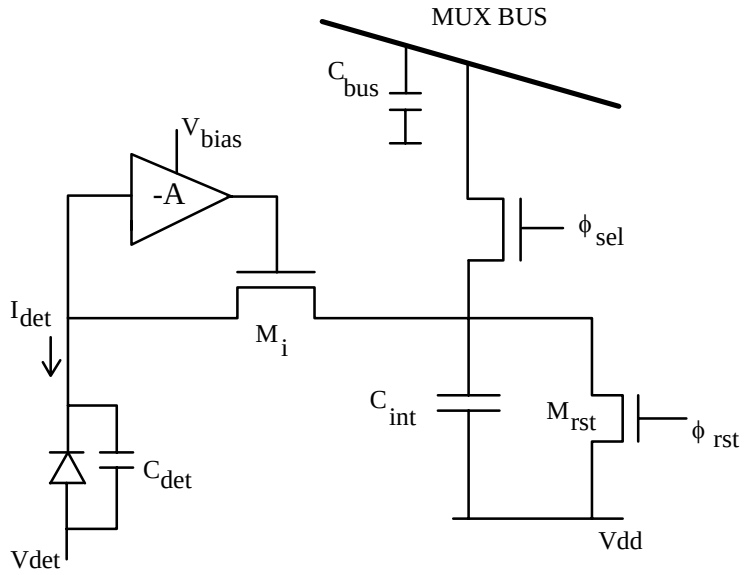


Fig. 4 Schematic of a buffered direct injection unit cell circuit.

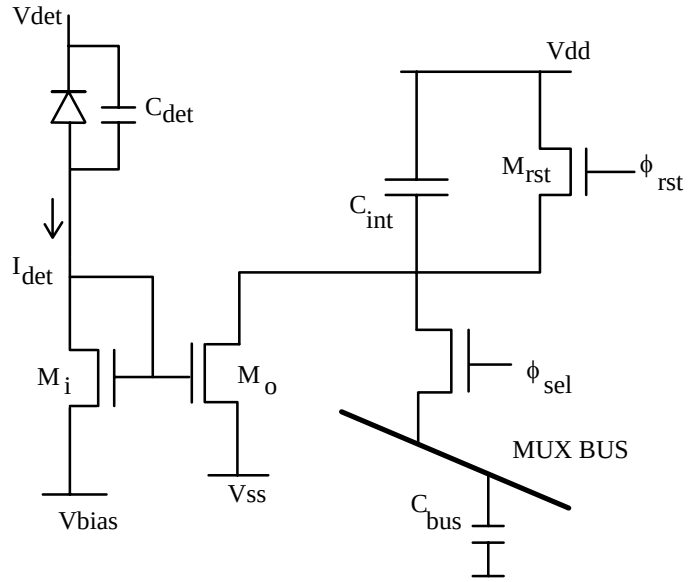


Fig. 5 Schematic of a gate Modulation input unit cell circuit.

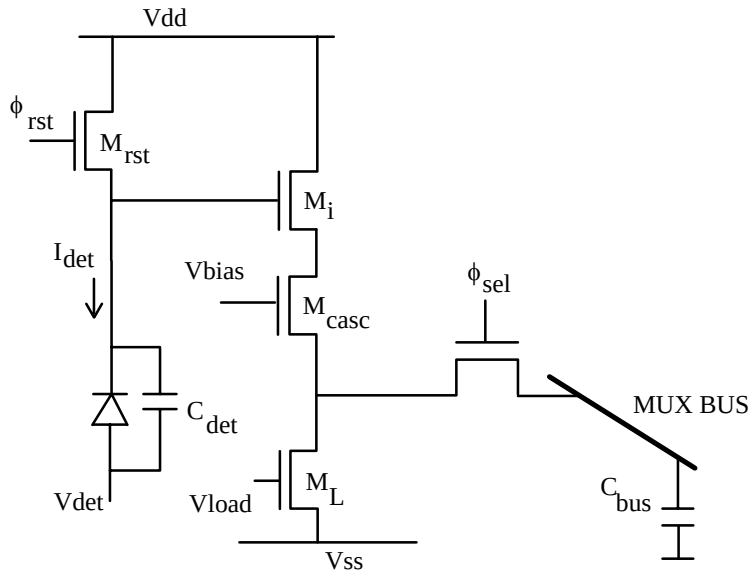


Fig. 6 Schematic of a cascode amplifier per detector unit cell circuit.

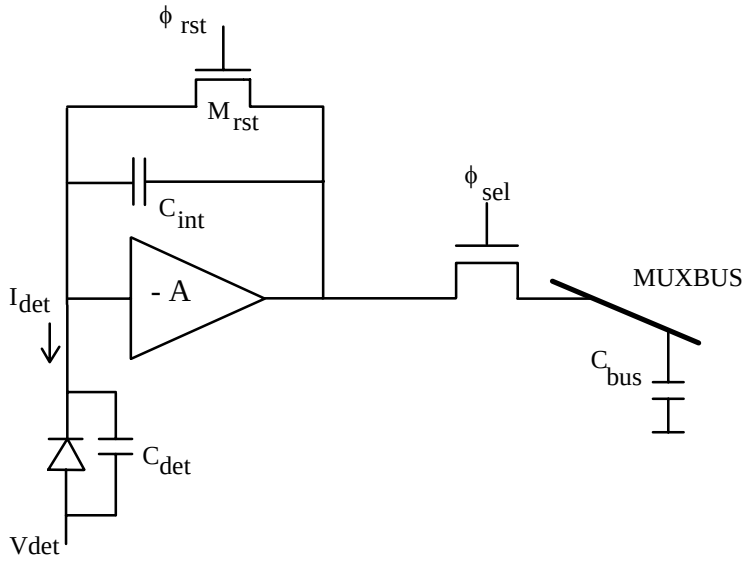


Fig. 7 Schematic of a capacitive transimpedance amplifier unit cell circuit.

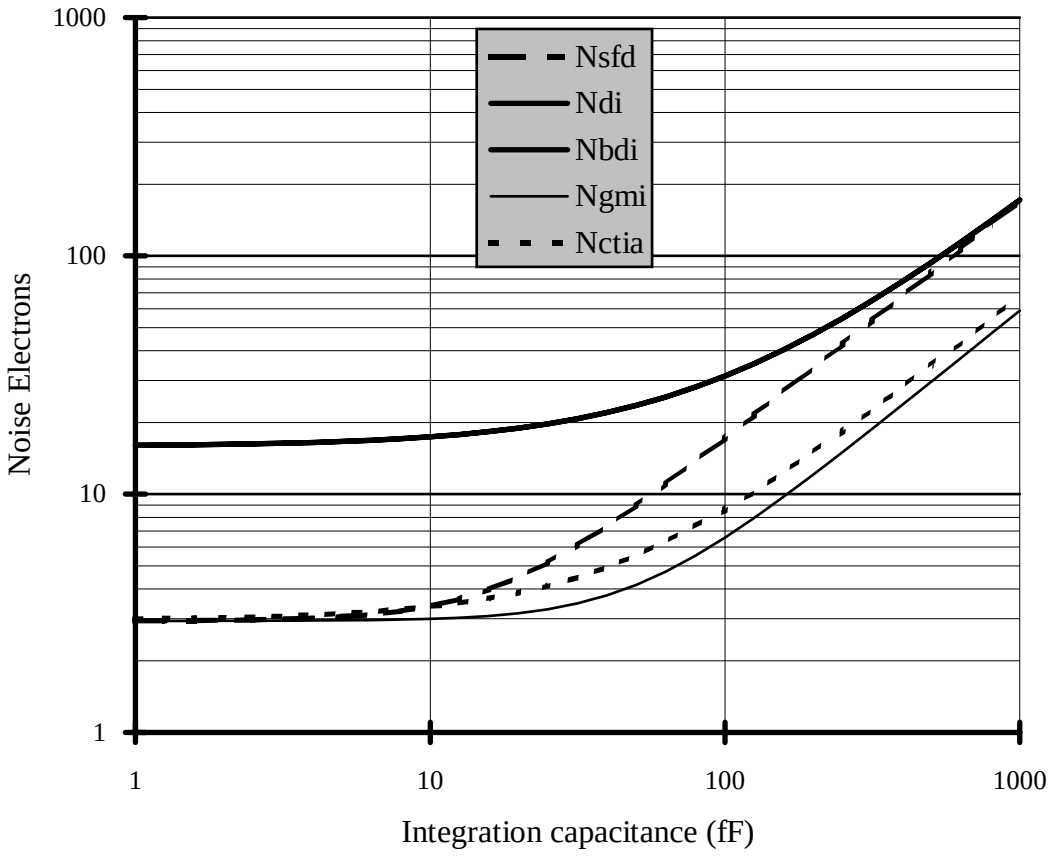
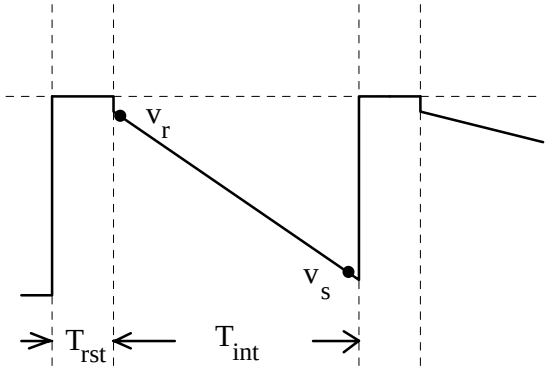


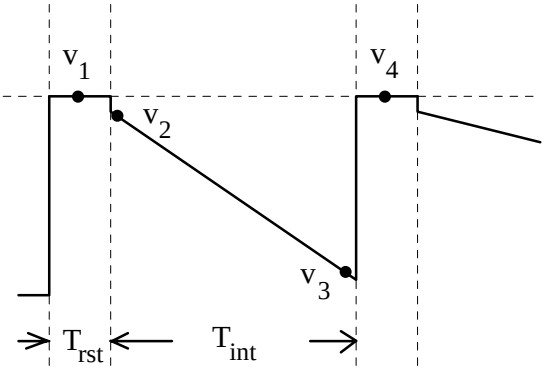
Fig. 8 Input-referred noise electrons as a function of integration capacitance.

C_{det} = 50 fF, C_{bus} = 0.2 pF, R_o = 1x10^{14} Ω, T_{int} = 10 msec.



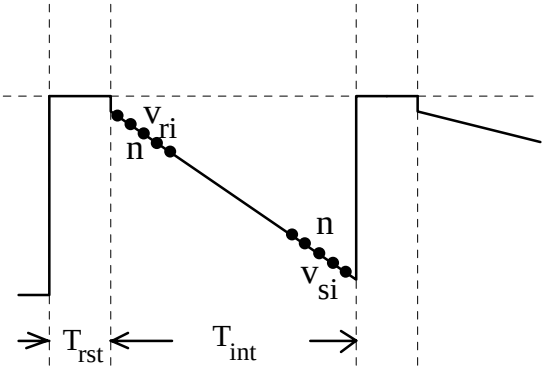
$$v_{cds} = v_r - v_s$$

Fig. 9a Schematic showing CDS readout data construction.



$$v_{mcds} = v_1 - v_2 + v_3 - v_4$$

Fig. 9b Schematic showing modified CDS readout data construction.



$$v_{mcs} = \Sigma\ (v_{ri} - v_{si}) / n$$

Fig. 9c Schematic showing MCS readout data construction.