FA 11.4: A CMOS Imager with On-Chip Variable Resolution for Light-Adaptive Imaging

Z. Zhou[1], B. Pain, E. Fossum[2]

California Institute of Technology, Pasadena, CA
[1]CondorVision Technology, Inc., Fremont, CA
[2]Photobit Inc., La Crescenta, CA

In addition to advantages of lower power and system miniaturization through camera-on-a-chip implementation, the CMOS active pixel image sensor (APS) enables development of smart imagers by integrating custom CMOS signal processing circuits on the focal plane [1,2]. This CMOS APS imager is capable of enhancing signal to noise ratio (S/N) under low illumination through summation of signals from neighboring pixels. On-chip S/N improvement in CMOS APS is demonstrated by pixel averaging or by pixel binning [3]. Pixel binning is implemented in a CMOS APS primarily designed for frame-transfer [4]. That implementation suffers from extraneous noise pick-up and high-residual fixed-pattern noise (FPN) due to the use of single-ended column integrator. This APS has improved kernel summing circuits implemented in fully-differential topology. The imager performance is improved by greatly reducing FPN and temporal circuit noise. This multi-resolution APS is suited for application in light-level-adaptive imaging.

Figure 1 shows the schematic of the multi-resolution chip. The column integrator array performs parallel signal summation for different rows. The summed signals are stored in the column memory capacitor bank. The global output integrator carries out the column-wise signal summation. Row and column decoders are used for randomly addressing the sensor array and for programming the size of the summation kernels. The schematic of the signal chain from the sensor pixel to the output of the chip is shown in Figure 2. The sensor uses a photogate APS pixel design [1]. The column circuits consist of a fully-differential switched-capacitor integrator, a pair of column memory capacitors, CLR and CLS, and the MOS switches for integration. The sample-and-hold capacitors, CMR and CMS, for the pixel reset and signal levels serve as the input capacitors for the column integrator. The column memory capacitors, CLS and CLR, are input capacitors for the output integrator. The output integrator uses two matched single-ended two-stage opamps. They drive 30pF and 1MW load at above 8M-Pixels/s, required for 30Frames/s readout of a 512x512 element array. The column opamp is a folded cascode opamp with switched capacitor common mode feedback circuit. It operates at much lower speed due to the column parallel readout. 2 MHz unit gain frequency and 60dB dc gain are sufficient for column parallel integrator settling with better than 9b accuracy. The amplifier is optimized to use minimum transistor size and lowest bias current.

For a nxm (n columns and m rows) kernel summation readout, signals from m rows of the sensor pixel are integrated by the column integrators one row at a time. The reset and signal levels of each row are first sampled on the S/H capacitors CMS and CMR as the integrators are reset. They are then differentially integrated on CIS and CIR. This process continues until all the rows in a given kernel are summed. The integrated signals are sampled and held on the column memory capacitors CLS and CLR. After row summation is completed, every n consecutive columns are integrated after each reset of the global integrator. The summed signals from nxm kernels are read out serially from the output of the global integrator. The summation kernel size is programmable according to illumination conditions. By using a square kernel size of nxn, the S/N enhancement is $\sqrt{n}$. At low illumination, S/N enhancement is greater than $\sqrt{n}$ since the circuit read noise dominates in the imager noise.

The column-wise FPN is caused mostly by the column opamp offset. In the fully differential readout, the offset is first sampled on the feedback capacitors as the integrator is auto-zeroed. To first order, it is compensated at each step of signal integration. Clock feedthrough appears as common mode pulse to the integrator and does not contribute to FPN. Residual FPN due to the capacitor ratio mismatch on the two sides of the integrator is given by,

$$V_{os,o} = m(\alpha_R - \alpha_S)V_c = m\Delta\alpha V_c \qquad (1)$$

where m is the number of row summation, $\Delta\alpha$ is the mismatch in capacitor ratio and V_c is the common mode voltage. The temporal read noise consists of noise from the pixel, the detector shot noise, noise associated with switching (kTC noise) and noise from the opamps. The output referred noise for n x m kernel summation can be approximated by,

$$\left\langle V_o^2 \right\rangle \approx n\frac{2kT}{C_m}\alpha^2\left\{2m\alpha^2 + \alpha + 3\beta + 2m(1+\alpha)b + mg^2\overline{N}\right\} \qquad (2)$$

where $C_{MR} = C_{MS} = C_M$; $C_{IR} = C_{IS} = C_I$; $C_{LR} = C_{LS} = C_L$; $C_{OR} = C_{OS} = C_O$;

$$\alpha = \frac{C_M}{C_I} = \frac{C_L}{C_O}\ ;\ \beta = \frac{C_M}{C_L}\ ;$$

g is conversion gain measured in volts/electrons: and $\overline{N}$ is average number of electrons per pixel during a single exposure. Estimated noise voltage at full resolution readout is about 320μV for 125Frame/s image readout rate, close to the measured value.

A 128x128 prototype sensor uses a 1.2μm single poly double metal n-well process with linear capacitor option. The sensor pixel is 24x24μm² with 29% optical fill factor. The column circuit is laid out in the 24μm column pitch and has total length of about 0.9mm. The chip area is about 4.7x5.2mm². Figure 3 shows the chip layout.

The device is tested at up to 125Frames/s. Figure 4 is a full resolution image taken at 100k-Pixels/s readout. Readout speed is limited by the pulse generator and the data acquisition board in the test bed. Results are summarized in Table 1. The sensor demonstrates 1.2V saturation signal, 72dB dynamic range and 8.3μV/e- conversion gain. The FPN is about 6mV (0.5% saturation), read noise 300μV and dark current 0.6nA/cm². More than 40% of the total 24mW power is consumed by the global integrator opamps due to the required drive capability. Images shown in Figure 5 demonstrate the signal enhancement as the summation kernel changes from 1x1 (no summation) to 2x2 and to 4x4. As the summation kernel size increases, both the signal amplitude and the image contrast increase. Figure 6 shows measurement of signal and S/N enhancement as kernel size is increased from 1x1 to 2x8 at constant illumination and exposure time. The output signal linearity over 1.2V range indicates good accuracy of row and column summation. S/N improvement is 11dB, as expected by theoretical prediction from Equation 2.

Acknowledgments:

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References: See page 433.

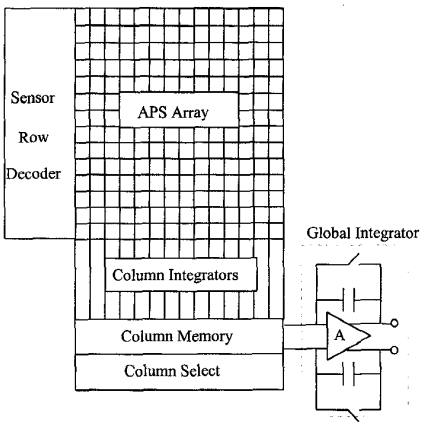


Figure 1: Schematic of the multi-resolution APS imager.

Figure 2: See page 433.

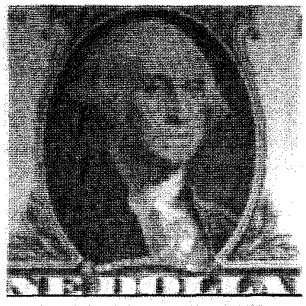
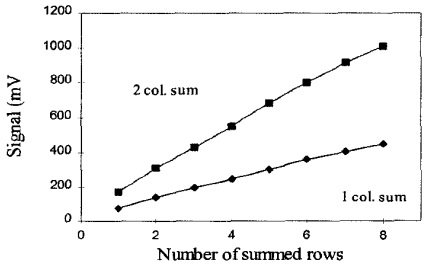


Figure 4: Raw image at full resolution at 100k-Pixels/s.



(a)

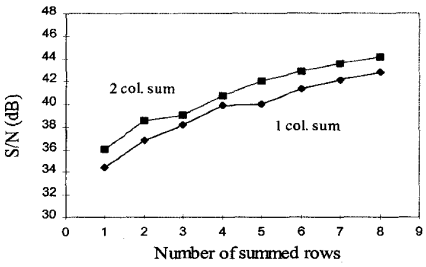


Figure 6: (a) Signal, and (b) S/N as a function of column and row summation for constant illumination.

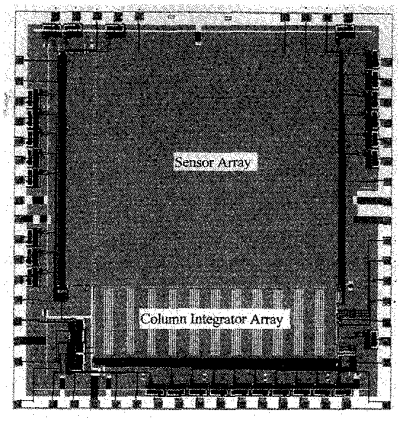


Figure 3: Sensor chip layout.

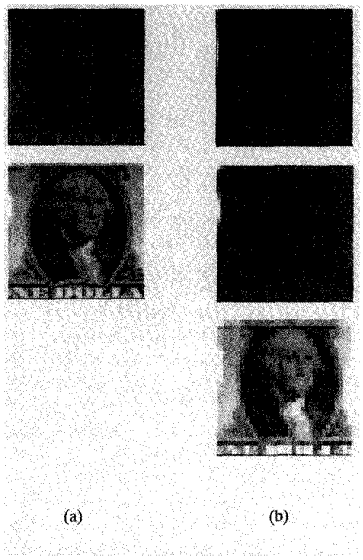


Figure 5: Image taken for summation kernel of 1x1, 2x2, and 4x4 at two (a and b) different illumination level.

Imager format	128 x 128
Integrator linearity:	better than 8 bit out of 1.8 V swing
Sensor saturation:	1.2 V
Temporal Noise:	303 μV r.m.s.
Dynamic range:	72 dB (disregarding FPN)
Conversion gain:	8.3 μV/e^-
Power consumption:	24 mW @ 125 frames/sec.
FPN:	6 mV
Dark current:	54 mV/sec. (0.6 nA/cm^2)

Table 1: Summary of the test results.