A CMOS ACTIVE PIXEL IMAGE SENSOR WITH AMPLIFICATION AND REDUCED FIXED PATTERN NOISE

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ABSTRACT

A CMOS active pixel image sensor (APS) with in-column programmable amplification is reported. The in-column amplification is achieved by using an auto-biased gain stage. Single-ended capacitor-coupled sampling in the column is used to reduce the fixed pattern noise (FPN). The sensor is implemented as a 64x64 element array fabricated using standard 2 μm n-well CMOS technology through MOSIS. The output conversion gain of the imager is 10 μV/e^- and 52 μV/e^- for low and high gain operation modes respectively. The in-column gain enhances the signal to noise ratio by a factor of 2.5. The FPN is about 3 mV and saturation 1.1 V. The variation of the gain is observed to be less than 3% in different columns.

I. INTRODUCTION

CMOS active pixel image sensors (APS) have recently emerged as a low cost alternative to charge-coupled devices for many applications [1,2]. The CMOS APS features good quantum efficiency, low read noise, high dynamic range, random accessibility, simple TTL-compatible clocking, and 100% compatibility with on-chip CMOS circuits for control, timing and analog-to-digital conversion. The major obstacle to utilization of APS technology is fixed pattern noise (FPN).

Previously reported CMOS APS designs employ a simple source-follower for pixel readout, two sample and hold capacitors in each column and a matched pair of output source-follower stages for reset and sampling signal output respectively [1]. This signal chain reduces the net output conversion gain since the output source-follower stage has gain less than unity, and introduces FPN susceptibility due to threshold voltage mismatch between the reset and signal sampling channels. While digital systems can compensate the FPN by using stored offsets and simple DSP, reduced FPN is desired for all-analog imaging systems.

This paper presents a different approach in APS signal readout that uses an auto-biased gain stage with a source-follower buffer and a.c.-coupled sampling capacitor in each column, and a single auto-zeroing, offset-compensated op-amp output stage. The gain stage improves the signal-to-noise ratio and the a.c.-coupled single-ended output reduces the FPN.

II. DESIGN AND OPERATION

The complete readout circuit is illustrated in Fig.1(a). Timing for the circuit operation is shown in Fig. 1(b). The design and operation of the pixel electronics has been described

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previously [1]. Briefly, the photosignal is integrated under the photogate PG. For readout, a row at a time is selected using transistor MP3. The floating diffusion node FD is reset to approximately 3.5 V using transistor MP1. The photogate is then pulsed to transfer the signal charge over the d.c. biased transfer gate TX (1.5 V) to the floating diffusion (FD) node. The floating diffusion node voltage change (typically 400-600 mV) is buffered by the in-pixel source-follower MP2 and load transistor MC1 located at the bottom of the column.

The column readout circuit consists of an auto-biased gain stage (MC3, MC5, MC7) followed by a source follower buffer (MC8, MC9). Auto-biasing is achieved by closing the auto-bias switch MC4 during the pixel reset operation. The circuit gain is reduced by the feedback capacitor CG3 to approximately unity gain if the high gain switch MC2 is disabled, and approximately a gain of 5 with MC2 enabled. The source-follower drives the a.c. coupling capacitor CC. During pixel reset, the clamp switch MC10 clamps the sampling capacitor CS to V_{ref} through the sampling switch MC11. Following pixel reset, the clamp switch is disabled. The pulsing of the photogate causes an increase in the voltage on the sampling capacitor CS proportional to the photosignal charge. Following the photogate pulse, the sampling switch is disabled to hold the photosignal on the sampling capacitor. It should be noted that this sequence of operations occurs in all columns simultaneously. The power saving switch MC6 can then be enabled, cutting off the current flowing in the column amplifiers.

The sampling capacitors in each column are then sequentially scanned for serial readout. Rather than using a source-follower per column as in previous CMOS APS designs, the charge on the sampling capacitor is dumped onto the horizontal bus. The bus voltage is kept constant using the capacitance transimpedance amplifier (CTIA) at the end of the horizontal bus. Thus the output of the CTIA has a voltage gain of CO/CS. The integrating capacitor, CO, is reset between each column selection. The auto-zeroing CTIA is designed to drive an oscilloscope at 30 Hz video frame rate. It uses a two-stage high gain op amp biased in a switched capacitor scheme. Capacitor CA is designed to pre-store the DC offset at the input of the op amp during the sampling period, which is then compensated in the output signal during the amplifying period. This auto-zeroing is not necessary for FPN reduction.

III. EXPERIMENTAL RESULTS

The sensor were implemented as a 64 X 64 array fabricated through MOSIS by using standard 2 μm n-well CMOS technology. The sensor chips were tested using the timing and biasing described above at a 24 Hz frame rate. The acquired images were monitored using a TV monitor driven by a scan converter. Quantitative measurements were taken at 100 kpixels/sec readout rate using a 16-bit, 100 kHz ADC and a PC computer. The input-referred conversion gain of the sensor was measured to be approximately 10 μV /e^- and 52 μV /e^- for low and high column gain operation respectively. A gain of 5.2 was obtained in-column for the high gain operation. No observable variation in the in-column gain was seen in the video image and the histogram of the gain distribution showed the variation were less than 2% for low gain and 3% for high gain operations. The output saturation level was measured to be 1.1 V for both low and high gain operation. This saturation is limited by the output voltage swing of the inverting amplifier, with about 2 V compliance being taken by the drain to source voltages of transistor MC7 and MC5.

Unexpected decoder feedthrough was observed in the raw image, likely due to capacitive coupling of the NAND decoder to the floating horizontal output bus. It is expected that use of a shift-register-style column scanning circuitry will eliminate this effect. Disregarding the decoder feedthrough, the measured FPN is about 3 mV p-p (0.27% saturation) This result is much better than the previously reported CMOS APS value of 3.3% saturation [1]. Fig. 2 shows the output image with the decoder feedthrough suppressed using DSP with the bottom, light-shielded row of the image used as offset reference.

The temporal noise performance was worse than that of previously reported chips. The noise level was measured to be 1.2 mV and 2.5 mV rms for low and high gain operation respectively, resulting in the dynamic ranges of 59 dB and 54 dB. The high noise level is likely coming from the extra gain circuit and the CTIA amplifier. Anomalously high 1/f noise was measured in accompanying n-channel test transistors (as high as 2 $\mu V/\sqrt{Hz}$ at 1 Hz). Better designs for these circuit to reduce the noise is currently under research. Although the in-column gain increases the noise, the signal-to-noise ratio is enhanced by a factor of 2.5.

IV. CONCLUSION

A CMOS APS with in-column programmable gain and low fixed pattern noise readout circuits has been demonstrated. The in-column gain enhances the S/N ratio by a factor of 2.5 with variation of less than 3% between columns. Although excessive decoder circuit coupling resulted in undesirable FPN spikes, the residual FPN was shown to be less than 0.27% saturation and indicates the likely FPN performance in an image sensor employing shift register scanning of columns.

V. ACKNOWLEDGMENTS

The research presented in this paper was carried out by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was supported by the National Aeronautics and Space Administration, Office of Advanced Concepts and Technology.

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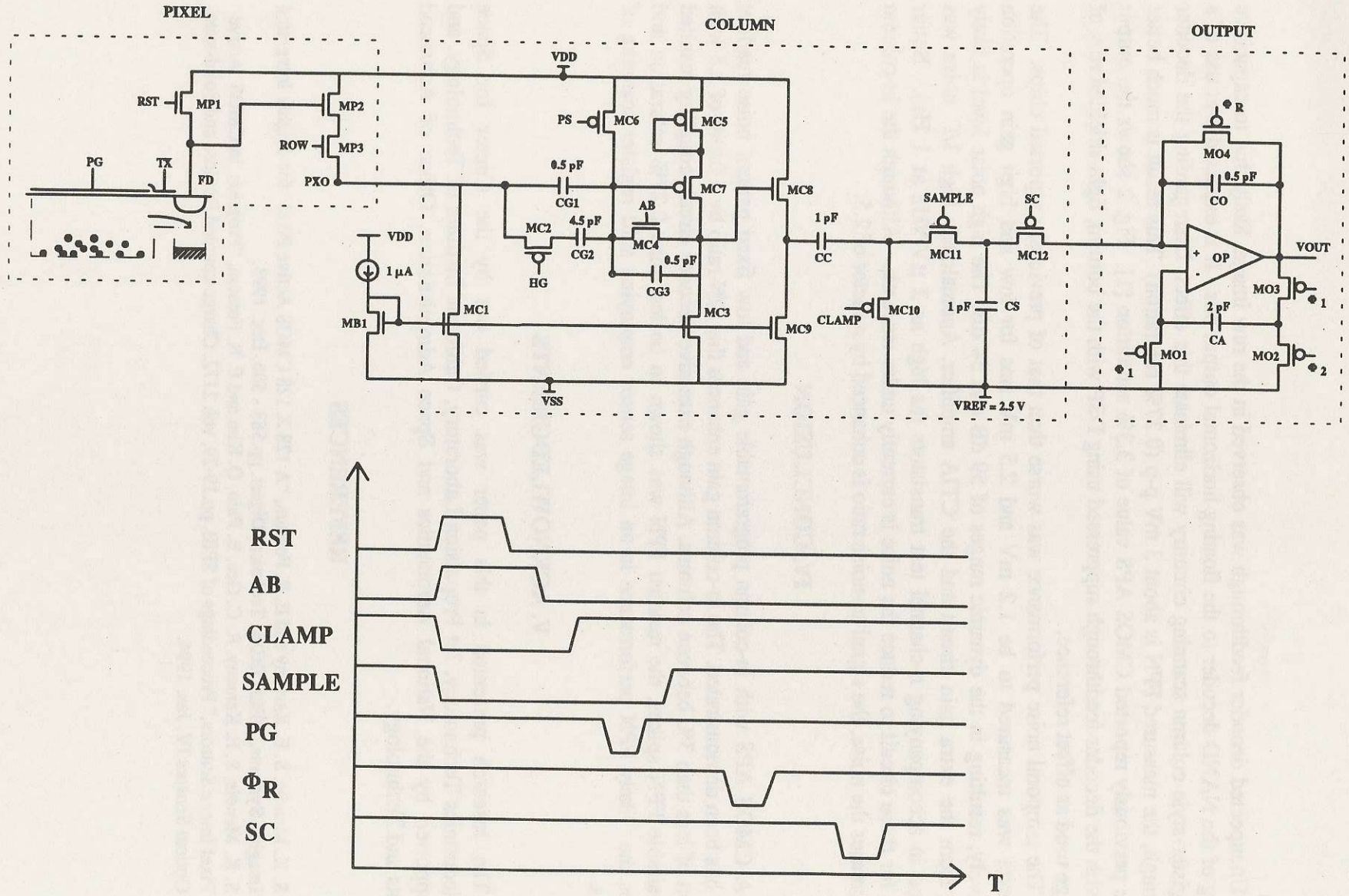
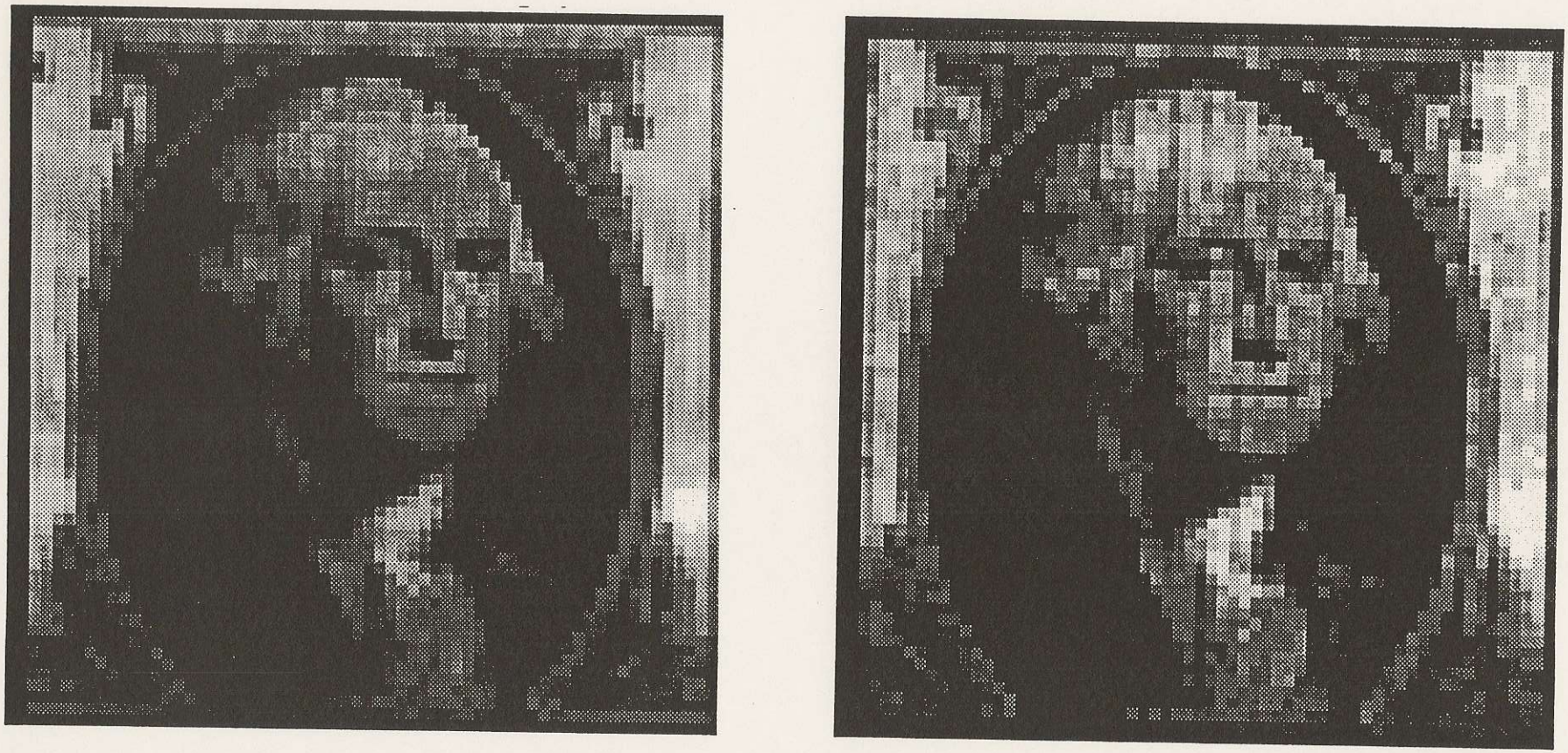


Figure 1(a) , Complete Readout Circuit. and 1(b), Clock Diagram



(a)

(b)

Figure 2, Images Taken With (a), Low Gain Operation and (b), High Gain Operation