TP 13.5: A 256x256 CMOS Active Pixel Image Sensor with Motion Detection

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This 256x256 active pixel sensor (APS) is designed for consumer multimedia applications requiring low-cost, high-functionality, compact cameras capable of acquiring high-quality images at video frame rates. This sensor allows random access of the image data, permitting a simple implementation of electronic pan and zoom. Use in portable equipment is simplified by standard operating voltages and low power (80mW@5V, 20mW@3.3V). Fabrication in a standard CMOS process allows the integration of a variety of new and existing digital circuits with the image sensor. In addition, by making use of the implicit dynamic frame buffer provided by the active pixel structure, the sensor can generate a signal that represents the difference between sequential frames. This may be used for motion detection, image stabilization, and compression purposes.

Each pixel in the APS imager is comprised of a photogate and four n-channel transistors as shown in Figure 1. Unlike previous APS photogate designs, the pixel design requires only a single polysilicon layer (i.e. no overlapping transfer gate) for full compatibility with the standard digital CMOS process [1]. During integration, the polysilicon photogate PG is biased to Vdd and carriers collect under the gate. The gate (Tx) of the transfer device Q1 is permanently biased to 1.25V, isolating the collected charge from the floating diffusion output node (FDON). During readout, FDON is first reset via Q2. PG is then driven to 0V and charge flows through Q1 to FDON. The source follower/access switch (Q3-Q4) drives the column output bus.

Use of local gain inside the pixel avoids the stringent charge-transfer efficiency requirement of a CCD process, and allows array size to be increased without readout speed and noise degradation. Pixel area is, however, increased and fill factor is reduced. In the 0.9μm CMOS process the APS pixels are 20x20μm² with a 25% fill factor (photogate area/total pixel area). Typically CCD pixels are less than one quarter this area and have higher fill factors [2].

Figure 2 shows the sensor architecture. Because of the random-access design, any sub-window of the array may be read out to perform electronic pan and zoom. By loading the row and column counters with non-zero values, the origin of the readout window may be arbitrarily changed. The size of the window may be set by controlling the maximum counts of these devices. The entire array may be read at a rate of 60f/s. Row access lines (PG, Tx, Row) run horizontally from row decoders.

Each column bus feeds into an output circuit at the base of the array. This circuit, shown in Figure 3, is used to sample and hold both the reset and signal values on the column bus. This arrangement allows correlated double sampling (CDS) of the pixel output to reduce pixel kTC noise, 1/f noise, and fixed pattern noise due to threshold variation. The reset and signal values are passed through a column decoder that selects one signal/reset pair for output. Finally the selected signal pair are fed to a differential amplifier that subtracts the reset value from the signal value, resulting in a CDS video output.

Figure 4 is a timing diagram for the signal required for operation of the circuit in its normal video output mode. To operate the device in differential mode, in which the difference between sequential frames appears at its output, use is made of the fact that, at the end of a normal cycle, the floating diffusion output node - FDON in Figure 1 - acts as a dynamic storage node onto which has been placed a charge representing the optical input of the photogate. In effect, the array of storage nodes is an implicit analog frame buffer, storing the entire frame. By altering the timing to that shown in Figure 4, it is possible to generate the difference signal. Rather than starting with a reset operation, the value on the output node (the "old" frame) is read out to one of the sample-and-hold capacitors. The reset is then performed, followed by a normal read operation (the "new" frame). This signal value is then stored on the other sample-and-hold capacitor. The two capacitors are then fed to a differential amplifier in the normal manner, however the output of that amplifier is now the frame-to-frame difference. Note that the hardware required for both normal and differential modes is identical - only signal timing is altered.

Although there is some charge leakage from the storage node during the integration period, under normal exposure conditions this does not have a significant effect on differential image quality. In a motionless scene, the differential output signal is 0V. Any movement in the scene causes a non-zero output to appear - by correlating the non-zero output with the address currently being applied to the row and column decoders it is possible to determine the position of the motion in the scene.

Conversion gain within the pixel is measured at 7μV/electron and the saturation level is 1.5V output-referred. Figure 5 shows the quantum efficiency (QE) of the APS compared to that of two commercial CCD devices.

The primary APS noise source is the pixel output transistor. Typical output-referred noise levels are 29 electrons rms and 74dB dynamic range. Fixed-pattern noise, dominated by column-to-column variations in output transistor thresholds is typically 1-2% after the output stage (Figure 3). This is reduced by an order of magnitude upon activation of a further level of sample-and-hold circuits that subtract the threshold variation between the pairs of output stage source followers.

References

[1] Mendis, S., et al., "CMOS Active Pixel Image Sensor", IEEE Trans. Electron Devices, vol. 41, no. 3, pp. 452-453, March, 1994.

[2] Kobayashi, A., et al., "A 1/2-in 380k-Pixel Progressive Scan CCD Image Sensor", ISSCC Digest of Technical Papers, pp. 192-193, Feb., 1993.

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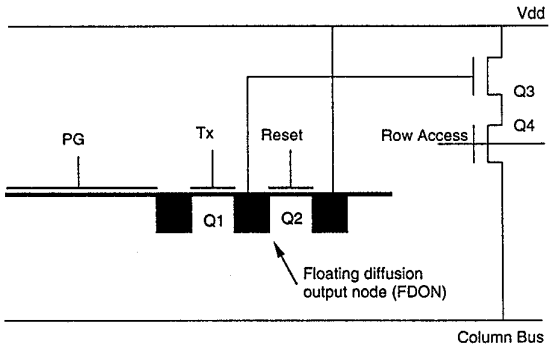

Figure 1: Active pixel circuit.

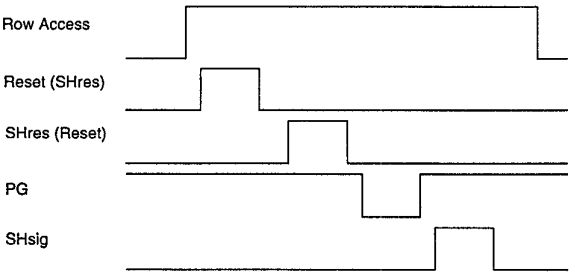

Figure 4: Timing diagram for normal video output, and in parentheses, that for frame-to-frame differential output.

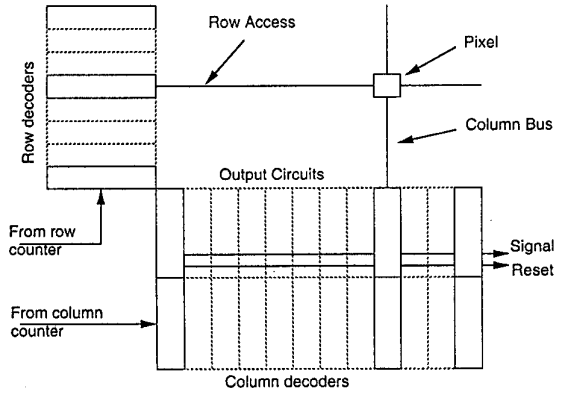

Figure 2: APS architecture.

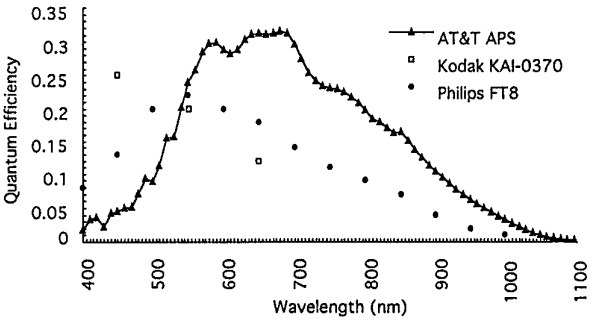

Figure 5: Quantum efficiency vs. wavelength for CMOS APS and those for a commercial interline transfer CCD and a commercial poly-gate frame transfer CCD.

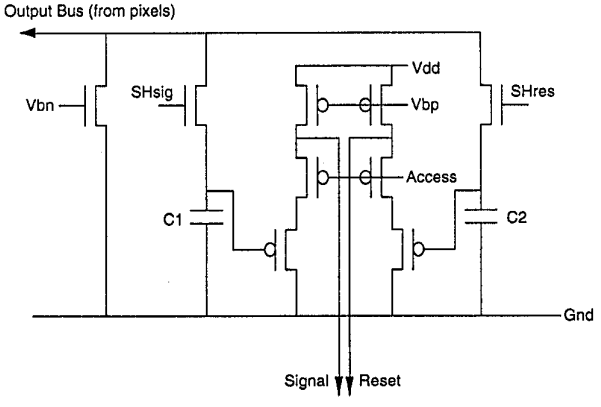

Figure 3: Sample and hold, source follower, and column access switches.