WA 17.7 A 250mW, 60Frames/s1280x720 Pixel 9b CMOS Digital Image Sensor

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Many imaging systems with industrial and machine vision applications now require sensors with a combination of >1Mpixel resolution and >30frames/s rate. This must be achieved at low cost and with minimum impact on system complexity or power consumption. Reported CCDs have this level of performance. However, the inherent analog nature of CCDs leads to a requirement for driving large external loads at high frequency from the image sensor. CMOS active pixel sensors (APS) are ideal for these applications due to the possibility for on-chip signal processing (especially analog-to digital converters [ADC]) integration and inherent low power consumption [1]. This advantage is especially important in large-format high speed imaging applications. Other CMOS image sensors reported to date have either targeted small-format applications or are low frame rate devices.

This 1280(H) x 720(V) CMOS APS capable of 60 frames/s operation includes on-chip, 10b, column-parallel, self-calibrating ADCs with 9b performance. Four 10b wide digital output ports support a data rate of 55.3 Mpixels/s. The sensor is in a standard 0.5μm 2P2M technology and has power consumption <250mW.

The sensor floorplan is shown in Figure 17.7.1. The core pixel array consists of 1280(H)x720(V) photodiode active pixels with 7.9μm pitch. Eight additional columns are added to each side of the array, and ten additional rows are added to the top and bottom of the sensor to aid in the alignment of the sensor in an optical system. In addition, 8 optically inactive rows of pixels, and a row of analog multiplexers at the bottom of the array to provide dark current calibration and ADC testing. Each of the 640 column-parallel ADCs at the bottom of the imager array is shared by two pixel columns and has a 15.8μm pitch.

To provide maximum flexibility, the majority of sensor functions are externally controlled, with the exception of the ADC timing and the readout sequencer blocks. The readout sequencer block controls the timing and multiplexing of a 160b wide, low speed, low noise internal digital bus onto the four, 10b output ports.

The sensor ADCs use a column-parallel successive-approximation architecture (Figure 17.7.2) [2]. A key feature of the column-parallel ADC architecture is the low conversion rate required from each ADC in the array, which has to operate only at the array row rate, rather than at the pixel rate. Each of the ADCs used in this sensor needs only operate at 200ksamples/s, even at the full 60Hz frame rate. Reducing this bandwidth greatly reduces power consumption of the ADC block. Each ADC is preceded by an analog sample-and-hold which includes correlated double sampling (CDS) for temporal noise suppression. Self-calibrating, fixed pattern noise (FPN) cancellation circuitry, integrated in each ADC, corrects for fixed column-to-column offsets. The ADCs are re-calibrated at the beginning of every frame to correct for environmental variations.

Another power-saving architectural feature is the use of a 160b wide, slow internal bus to transfer the ADC results to the digital output ports. Due to the large sensor format, the capacitive load on the internal data bus can be quite substantial. Operating this bus at the pixel rate would be prohibitive due to excessive power consumption. Figure 17.7.3 is a block diagram of the data path from the data in the ADC's latches to the four output ports. The internal data bus simultaneously transfers the data from 16 ADC's to the Output Sequencing block. Sixteen pixel blocks are transferred during each transition of ϕ_S. The sequencing block sorts this data for the four, 10b wide output channels. Data from four pixels becomes available at the output during each of the ϕ1- ϕ4 clock phases. Each of these clock phases corresponds to one input clock pulse. Therefore, the wide internal data bus reduces the internal transfer speed to 1/4th that of the output ports even though the data is appearing at the pixel rate at all output ports.

At 60 frames/s, the sensor is clocked from a 74.25MHz source. The total row time at this frame rate is 22.32μs. This period is divided between the time required for analog operations, i.e. the readout of a pixel row and the ADC conversion, and that for digital operations, i.e. the time to burst out the digital data from an entire row. A high-speed clock allows an entire row of data to be burst out from the four output ports in 4.32μs. This maximizes the time available for the analog section of the operation. The analog sequence starts with the selection of a pixel row, whose output is sampled onto the ADC inputs. Each ADC is shared by two columns and must perform two conversion cycles in each row. These digital results are stored in the ADC internal latches. The data is then transferred in a 16 pixel block through the internal digital bus. The sequencing block then transfers this data in 4 pixel blocks to the 4 output channels. This process is continued to read out an entire row.

Maximizing the analog cycle time allows pixel readout and ADC operations at a rate three orders of magnitude slower than the input clock. Separating analog-to-digital conversion and digital output in time also has the effect of preventing digital crosstalk from corrupting the ADC process.

The sensor is in a 0.5μm, 2P, 2M process. Yield on the large-area dice is sufficient for commercial applications. The output-referred conversion gain of the sensor is approximately 7μV/e-. Measured output-referred dark current in the sensor at room temperature is 23mV/s or approximately 860pA/cm^2. Measured saturation is 2.5V or 357,000e-. Figures 17.7.4 and 17.7.5 show the differential and integral nonlinearity of a typical ADC in the array. The sensor fixed-pattern noise is reduced to 2 LSB or 0.4% of saturation with the ADCs auto-calibration function. An example image taken with the sensor is shown in Figure 17.7.6. Measured sensor total power consumptionis 250mW at 5V supply and 60 frames/s. The 640 ADCs in the array, and the internal readout bus account for 150mW. Each ADC is operated at 200ksamples/s and performs two conversions per row. This corresponds to a figure of merit of ~1μW/1kHz [2].

References:

[1] E.R. Fossum, "CMOS Image Sensors: Electronic Camera on a Chip" (Plenary paper), Tech. Dig. of IEEE International Electron Devices Meeting, pp. 17-25, Dec. 1995.

[2] Z. Zhou, B. Pain, E.R. Fossum, "CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-To-Digital Converter", IEEE Transactions on Electron Devices, pp. 1759-1763, October 1997.

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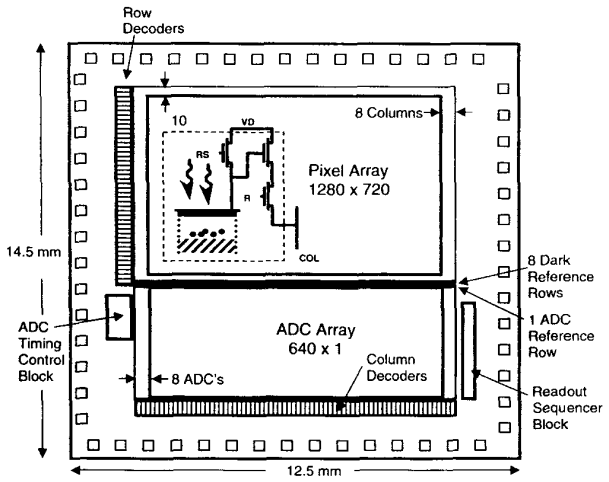

Figure 17.7.1: APS digital imager floorplan.

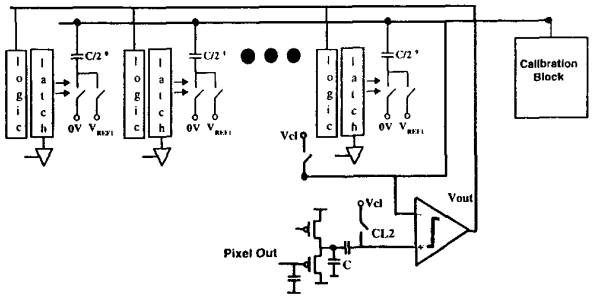

Figure 17.7.2: Successive-approximation ADC architecture.

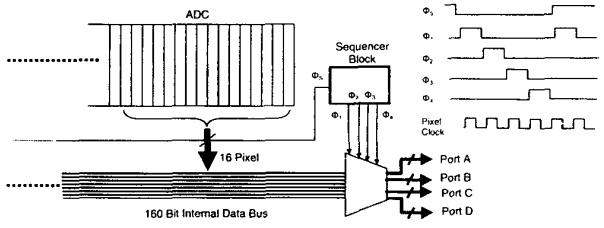

Figure 17.7.3: Data path block diagram.

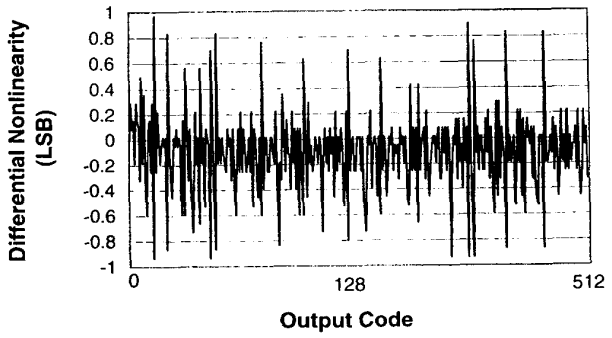

Figure 17.7.4: 9b converter differential nonlinearity.

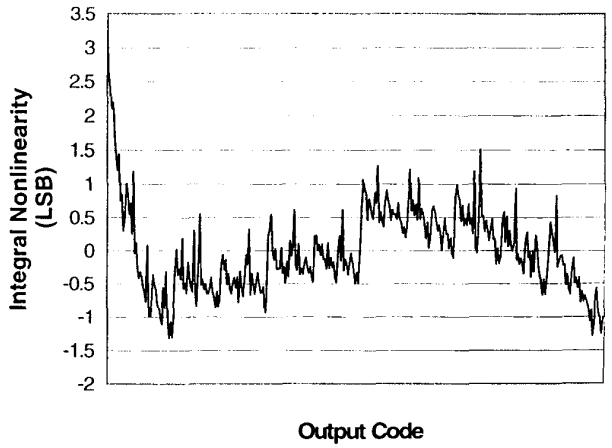

Figure 17.7.5: 9b converter integral nonlinearity.

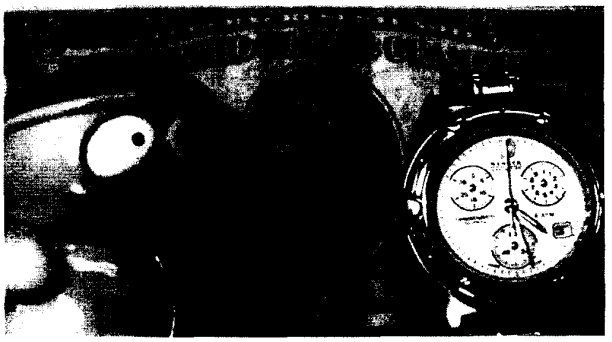

Figure 17.7.6: Sample Image.

Technology	0.5µm, 2P, 2M
Pixel array size	1280(H) x 720(V)
Format	Progressive
Pixel size	7.9µm x 7.9µm
Designed for Optical fill factor (effective fill factor larger)	23%
On-chip ADC	10-bit column parallel, 9-bit performance
Output structure	10-bit digital, Quad port
Maximum frame rate	> 60 fps
Pixel readout rate	> 55 Mpix/sec
Conversion gain	7 µV/e-
Dark signal (output referred)	23 mV/sec
Dark current (room temp)	860 pA/cm^2
Saturation	2.5 V
Saturation	357000 e-
Fixed pattern noise	< 2 LSB p-p
Power consumption	< 250mW at 5 volts

Table 17.7.1: Measured performance.