

PG, a d.c. biased transfer gate TX and an output diffusion FD. It also contains a reset transistor R, a source-follower input transistor and a row-selection transistor X. In essence, a small surface-channel CCD has been fabricated in each pixel. At the bottom of each column of pixels, there is a load transistor VLN and two output branches to store the reset and signal levels. Each branch consists of a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower with a column-selection switch (Y1 or Y2). The readout circuits are common to an entire column of pixels, except the load transistors of the second set of source followers VLP1 and VLP2, which are common to the entire array.

The operation of the CMOS active-pixel sensor is illustrated in Fig. 2. It is assumed that the rail voltages are 5V and 0V, although higher and lower voltage operation is possible and has been demonstrated. The transfer gate TX and the source follower load transistors VLN, VLP1 and VLP2 are biased at 2.5V. During the signal integration period (Fig. 2a), photo-generated electrons are collected under the photo-gate biased high at 5V. The reset transistor R is biased at 2.5V to act as a lateral anti-blooming drain, and the row-selection transistor X is biased off (0V). Following signal integration, an entire row of pixels are read out simultaneously. First, the row of pixels to be read out are addressed by enabling row selection switch X. The pixel output node FD is reset by briefly pulsing the reset gate R to 5V, to reset the floating diffusion output node FD to approximately 3.5V (Fig. 2b). The output of the first source follower is sampled onto capacitor CR at the bottom of the column by enabling sample

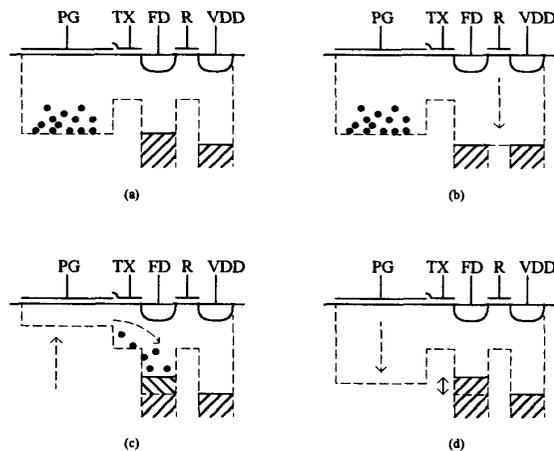


Fig. 2. Operation of the active-pixel-sensor: (a) signal integration; (b) reset; (c) signal charge transfer; (d) signal readout.

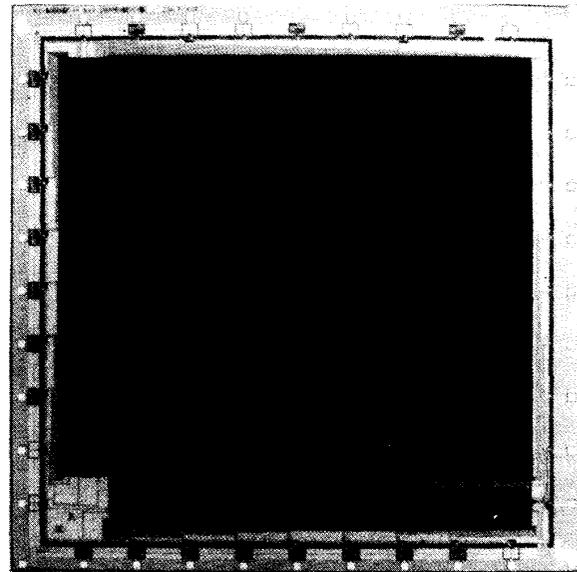


Fig. 3. Photograph of completed integrated circuit.

and hold switch SHR. Then, PG is pulsed low to 0V, transferring the signal charge to FD (Fig. 2c). The new output voltage is sampled onto capacitor CS by enabling sample and hold switch SHS (Fig. 2d). The stored reset and signal levels are sequentially scanned out through the second set of source followers by enabling column address switches Y1 and Y2. Storing the reset and signal levels on separate capacitors permits correlated double sampling (CDS) which suppresses kTC noise from the pixel and 1/f noise and threshold variations from the output transistor [11]. The main source of noise in this system is the kTC noise introduced by the sample and hold capacitors. The calculated r.m.s. noise on each 1 pF capacitor is 64 μ V, resulting in 91 μ V for differential mode.

The pixel unit cell and read out circuits were designed to achieve 30 Hz operation of a 128 \times 128 array. The fabricated image sensor consists of a 128 \times 128 array of active pixels, row and column address decoders, clock generator circuits and a bank of sample and hold capacitors and read out circuits. A double-poly, double-metal p-well CMOS process with 2 μ m design rules was used through MOSIS, resulting in a 40 μ m \times 40 μ m pixel size. The fill-factor calculated as the ratio of the active area in the design to the total pixel area is 26%. The 7-bit row and column address decoders were formed using standard CMOS logic permitting direct

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X-Y addressing of the image sensor. The address decoders and the clock generator circuits were laid out to fit within the 40 μm pixel pitch. The completed IC fits a standard MOSIS 6.8 mm \times 6.8 mm die and was packaged in a 40 pin DIP. A photograph of the completed IC is shown in Fig. 3.

3. Experimental Results

The active pixel image sensor was operated with the timing and voltages described above. Both dark and illuminated testing of the sensor was performed. By performing electrical tests on a test structure on a separate IC, the pixel sensitivity was determined to be 4.0 $\mu\text{V}/e^-$. The sensor was nominally clocked at 2 $\mu\text{s}/\text{pixel}$, corresponding to a frame rate of approximately 30 Hz. Although the well capacity was calculated to be approximately $6 \times 10^6 e^-$, saturation was determined by the output amplifier, and was observed to be 600 mV or 150,000 e^- . Global fixed pattern noise (FPN) observed in the differential output signal was approximately 20 mV p-p (3.3% sat.), with a local variation of approximately 8 mV p-p. The global variation is attributed to poor control of the p-well potential towards the center of the array since slower clocking rates reduced the effect, and an earlier 28 \times 28 array showed a similar but much smaller effect. Dark current was measured to be approximately 62 $e^-/\text{msec}/\text{pixel}$, or under 1 nA/cm². Noise in the fabricated array is fundamentally limited to 22 e^- r.m.s. due to the kTC noise on the 1 pF sample and hold capacitors. However, the measured noise level at a 30 Hz frame rate at room temperature is presently limited by dark current shot noise to approximately 42 e^- r.m.s., for a dynamic range of 71 dB. No

lag or smear was observed and blooming was suppressed through the biasing of the reset transistor R. A laser spot scan of a single pixel was performed with a 632 nm He-Ne laser with a beam diameter of approximately 1.5 μm . The responsivity map of the pixel scanned with a step size of 2 μm is presented in Fig. 4. The layout of the pixel is shown in Fig. 5 for comparison. The response is uniform across the poly1 photo-gate area with no overlap of poly2 or metal, and drops off rapidly at the edges. A lower response is noticeable in areas overlapped by poly2. Performance of the sensor is summarized in table 1. Images acquired by the CMOS active pixel sensor were displayed on a video monitor. A photograph of a US one dollar bill taken from the video monitor is shown in Fig. 6.

4. Conclusions

A new CMOS-based image sensor that is well suited for highly integrated imaging systems has been presented. Significant improvement in CMOS active-pixel-sensors is anticipated in the near future. Reducing fixed-pattern noise through the use of an n-well process and improvements in the column CDS circuitry are currently being investigated. A pixel design with a floating gate output structure enabling multiple read operations is also being considered. Reduction in pixel size through the use of 0.8 μm CMOS technology should reduce dark current. The use of microlenses will improve the effective fill-factor to over 70%. This initial work paves the way for the development of more complex pixel structures and the integration of on-chip electronics in the future.

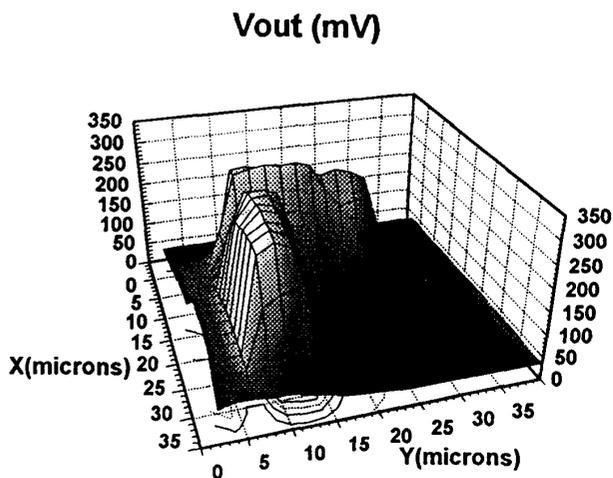


Fig. 4. Responsivity map of pixel.

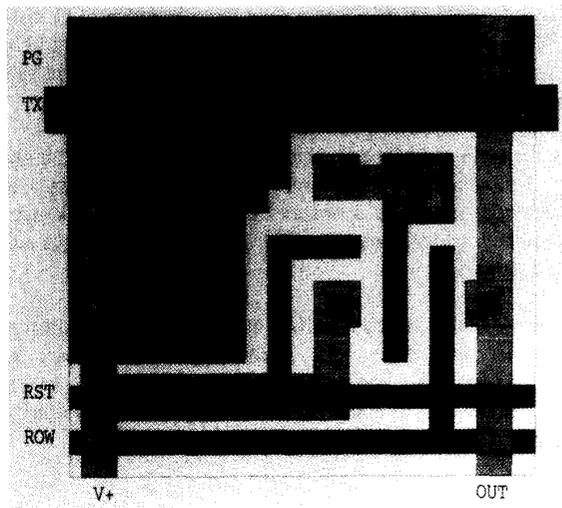


Fig. 5. Layout of pixel.

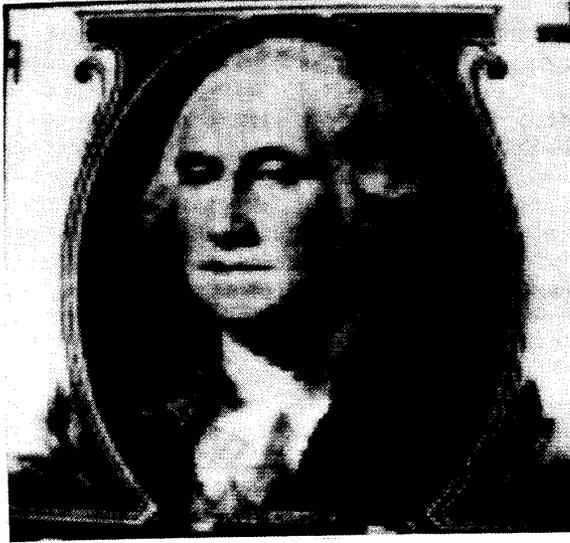


Fig. 6: Photograph of US \$1 bill taken from video monitor.

5. Acknowledgments

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Table 1. CMOS Active Pixel Image Sensor

| PARAMETER | VALUE |
|-----------------------|--|
| Technology | 2 μm p-well CMOS |
| Pixel Size | 40 μm \times 40 μm |
| Array Size | 128 \times 128 |
| Aperture | 26% |
| Required Voltages | Clocks: 0, 5V; d.c. 2.5 V |
| Dark Current | 62 $\text{e}^-/\text{ms}/\text{pixel}$ |
| Nominal Pixel Readout | 500,000 pixels/s |
| Output Sensitivity | 4.0 $\mu\text{V}/\text{e}^-$ |
| Noise | 42 e^- r.m.s. |
| Saturation | 150,000 e^- |
| Dynamic Range | 71 dB |
| Fixed Pattern Noise | 3.3% p-p sat |

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