12.3 A 1¼ inch 8.3M Pixel Digital Output CMOS APS for UDTV Application

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Several ultra-high definition imaging sensors, applicable in TV systems, electronic cinemas and tele-medicine, have been reported [1-3]. However, these sensors require a large optical system, high power and many components for driving and signal-processing circuits, limiting the realization of a practical camera system. A newly developed digital-output CMOS image sensor fabricated in 0.25μm CMOS technology for a compact ultra-high definition television (UDTV) camera is presented. The image sensor size corresponds to 1¼-inch optical format and the die size of the chip fits into the standard reticle window (20mm x 20mm).

The UDTV system requires 8.3 million pixels, 60frames/s operation in the progressive scanning mode, which translates to approximately 500MHz pixel readout rate. To eliminate the difficulty of handling analog signals with such a wide frequency bandwidth, analog-to-digital converters (ADC's) are implemented on-chip. A block diagram of the UDTV sensor and a layout plot are shown in Figs. 12.3.1 and 12.3.2, respectively. A sensor architecture is adopted having column-parallel successive-approximation 10b ADC's, column-parallel 2 SRAM banks [4] and 16 parallel output ports to achieve the high throughput of over 5Gb/s. There are 3936 x 2196 pixels and 3840 x 2160 effective pixels resulting in a pixel pitch of 4.2μm to fit a 1¼-inch optical format. Although the sensor reported in [4] achieved 9.75Gb/s, with a 7.0μm pixel, exceeding the data throughput of 5.2Gb/s for this UDTV application, the smaller pixel size of 4.2μm and the larger number of pixels requires adaptations to the design. These include a smaller pixel, implementation of a column-gain stage, a shared-ADC with sample-and-hold circuits, operation timing, noise-robust bias circuits and careful bus routing for high quality image reproduction. Due to the layout pitch, one 10b ADC is shared by 2 columns and the column-parallel signal processors are split into 2 banks, each having 984 ADCs at the top and bottom of the array.

The pixel consists of a deep n-well/p-substrate photodiode with on-chip microlens and 3 transistors: a driver transistor, a reset transistor and a row select transistor. The fill factor of the photodiode without the microlens is about 40%. To obtain a high precision optical black level clamp, optical black pixels with light shields, consisting of a metal layer and black filter material, are implemented at the periphery of the effective pixels.

Prior to the ADCs, an analog gain stage, which has gain settings of x0.7, x1.0, x1.3, x2.0, x4.0, is employed. Fixed-pattern noise (FPN) generated in each pixel and the column analog signal chain is suppressed before the A/D conversion. Potential column FPN caused by the input-offset voltage variations of the ADC's are suppressed by self-calibration functionality implemented in each ADC.

Figure 12.3.3 shows a row timing diagram. The column-analog gain stage is activated at the beginning of a row time, and a signal voltage and an offset voltage after pixel reset are sampled and held ('Gain and S/H'). This operation is done in parallel for all columns. No data readout occurs during these two periods to avoid potential digital noise interference, since this analog processing period is critical for low noise performance. Two A/D conversion cycles ('ADC1' and 'ADC2') follow in the remaining period. The digital data is sampled into the front-end memory SRAM 1, and is shifted into the back-end memory SRAM 2 for readout when the digitization is complete. This configuration permits the readout of the previous row data during the 'ADC' periods. The timing control circuits generate all the required pulses from four input pulses: a master clock, a frame trigger, a row trigger, and a shutter trigger.

A photo of the image sensor sample in a 262 pin ceramic PGA package is shown in Fig. 12.3.4. This particular sensor sample is without the glass lid and the black filter for demonstration purposes. Decoupling capacitors are placed on the edge of the cavity to stabilize applied voltages.

A reproduced image obtained from the 8.3M-pixel UDTV sensor is shown in Fig. 12.3.5. The sensor operated in the progressive scanning mode at 60frames/s, with column-amplifier gain of 1.0 and no FPN is seen. Figure 12.3.6 displays a magnified image from a center portion with resolution of 2000 lines.

Power consumption was measured at less than 760mW including the power consumed in output drivers when the sensor operates at 60frames/s progressive scanning mode with a master clock at 49.5MHz and 3.3V supply. Conversion gain of 0.06LSB/e^- is extracted from the photon shot noise measurement, which corresponds to 43μV/e^- at the pixel electrode. Saturation charge and random noise are 25,000e^- and 42$e^-_{r.m.s.}$, respectively, with an ADC input range of 750mV, analog gain of 0.7 and hard reset operation. This yields a dynamic range of 55.0dB. Since the reset-noise component is estimated to be 35$e^-_{r.m.s.}$, the results suggest the random noise is dominated by the reset-noise. FPN including the FPN caused by the column parallel processors is less than the random noise level. Sensitivity with on-chip microlens was measured to be 4.2kb/lux-s (3.0V/lux-s) using a 2700K light source and an IR-cut filter with cut-off wavelength 650nm.

A 60rames/s 1¼-inch 8.3M-pixel digital-output CMOS APS features lower power and smaller optical format than earlier CCD UDTV sensors and should pave the way for digital cinema and tele-medicine applications as well as UDTV in the future.

Acknowledgements
The authors acknowledge A. Krymski, N. E. Bock, J. Solhusvik, P. O. Pahr, G. Strand and F. Okano for their valuable discussions.

References
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[2] K. Mitani, et. al., "Experimental Ultrahigh-Definition Color Camera System with Three 8M-pixel CCDs," *SMPTE Journal*, pp. 148-153, April 2002.
[3] S. Stough, et. al., "High-Performance Electro-Optic Camera Prototype," *SMPTE Journal*, pp. 140-146, March 2001.
[4] A. Krymski, et. al., "A High Speed, 240frames/s, 4 Megapixel CMOS Sensor," *IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 28-131, June 2001, and to appear in IEEE Trans. Electron Devices, Jan 2003.

 0-7803-7707-9/03/$17.00

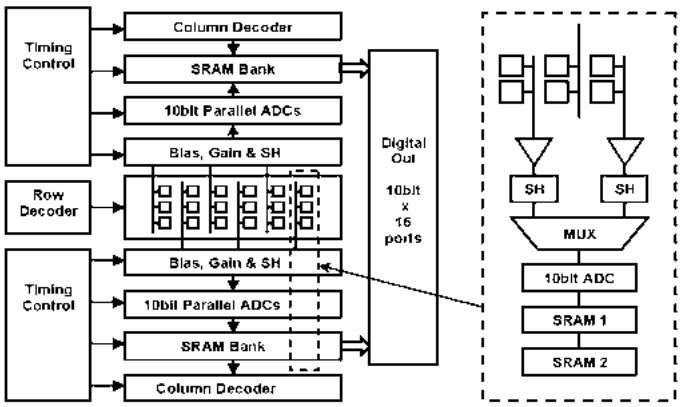

Figure 12.3.1: Chip block diagram.

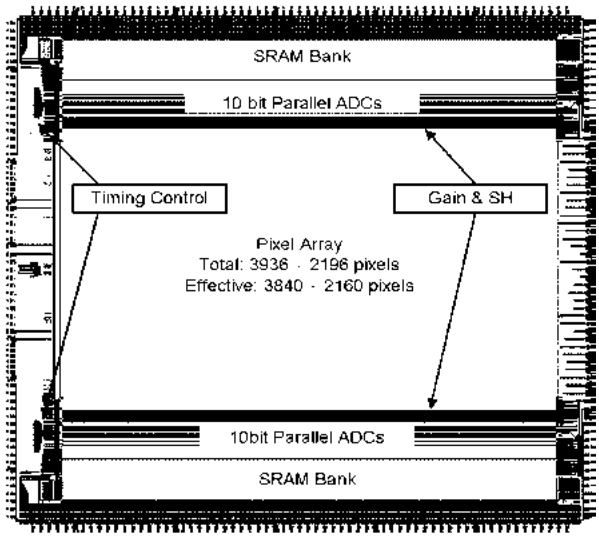

Figure 12.3.2: Chip layout.

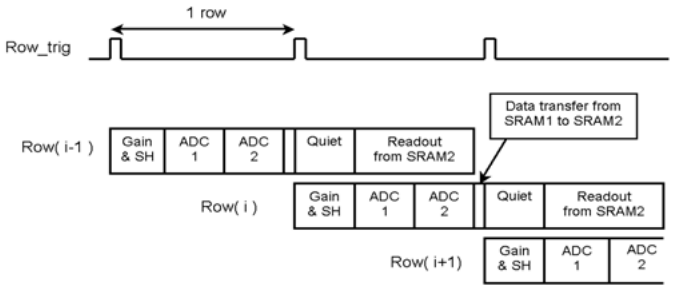

Figure 12.3.3: Row operation timing.

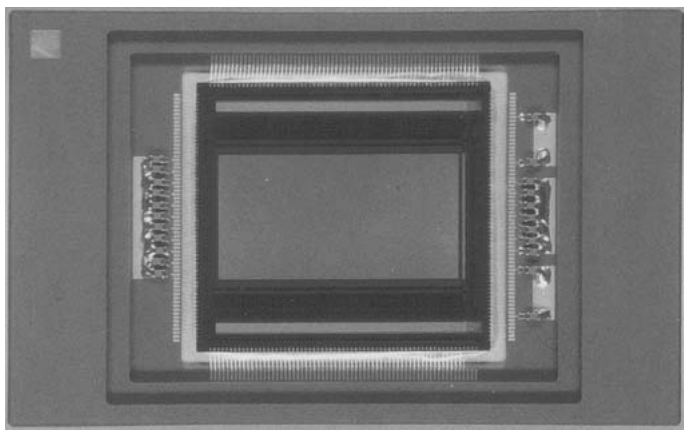

Figure 12.3.4: Chip and package photograph.

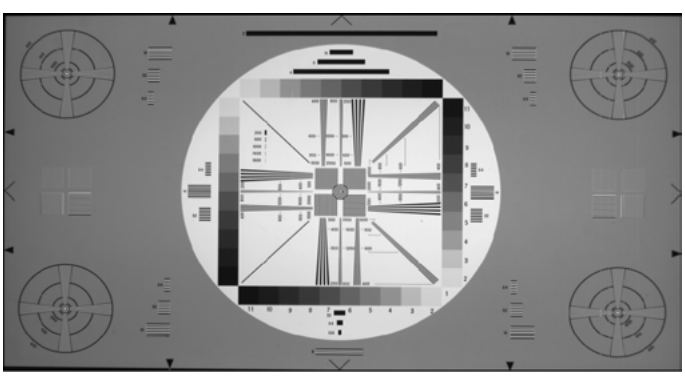

Figure 12.3.5: Reproduced image.

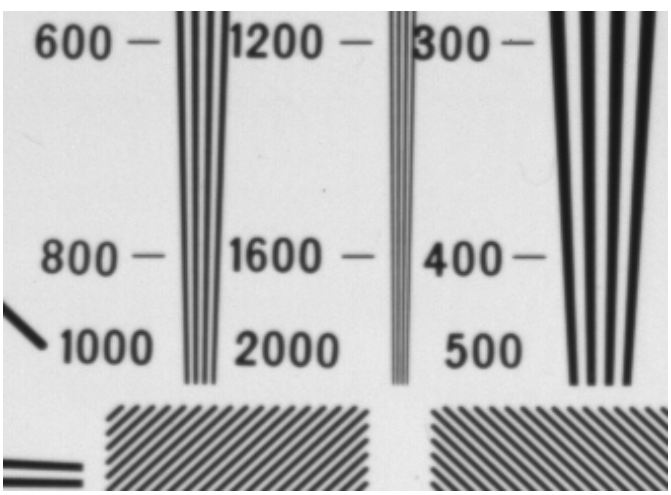

Figure 12.3.6: Reproduced image (magnified center portion).

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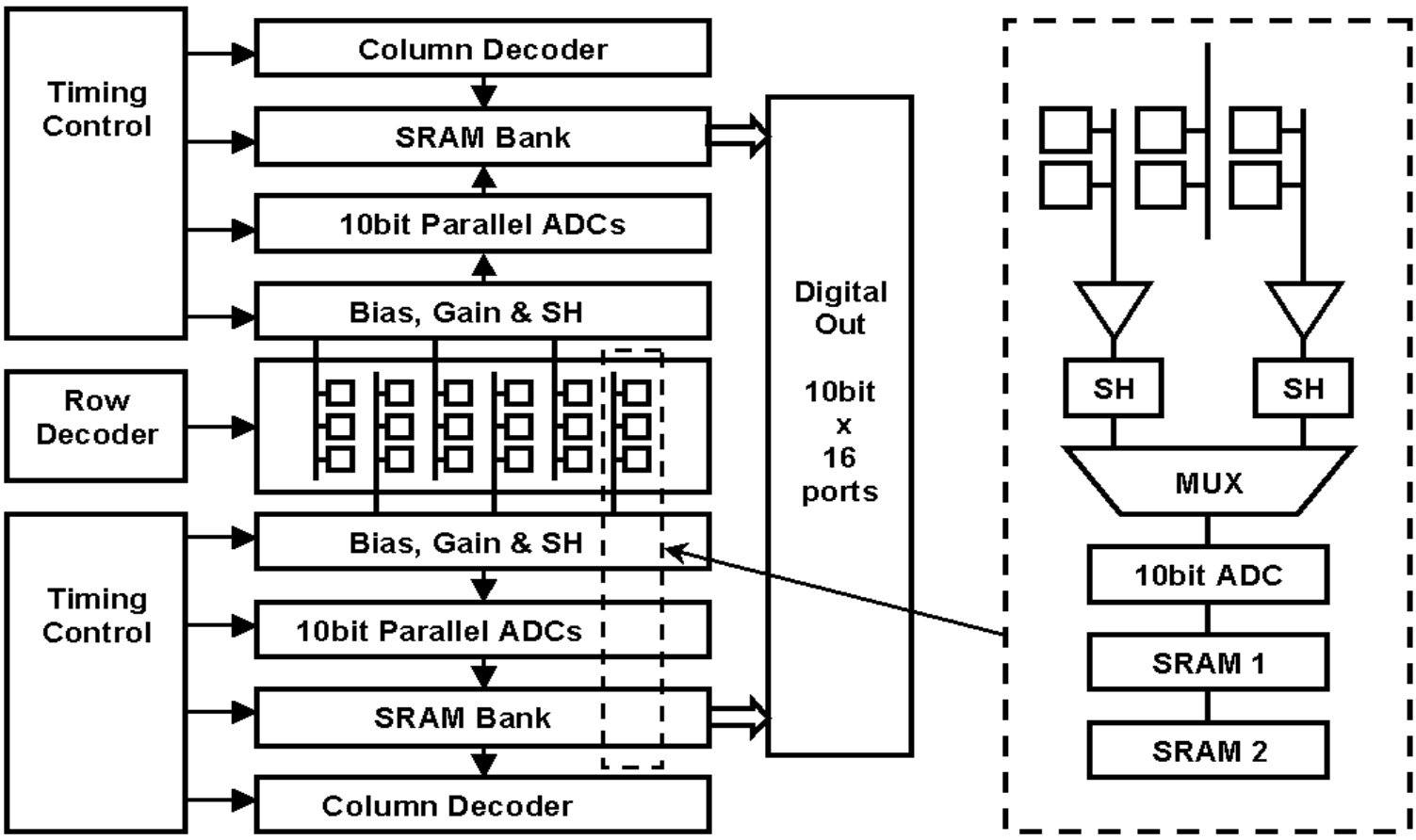

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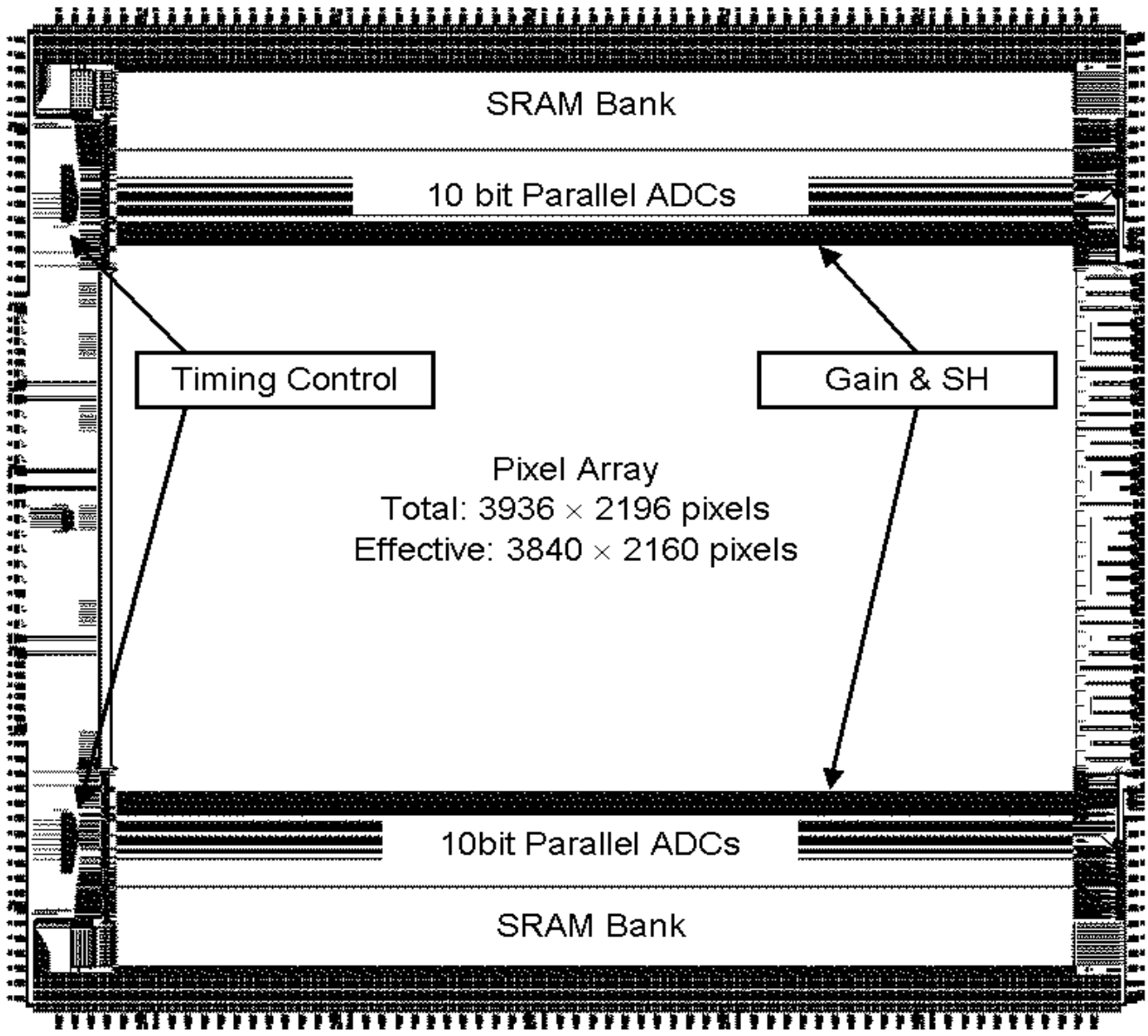

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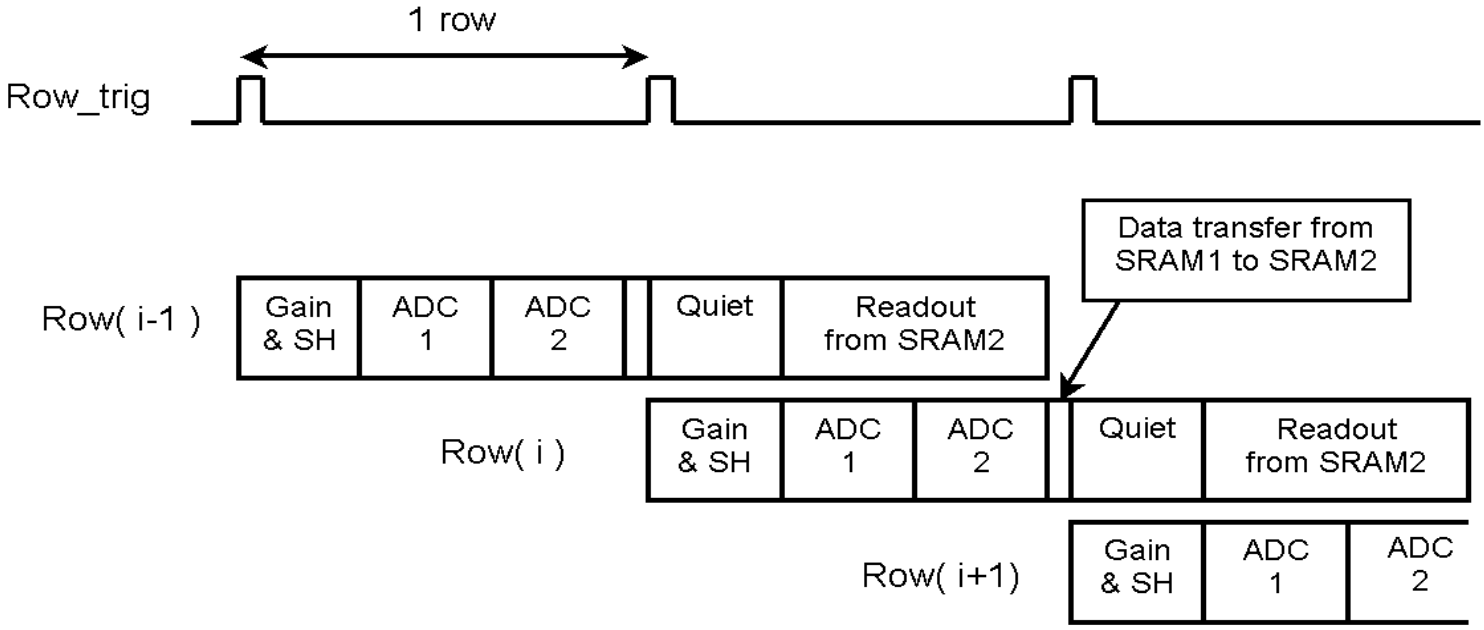

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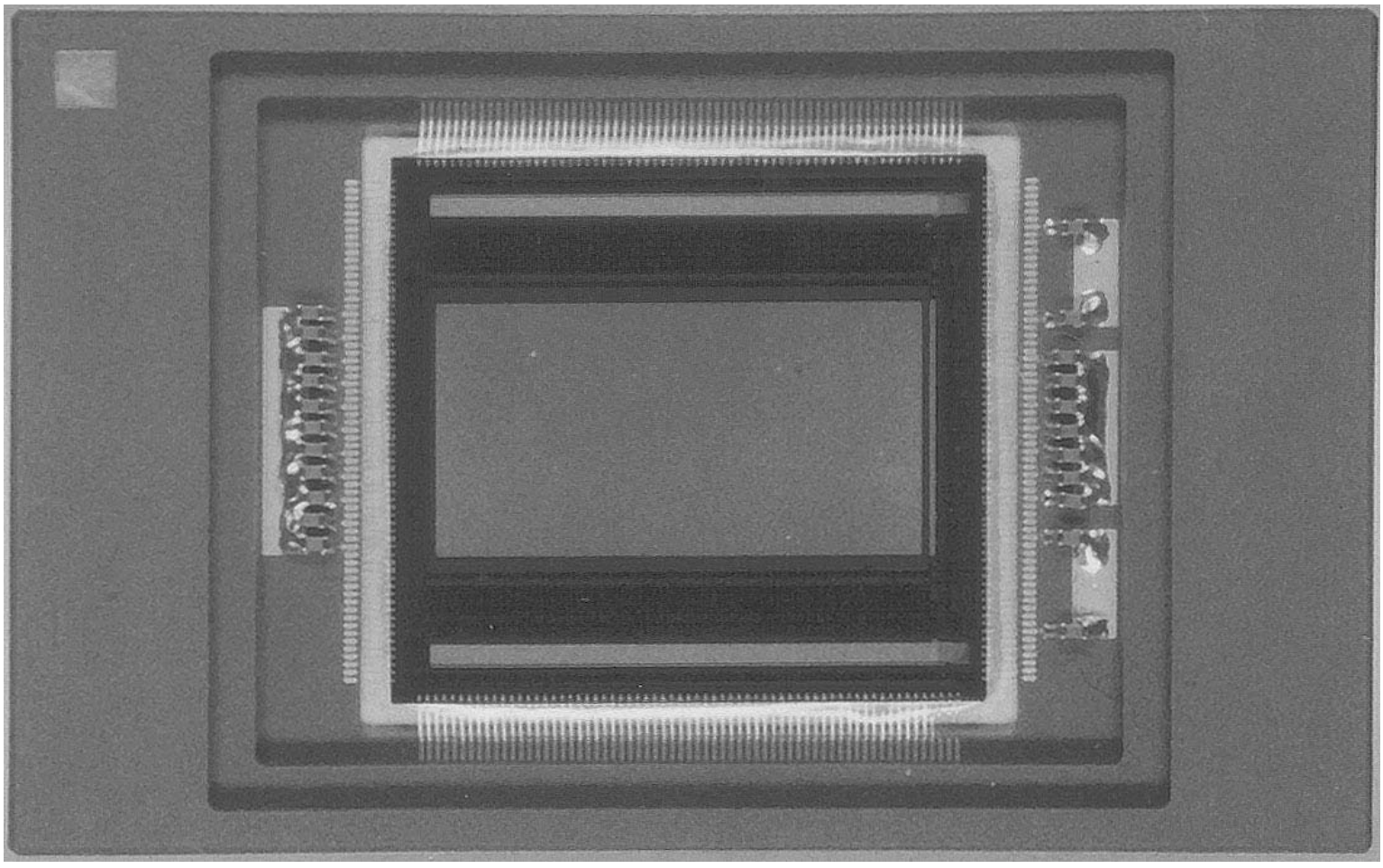

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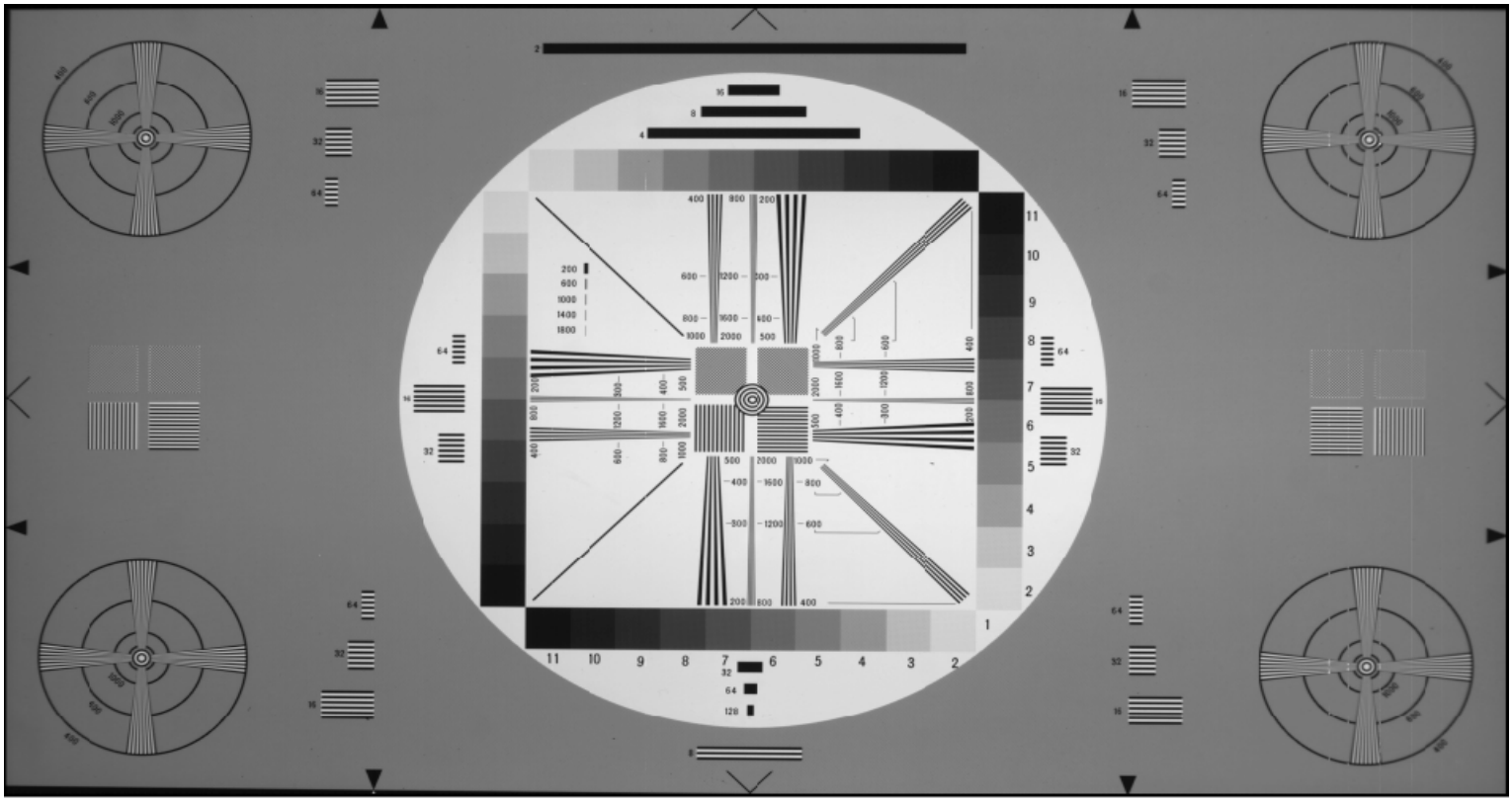

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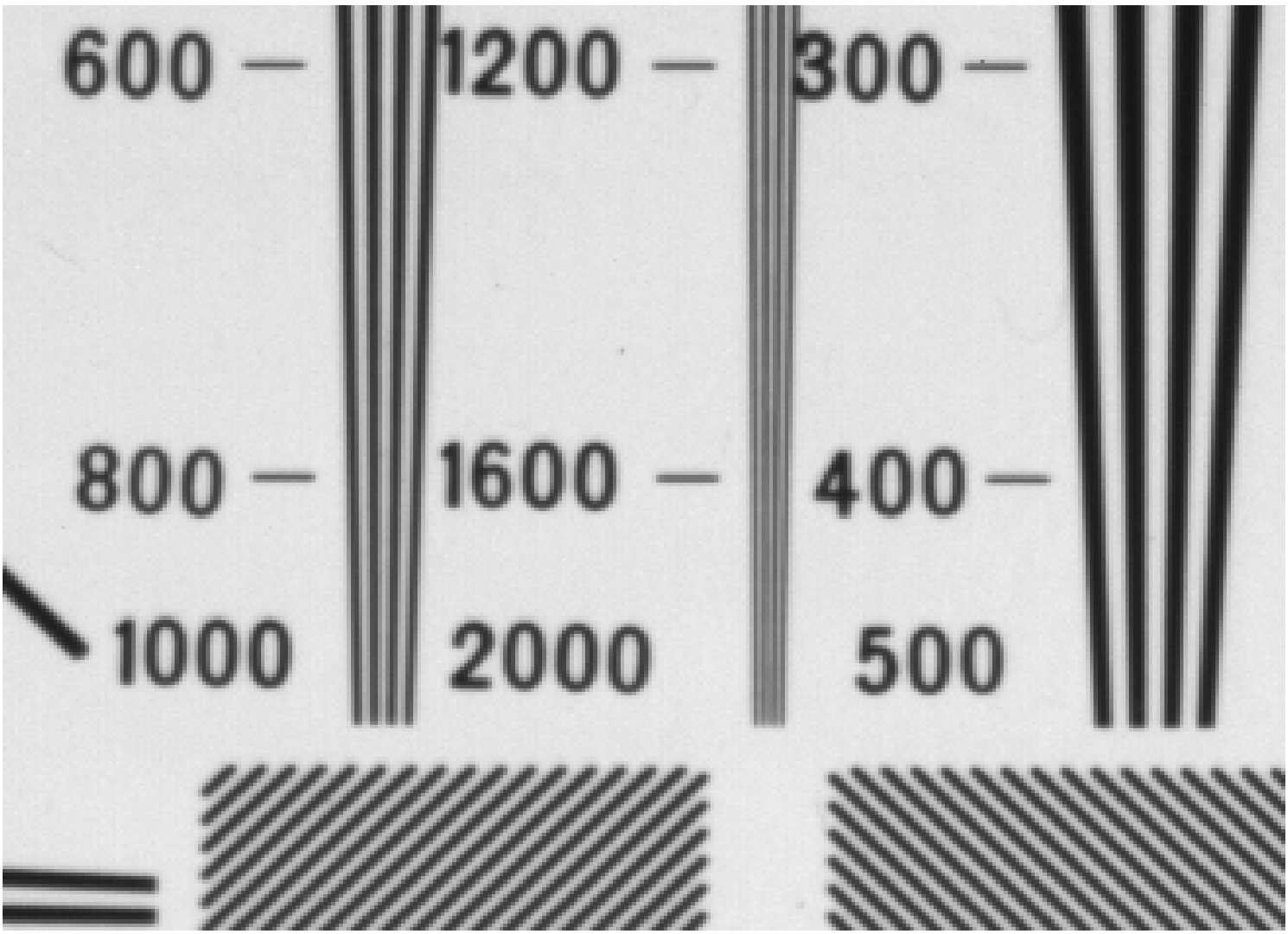

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