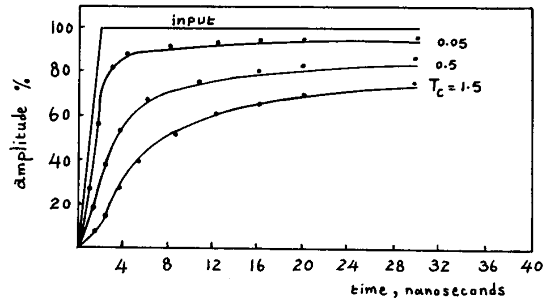

Fig. 4. Output waveforms for lines with different time constants T_c (in nanoseconds) for a 2-ns input ramp signal. ——: Calculated, [5]. •: Calculated, (8).

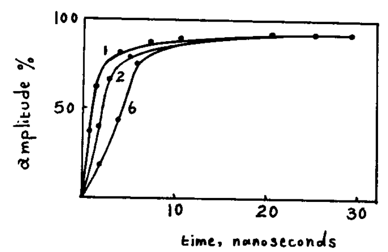

Fig. 5. Output waveforms for input ramps of 1, 2, and 6 ns for a line with a time constant $T_c = 0.1$ ns. ——: Calculated, [5]. •: Calculated, (8).

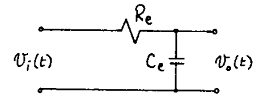

Fig. 6. Proposed equivalent circuit model for the RC transmission line of Fig. 1. $R_eC_e = \sigma\beta/\alpha$, $C_e = (\beta\lambda/\alpha)C$, and $R_e = \lambda R$.

From (5) it is obvious that the approximation proposed here to represent the transfer characteristic of the distributed RC transmission line of Fig. 1 corresponds to the equivalent circuit shown in Fig. 6. Such a simple equivalent circuit can be easily implemented for computer-aided analysis of the response of VLSI circuit interconnects to input signals with nonzero rise times.

III. Conclusions

In this correspondence a simple expression has been proposed for the transfer function of an infinitely long distributed RC transmission line. Using this expression a simple lumped network for modeling the distributed RC transmission line has been proposed. An excellent agreement, both qualitatively and quantitively, between predicted and previously calculated results proves that the approximations made in this correspondence are justifiable.

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A 1-GHz Charge-Packet Replicator/Subtractor Circuit for GaAs CCD Signal Processing

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***Abstract*—A novel charge-packet replicator/subtractor circuit based on GaAs charge-coupled device (CCD) technology is described. The circuit exhibits linear gain of 0.989 operating at 1-GHz replication frequency, while consuming only several milliwatts of dynamic power. Experimental results for a prototype circuit operating over the frequency range of 1 MHz to 1 GHz are presented.**

I. Introduction

GaAs charge-coupled devices (CCD's) have a demonstrated capability for high-throughput (0.1–4 GHz) sampled-analog signal processing in the charge domain [1]. Potenial applications include very-high-frequency adaptive filters, programmable correlators, fast-in/slow-out signal acquisition, and HDTV analog image processing [2]–[5]. Central to many of these operations is the need for an accurate and linear charge-packet sensing device. In addition, since many of the functions involve differential operations, an accurate method of subtracting analog signals in the charge domain is highly desirable. In this paper, we present a linear unity-gain charge-packet replicator/subtractor

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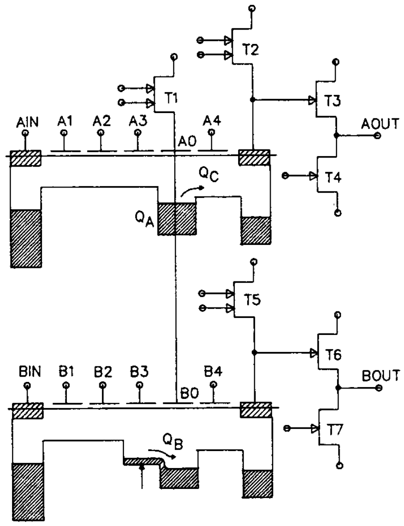

Fig. 1. Schematic diagram of charge-packet replicator/subtractor.

circuit based on GaAs CCD technology. Experimental results for a prototype circuit operated over a replication frequency range of 1 MHz to 1 GHz are discussed.

II. Circuit Description

Fundamentally, the replicator/subtractor outlined below operates on a charge balancing scheme. The ideal circuit may be viewed as two capacitors connected in series, in which the parasitic capacitance on the common node is assumed to be zero. In this case, addition of a negative signal charge to one side forces an equal quantity of negative charge away from the other, which, if collected, is a perfect replica of the signal charge packet. This ideal situation can be very nearly realized using GaAs CCD technology, largely because of the low parasitic capacitance offered by the GaAs semi-insulating substrate and nonoverlapping electrodes. Floating-gate charge sensing schemes have been widely used in Si CCD's for nondestructive signal summing and output amplification (see, for example, [6]). However, due to relatively large parasitic capacitances, charge-packet regeneration circuits have tended to be nonlinear or require additional amplification circuitry. Aside from being the first implementation of a charge-packet replication/subtraction circuit in GaAs technology, the circuit described below is also novel in that the low parasitic capacitance of the GaAs substrate is used to advantage in implementing a compact, near-unity-gain circuit which exhibits a high degree of linearity. Furthermore, the circuit is easily implemented in both applications requiring high-speed signal regeneration and those requiring charge-domain arithmetic, in which the results of the subtraction operation need to be available for further processing.

A schematic diagram of a prototype charge-packet replicator/subtractor is shown in Fig. 1. The circuit consists of two parallel CCD shift registers, capacitively coupled though the connection of gates A_0 and B_0, with FET T_1 used to reset the voltage on the common node. The source-follower output amplifiers with reset transistors (T_2–T_7) are strictly for characterization, and are otherwise unnecessary. Gates A_1–A_3 and B_1–B_3 generate the charge packets used in the replication/subtraction operation, though in a signal processor these operands would already exist. Gate A_4 isolates the common node from subsequent circuitry.

The operation of the circuit begins with the generation of charge packet Q_A, and its subsequent storage under gate A_0. FET T_1 is then cut off, allowing node A_0/B_0 to float. Barrier gate A_4 is dc biased at a level sufficient to confine Q_A, but more positive than the low (off) level used in clocking gates A_1–A_3. With Q_A stored and the common node floating, charge packet Q_B is then introduced under gate B_0. If parasitic capacitance is ignored, charge balancing occurs through redistribution of charge packet Q_A. Thus, an amount of charge Q_C equal to Q_B is forced over the barrier provided by gate A_4 and collected at the output amplifier. Note that if the capacitance to the substrate is assumed negligible, the voltage on barrier gate A_4 is not critical. In one clock cycle, Q_B is replicated and simultaneously subtracted from Q_A.

III. Gain Versus Speed

The effect of nonzero stray capacitance on circuit operation is a deviation from unity gain. In replication mode, where Q_A is fixed, the gain g remains linear; however, in subtraction mode the variation in capacitance due to the varying size of Q_A gives rise to a nonlinear gain coefficient. In general, $Q_C = g \cdot Q_B$, where the general form of the gain is

$$g = 1 - C_P / C_{A0}. \tag{1}$$

C_P is the parasitic capacitance on node A_0/B_0, and C_{A0} is the capacitance of gate A_0.

In the case of nonoverlapping-gate CCD's, as used in the prototype circuit described below, the dominant source of parasitic capacitance is due to the sidewall of the reset FET T_1 operating in cutoff. Using an expression given in [7] for the sidewall capacitance of a cutoff MESFET, it can be shown that

$$g = 1 - K_1 \cdot (W_{T1} / A_{A0}) \tag{2}$$

where

$$K_1 = [T' - Q_A/(qN_D)] \cdot \tan^{-1}\left[(V_{bi} - V_{TH})/(V_{TH} - V_{gs})\right]^{1/2} \tag{3}$$

W_{T1} is the width of FET T_1, A_{A0} is the area of gate A_0, T' is the effective thickness of the active layer, N_D is the doping, V_{bi} is the built-in potential of the Schottky gates, V_{gs} is the gate voltage on T_1, and V_{TH} is the threshold voltage. In subtraction mode, the maximum deviation from unity gain is obtained for Q_A equal to zero, and is typically 2 to 3 times the deviation in replication mode in which Q_A is set at the maximum charge packet size.

The constraint on possible values for W_{T1}, and hence achievable gain, results from consideration of the desired maximum frequency of operation. The reset FET (T_1) must be able to discharge a maximum-size charge packet from node A_0/B_0 in less than one half of a clock period. If a simple square-law approximation to the drain current of T_1 is assumed, this implies that

$$f_{\max} = K_2 \cdot (W_{T1} / A_{A0}) \tag{4}$$

where

$$K_2 = I'_{ds}/(2Q'_{\max}) = \beta'(V_{gs} - V_{TH})^2/(2qN_DT') \tag{5}$$

I'_{ds} is the drain current per unit gate length, $Q'_{\max}$ is the

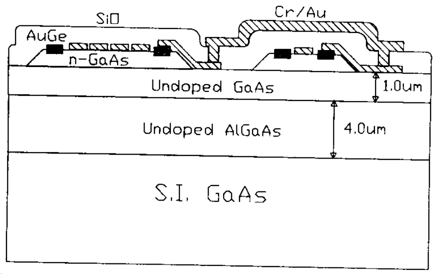

Fig. 2. Cross section of device structure used in prototype circuit. Notice that the same active layer is used for both CCD's and MESFET's.

maximum charge packet size per unit area, and β' is the transconductance parameter per unit gate length. Combining (2) and (4) gives

$$g = 1 - (K_1/K_2) \cdot f_{max}. \quad (6)$$

Thus, there is a direct trade-off between gain and the maximum operating frequency of the circuit. Note that increasing the gain also improves the linearity of the subtraction operation.

A second-order effect, which is ignored in the above analysis, is the variation in gain with the varying size of charge packet Q_B. When Q_B is replicated or subtracted, charge totaling $g \cdot Q_B$ is added to the capacitance of gate A_0, hence changing the common-node voltage $V_{A/B}$. The change in common-node voltage in turn changes the bias on the sidewall capacitance of T_1, as well as the bias of gate A_0. Therefore, the ratio C_P/C_{A0} changes dynamically during the replication/subtraction process and is sensitive to the input signal size. This second-order effect is expected to dominate the signal-to-noise properties of the circuit. In the following section, the error introduced by the constant gain assumption is computed by incrementally introducing charge packet Q_B and dynamically adjusting the C_P/C_{A0} ratio. The analysis is carried out over all input signal sizes to determine the maximum resulting error Q_n. The estimated signal-to-noise ratio (SNR) is then $20 \cdot \log(Q_{max}/Q_n)$.

IV. Experimental Results

The replicator/subtractor circuit shown in Fig. 1 has been fabricated and characterized over a wide range of frequencies. A device cross section is shown in Fig. 2. The circuit was fabricated on both MOCVD and MBE-grown active layers. Mesa isolation was used with Au-Ge alloyed ohmic contacts. Schottky gate metal is e-beam deposited Cr followed by thermally evaporated Au. E-beam evaporated SiO was used as the interlayer dielectric. A second level of metal (Cr-Au) is used for interconnects. The CCD gates are 100 μm wide by 2 μm long, separated by 1-μm gaps. FET gate lengths are 1 μm. The FET gate widths are 100 μm, except for the reset transistors, $T_1/T_2/T_5$, which are 25 μm wide. This CCD structure, with an appropriate active layer, exhibited a charge transfer efficiency (CTE) greater than 0.999 at 1 GHz [8]. As described below, the original and replica charge packets undergo the same number of transfers, thus no variation in performance with CTE was expected nor observed. The necessary area for the replicator/subtractor, which includes gates $A_0/B_0/A_4$ and FET T_1, is approximately 1500 μm^2.

Referring to Fig. 1, gates $B_1 - B_4$ are clocked respectively with phases $\phi_1 - \phi_4$, while gates $A_1 - A_3$ are clocked with phases $\phi_4 - \phi_2$. In this way charge packet Q_A arrives under electrode A_0 prior to charge packet Q_B arriving under electrode B_0. The size of charge packet Q_A is set by a dc bias on A_{IN}, and set so as to produce a full-well charge packet, Q_{max}, when characterizing the replicator. The barrier gate A_4 is dc biased and a signal generator is applied to input B_{IN}. Charge packets are set under gates A_2 and B_2 by injection, governed through the bias on A_{IN} and B_{IN}. The output amplifiers are biased identically as source followers.

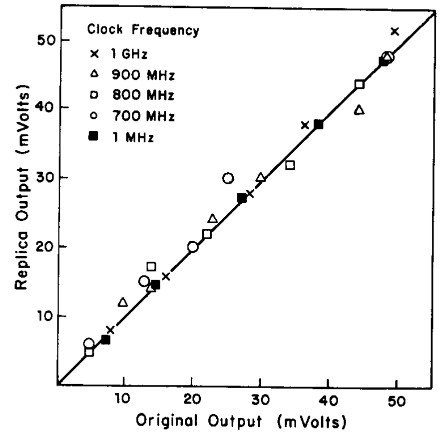

Fig. 3. Output due to an original charge packet, Q_B, versus output due to the replica charge packet, Q_C, over the frequency range 1 MHz to 1 GHz. The 1-MHz data are attenuated 20 dB.

Fig. 3 shows the T_6/T_7 output due to an original charge packet, Q_B, versus the T_3/T_4 output due to the generated replica charge packet, Q_C, for clock frequencies from 1 MHz to 1 GHz. The accuracy of the measurement is approximately ± 3 mV. Notice that within the experimental error the gain is linear and unity. Calculation using (2) and parameters based on Schottky $C-V$ and MESFET $I-V$ measurements estimate the experimental deviation from unity gain due to parasitic capacitance to be less than 1 mV.

Fig. 4 shows the calculated gain and operating speed trade-off versus design parameter W_{T1}/A_{A0} for two of the active layers used experimentally. In addition, for specified design points, the estimated SNR is also given. The dimensions of the CCD electrodes are generally dictated by the need for high-CTE operation, thus the width of reset gate T_1 is the critical parameter in determining the speed-gain trade-off for the replicator/subtractor. Note that an operating speed of 1 GHz, gain of 0.989, and SNR of 54 dB are possible using an active layer previously shown to be compatible with high-frequency, high-CTE GaAs CCD's [8]. Furthermore, it should be possible in many applications to operate the replicator/subtractor circuitry at some fraction of the clock rate in return for increased gain and linearity. At high clock frequencies, where the effects of leakage current are minimized, it was possible to vary the voltage on gate A_4 over a 4-V range without effecting the gain of replication.

V. Conclusions

A charge-packet replicator/subtractor circuit has been described and demonstrated at frequencies from 1 MHz to 1 GHz. Due to the low parasitic capacitance of the GaAs semi-insulating substrate, the gain is linear and nearly unity. The chip area required for the circuit consists of several CCD gates and a small MESFET. Based on $C-V$ measurements, the dynamic

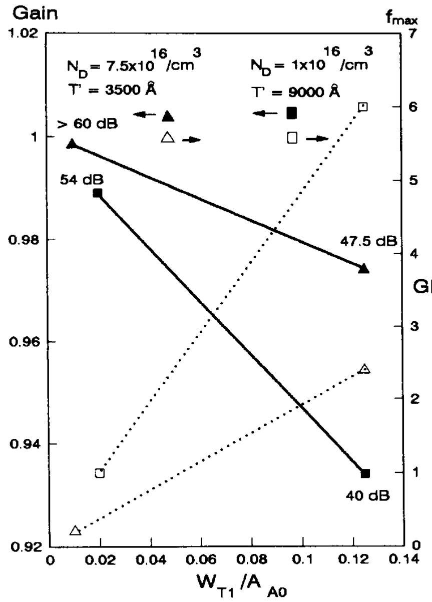

Fig. 4. Calculated gain and maximum operating frequency versus design parameter W_{T1}/A_{A0} for two different active layers. Also shown is the estimated SNR at four different design points. Calculations are outlined in Section III, and based on data from Schottky $C-V$ and MESFET $I-V$ measurements.

power consumed for the replication/subtraction process (operating with 5-V clock swings) is estimated to be on the order of several milliwatts at 1 GHz, where the operation takes place in 1 ns. Design constraints have been outlined and compared to experimental results in an effort to explore the trade-off between speed and gain. Furthermore, the circuit has been shown to be relatively insensitive to the precise voltages used during operation. In conclusion, the high performance and low consumption of real estate and power shown by this charge-domain replicator/subtractor make it a promising circuit for use in high-speed analog signal processors based on GaAs CCD technology.

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Frequency Limitations of a Conventional Phase–Frequency Detector

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Abstract —**The phase and frequency discriminator characteristics of a digital phase–frequency detector (DPFD) are analyzed in detail. Analytical expressions that correctly predict the high-frequency behavior of the circuit are derived. The results show excellent agreement with measurements and computer simulations.**

I. Introduction

Digital phase–frequency detectors (DPFD's) are commonly used to improve the pull-in range and the pull-in time of phase-locked loop (PLL) circuits and are especially suited to frequency-synthesis applications with periodic inputs. It is a well-known fact that a DPFD cannot tolerate missing transitions when used with random data [1]. However, a DPFD can still be used in clock-recovery applications when all the data transitions are present (e.g., with a training sequence during capture or after a low-Q LC filter). Although widely used, the exact frequency-discriminator characteristics of DPFD's are little known [2], [3]. In the following sections, the phase- and frequency-detector characteristics of typical sequential-type DPFD's will be analyzed in detail. The nonideal behavior of the digital circuitry due to gate delays will be shown to alter the DPFD phase- and frequency-discriminator characteristics significantly, thus limiting the maximum frequency of operation.

II. Low-Frequency Analysis

The DPFD circuit to be analyzed is a well-known circuit that can be implemented using either D-type master–slave flip-flops or $R-S$ latches as shown in Figs. 1 and 2, respectively. The outputs U and D will respond only to the positive-going edges of the inputs R and V. Therefore, the input duty cycles do not have any effect on the outputs. When the two frequencies are equal, one of the outputs has a duty cycle that is a function of the difference between the input transition times while the other output remains inactivated or low. The active output depends on the initial conditions. Hence, the time average of

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