

Chapter 23

The Invention and Development of CMOS Image Sensors

A Camera in Every Pocket

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23.1 Introduction

CMOS (complementary metal-oxide-semiconductor) image sensors (CIS) in 2022 are produced, tested, and sold at the rate of about 6 billion sensors per year. Assuming each goes into a camera, that translates to about 200 cameras per second. Most of these cameras wind up in smartphones since smartphones became the “killer application” for the technology. They are also widely used in nearly all other visible light sensor applications, such as in automobiles, medicine, security, webcams, body cams, and drones, and have also spawned social media giants and aided in social justice. All these picture or video-taking cameras use the active pixel sensor with intra-pixel charge transfer technology invented 30 years ago, around 1992 at the NASA Jet Propulsion Laboratory, to solve problems with Charge-Coupled-Device (CCD) cameras in interplanetary spacecraft cameras. However, that pivotal invention, like most inventions, stood on the shoulders of prior inventions, and has also been further improved and complemented by a host of other inventive technologies since then. In this paper, we will take a short swing through some of the key developments in the invention and development of present-day CMOS image sensors, as well discuss recent developments in photon-counting image sensors.

23.2 Underlying Technology

At the heart of every camera, where the conversion from light to electronic signal takes place, is the image sensor – an integrated circuit (Figure 23.1). The optics of the camera focus the light as an image on the pixel-array portion of the surface of the sensor, which also has its own optical structures [2]. The absorption of visible-light photons creates electron–hole pairs in the semiconductor. The quantum efficiency (QE) is the ratio of useful photoelectrons to incident photons and often ranges from 50 to 80%. The photoelectrons are collected by diffusion and drift into an electrostatic “potential well” created by selective semiconductor doping via ion implantation. Photoelectrons are integrated in this storage well during the exposure (Figure 23.2). The pinned photodiode structure, invented by Teranishi, was used in CCDs and now in CMOS image sensors [3, 4]. At the end of the exposure integration period, the charge-domain signal is then converted to voltage by transferring the charge to a sense capacitance in the pixel. The change in the charge on this capacitive sense node causes a change in voltage, thus converting the signal from charge domain to voltage domain (Figure 23.3).

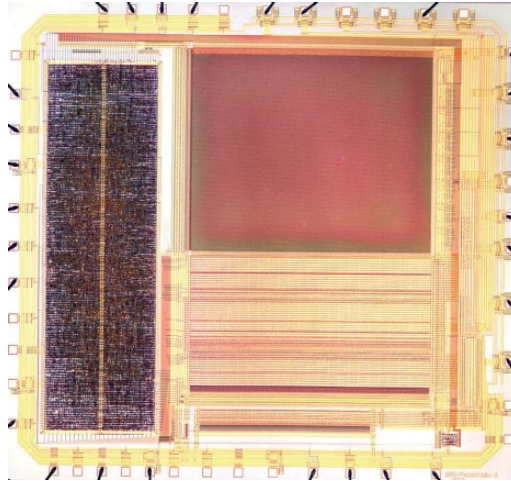


Figure 23.1 Early CMOS image sensor chip for webcams. Source: From [1] PHOTOBIT CORP. Left is digital logic for control and I/O. Top right is the pixel array. Bottom right are the column-parallel analog signal processing and analog-to-digital converter (ADC) circuits.

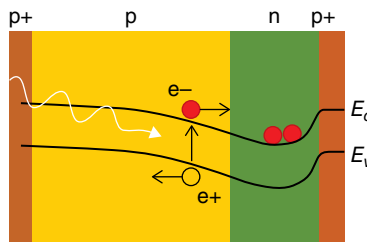


Figure 23.2 Photoelectrons are collected in an electrostatic storage well (N-region) created by selectively doping the silicon. In this case, photons enter the detector layer from the nominal substrate side, or backside, in so-called backside illumination (BSI) to increase pixel quantum efficiency.

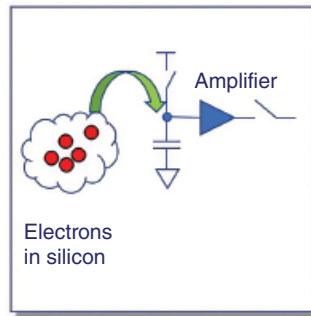


Figure 23.3 During readout of a CCD or CMOS image sensor, the signal charge is transferred onto a sense capacitance whose change in voltage is measured by an amplifier. For CDS, the amplifier voltage is sampled twice, once just before charge transfer, and once right after charge transfer, and then taking the difference to suppress reset noise and amplifier offset.

The change in voltage is usually buffered by a near-unity-gain source-follower metal-oxide-semiconductor field-effect transistor (MOSFET). This “floating diffusion amplifier” was first proposed by Kosonocky for a CCD and the signal may be further amplified by conventional electronics. The relationship between the change in output voltage and the number of photoelectrons is called the conversion gain (CG) with units of volts/electron. Typical CGs today are in the 30–75 $\mu\text{V}/e^-$ range.

Photon arrival rates are well-described by Poisson statistics, with a variance equal to the mean. Thus, repeated measurements of the same average photon flux will yield different results each time, and the standard deviation is referred to as photon shot noise. The signal-to-noise ratio (SNR) thus varies as the square root of the signal level, leading to low SNR at low signal levels. Thus, in low light, the signal often appears relatively more noisy (or “grainy”). The SNR can be improved by increasing the exposure time to increase the signal, but is limited according to the maximum number of photoelectrons that can be stored in the storage well (so-called “full well capacity” or FWC). An FWC of several thousand electrons is typical, leading to a maximum SNR of perhaps 50–70 or so.

Noise is also introduced by the readout process due to various noise sources in the readout circuit transistors and reset noise on capacitors. The use of correlated double sampling (CDS), invented by White [5], is one way to reduce reset noise and $1/f$ transistor noise. Correlated multiple sampling (CMS) may also be used. For larger signals, photon shot noise is the dominant noise. For low-light levels, the readout noise becomes critical in determining SNR. The readout noise is often referred to the equivalent number of input photoelectrons. For example, 150 μV rms of read noise with a CG of 50 $\mu\text{V}/e^-$ would be input-referred as 3 e^- rms. These days, the read noise of image sensors is typically in the 2–5 e^- rms range and is often dominated by residual $1/f$ noise from the first source-follower transistor.

23.3 Early Solid-State Image Sensors

In the 1960s, several groups pioneered building solid-state image sensors [6]. Weckler at Reticon realized that one could integrate photoelectrons on the built-in capacitance of a floating PN photodiode. This charge could then be readout by connecting the PN junction via a MOSFET switch to a readout circuit. This is now called a passive-pixel MOS image sensor. Noble at Plessey worked contemporaneously and built on Weckler’s idea and used a source-follower as a readout amplifier. Adding a switch to reset the photodiode and a switch to connect the source-follower to some additional readout sequencing circuits, Noble’s image sensor was the first three-transistor (3T) active pixel sensor. Unfortunately,

these early approaches yielded neither good nor stable image quality compared to image-pickup tubes due to limitations of the circuit configuration and semiconductor technology of the mid-1960s. Images suffered from large temporal noise and fixed-pattern noise. The circuit was susceptible to drifts in operating voltage and manufacturing yield. Reticon and Hitachi later continued to explore these passive pixel and 3T active pixel approaches but none achieved viable commercial success due, in part, to the above but also due to the invention and rapid development of CCDs.

In 1969, the CCD concept was invented by Boyle and Smith at Bell Labs as a solid-state equivalent to magnetic bubble memory. The CCD was based on the MOS gate structure using a series of adjacent gates. By pulsing each gate in sequence, minority carriers in the semiconductor (e.g. electrons) can be dragged along in the semiconductor due to electrostatic attraction [7]. The electron signal charge can either be electrically injected or created by light. In the former, the CCD acts like a delay line, and in the latter, the charge (or voltage) that is read out is indicative of the spatial distribution of light. When the CCD is configured as a 2D array of MOS gates, an image can be focused on the device, and the charge from that light pattern read out as a digital image (Figure 23.4). The first practical CCD image sensor was invented by Tompsett [8] and many significant improvements quickly followed.

The CCD was immune from many of the manufacturing issues that plagued the early passive and active pixel sensors, and efforts in the United States, Europe, and especially Japan rapidly developed the CCD into a workhorse image sensor [7]. The CCD image sensor became the basis for consumer camcorders from Japanese manufacturers and later broadcast TV cameras, and by the 1990s, digital still cameras.

Despite their success, CCD image sensors had many drawbacks due to the thousands of charge transfer steps required to readout each pixel in the image. The charge transfer requires considerable energy or power, especially in driving the higher voltage and higher capacitance multitude of transfer gates to achieve a desired charge transfer efficiency of at least 99.999%. Whenever the pixel count in the image sensor is increased, even more energy and power is required for readout. The intrinsic performance of the CCD also must improve since more transfer steps are required, and the charge transfer speed must increase for the same frame rate. CCDs were thus hard to scale to larger sizes. The cost of CCDs was fairly high because the manufacturing process to make a CCD was a very different recipe from that used by mainstream CMOS electronics (e.g. for computers and memory), and essentially every generation of CCD had to have a new and improved process whose development cost was amortized across the sale of those CCDs. All the drive and readout electronics had to be on additional chips and further increased power dissipation and camera form-factor. While highly dwarfed in volume by CMOS image sensors, CCDs still find niche (albeit shrinking) applications in some machine vision and scientific cameras.

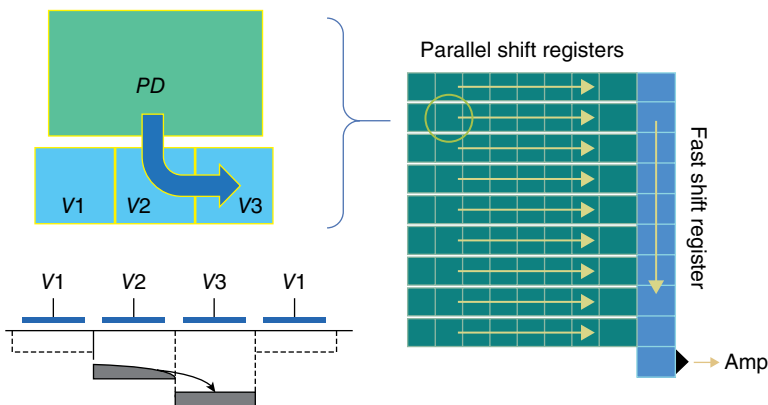


Figure 23.4 Illustration of a CCD interline transfer (ILT) pixel, top view (top left), charge-transfer shift register (bottom left), and a CCD ILT array (right).

23.4 Invention of CMOS Image Sensors

NASA had an additional problem with CCDs used in interplanetary spacecraft. Those CCD cameras were exposed to radiation in space that caused microscopic defects in the image sensor chip. The defects resulted in a continuous degradation in performance – both in charge transfer efficiency and dark current (like junction leakage current). Also, the power dissipation of CCD cameras was high – a problem when operating from a battery (CCD camcorder batteries were large, for example, and were depleted after perhaps 30 minutes of use) or a solar panel power supply or a radioisotope thermoelectric generator (RTG) aboard a spacecraft. Additionally, the electronics required to provide timing and clocking signals to drive the CCD, and to process the output signals including analog-to-digital conversion (ADC), were bulky and power-hungry.

In 1992, the author, working at the NASA Jet Propulsion Laboratory at Caltech, proposed a new approach for image sensors that would use an active pixel sensor with intra-pixel charge transfer, and use a mainstream CMOS microelectronics process flow as the baseline [9, 10] (see Figure 23.5). By using CMOS, one could not only capture the image, but one could also put all the timing and control circuits and all the signal processing circuits, including ADC, on the same chip. This would allow miniaturization of the spacecraft camera and reduce power consumption significantly (100×) as well as avoid many of the charge-transfer degradation issues associated with exposure to radiation in space [11] (see Figure 23.6).

Each pixel is composed of a tiny CCD with its own readout and selection electronics (see Figures 23.7 and 23.8). Using intra-pixel charge transfer allows the use of noise reduction techniques like CDS, thus enabling imaging performance comparable to CCDs. Incorporation of pinned photodiodes improved QE. By using CMOS as the baseline, the integration of additional signal processing and on-chip ADC to further improve performance of the active pixel sensor was also possible. A high-quality “camera-on-a-chip” became feasible. Both rolling shutter and global snapshot shutter implementations were conceived of in the early days, with rolling shutters yielding smaller, more competitive pixels. Global shutters have continued to improve and are desired when rolling shutter artifacts due to certain types of motion need to be suppressed [12].

The early sensors made in 1993–1995 showed great promise and it became clear that the technology was not only useful for space but also for consumers on planet Earth. However, the deeply entrenched CCD industry was very slow to recognize the advantages of the CMOS active pixel sensor camera-on-a-chip. US industry was similarly reluctant to engage with the new technology despite many attempts to evangelize and transfer the technology (with some notable exceptions). In 1995, the author and

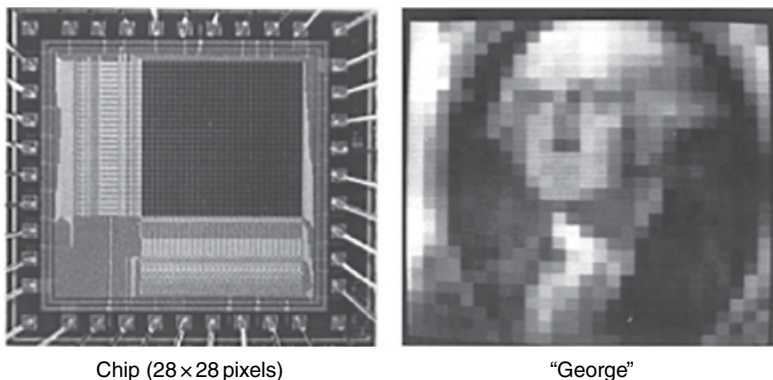


Figure 23.5 First CMOS image sensor chip and acquired 28×28 pixel image of a one-dollar bill from 1993 at NASA's JPL at Caltech. Source: Courtesy of Eric R. Fossum.

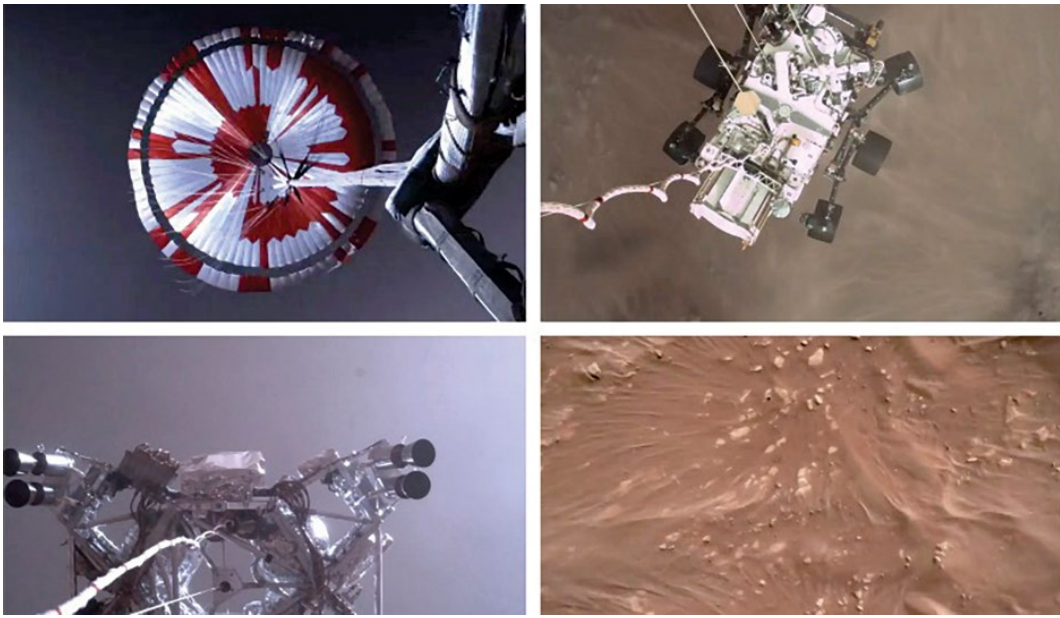


Figure 23.6 Video grabs of the Mars 2020 Perseverance rover landing. Perseverance has about 20 CMOS cameras on board including one on the Mars helicopter. Top left: Looking up at parachute. Bottom left: Looking up at “sky crane” descent vehicle. Top right: Looking down at the 1000 kg rover on the sky crane tether before landing: Bottom right: Mars surface just before landing. Source: NASA.

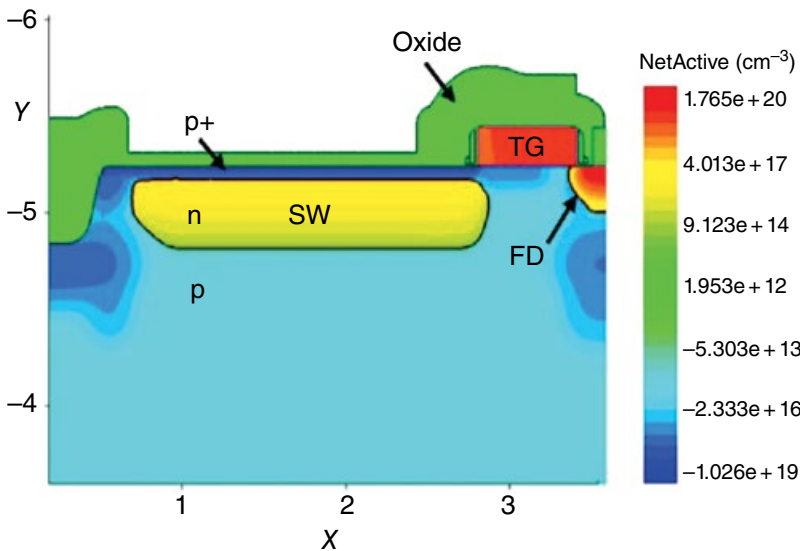


Figure 23.7 TCAD simulation of a pinned photodiode (PPD) charge storage region and transfer gate (TG) and sense node (FD). Source: From Fossum and Hondongwa [4]/IEEE.

several members of the team at JPL cofounded a spinoff company, Photobit, to commercialize the technology. Photobit grew to about 135 people before being acquired by Micron in 2001 and produced sensors for web cams, dental X-rays, swallowable pill cameras, high-speed machine vision systems, automotive rain wiper and high beam control, drowsy driver warning, star trackers, and other applications.

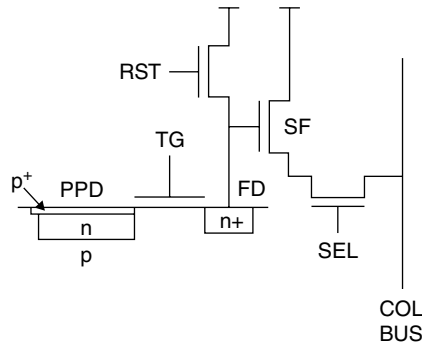


Figure 23.8 Circuit schematic of CMOS image sensor pixel including reset gate (RST), source-follower (SF), and row select switch (SEL). Source: From Fossum and Hondongwa [4]/IEEE.

By 2001, the “killer-app” of cellphone cameras was very visible on the horizon and Micron became a world leader in this technology [11].

Around the same time, some other large companies such as Sony and Samsung started to make large capital investments and seriously develop CMOS image sensors. Today, these two vertically integrated companies dominate the image sensor market place. Foundries like TSMC, X-Fab, and Tower-Jazz are also playing a major role for fabless companies. Micron later spun-off the image sensor business as Aptina, and later Aptina was acquired by ON-Semi (which grew out of Motorola).

In 2023, it is estimated that over 6.5 billion image sensors (or the same number of cameras) will be shipped worldwide corresponding to a semiconductor component revenue of \$19.3B [13] as shown in Figure 23.9. While nearly all of these CMOS image sensors still utilize active pixels with intra-pixel charge transfer, many improvements have been made since the 1992 invention. The use of 3-D stacked structures and back-side illumination (BSI) with deep-trench isolation (DTI) has resulted in significantly improved performance and capability [14–16]. Shared readout [4] results in pixel pitch reduction, as well as a plummeting cost per pixel. Older CCD “VGA” sensors with 0.3 megapixels once cost about US\$100 in the mid-1990s. Today, a VGA CMOS image sensor might cost more than 200× less or US\$0.50.

CMOS image sensors today are ubiquitous, and several image sensors are typically found in every smartphone (e.g. front selfie camera and one or more rear-facing cameras) which in turn enabled

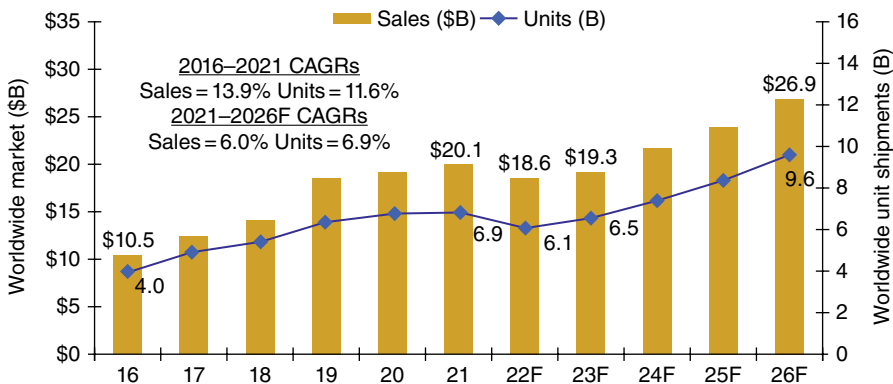


Figure 23.9 CMOS image sensor sales growth according to IC Insights. Source: Adapted from [13]. The Covid-19 pandemic and semiconductor supply chain issues cause a downward forecast for 2021–2023 with growth expected to recover after that.



Figure 23.10 2017 Queen Elizabeth Prize for Engineering presentation at Buckingham Palace. (L-R, HRH then-Prince-now King Charles III, Fossom, Tompsett, Teranishi). Source: Queen Elizabeth Prize for Engineering Foundation.

industry giants like Facebook, Instagram, Tiktok, and YouTube. They are also used in nearly every other camera application from automobiles to swallowable pill cameras to smart doorbells to police bodycams. While CCD unit volume was always small compared to today's CMOS image sensor unit volume, CCD manufacturing has come to an end for most applications.

In 2017, the importance of digital image sensors in everyday life was recognized through the awarding of the Queen Elizabeth Prize for Engineering to Smith and Tompsett (CCD image sensors), Teranishi (pinned photodiode), and Fossom (CMOS image sensor) (Figure 23.10).

23.5 Photon-Counting CMOS Image Sensors

In 2005, a different approach for image sensors was proposed [17]. In this proposed device, single photons would be detected and counted by a large number of specialized yet tiny pixels (called jots) operating at a high frame rate. Detection would be essentially binary, either 0 for no photon, or 1 for a photon. Frames of binary data could be used to recreate a gray-scale image, and image in the dimmest possible light. First called a digital film sensor, the concept was later renamed a Quanta Image Sensor (QIS) and extended to multi-bit operation [18].

Other groups began to demonstrate the QIS concept and prove the imaging characteristics model using single photon avalanche detector (SPAD) arrays. SPAD devices have been in development for about 26 years with recent rapid progress [19]. In 2021, a 3.2 Mpixel SPAD array was reported for the first time with a 6.4 μm pixel pitch [20]. Since the SPAD relies on avalanche multiplication for signal gain, it requires high internal electric fields and relatively large spacing between pixels to ensure isolation, and they may also typically have high dark count rates (dark current). Despite these issues, SPADs have been proven very useful for fast photon arrival timing applications such as 3-D imaging.

In 2012, work on realizing a CMOS QIS began at the Thayer School of Engineering at Dartmouth. Instead of using avalanche gain to detect single photoelectrons, the gain comes from using a very

small sense node capacitance yielding CG in the range of $300\text{--}500\mu\text{V}/e^-$. Using intra-pixel charge transfer, a single electron transferred to that capacitance can produce a discernible signal that is well above the noise floor (e.g. $0.2e^-$ rms noise floor) and thus give a low error rate for detection of single photoelectrons. The detection process is slower than for SPADs, but sub-microsecond timing is achievable. Further, avoiding the high electric fields of SPADs enables smaller pixels or jots, improved manufacturability, and thus lower cost per pixel and smaller optics. Power dissipation is also considerably smaller. In 2017, Dartmouth reported a room-temperature 1 Mpixel QIS device implemented in a nearly standard BSI CIS 3D stacked process with $1.1\mu\text{m}$ pixel pitch, operating at 1000 fps and dissipating about 20 mW total power [21] (see Figures 23.11–23.13). The 1 Mpixel QIS was demonstrated more than two years earlier than the first 1 Mpixel SPAD array and with much less development time and with much smaller pixels. About 34 CMOS QIS $1.1\mu\text{m}$ pixels can fit into the area of one SPAD $6.4\mu\text{m}$ pixel. This is the strength of working in a nearly standard CIS processes. SPAD technology has also been exploiting technologies used for CIS such as 3-D stacking and low dark current



Figure 23.11 QIS test chip containing 20 different 1 Mpixel arrays designed by Dartmouth and fabricated by TSMC in a 65 nm stacked BSI CIS process. Source: Eric R. Fossum.

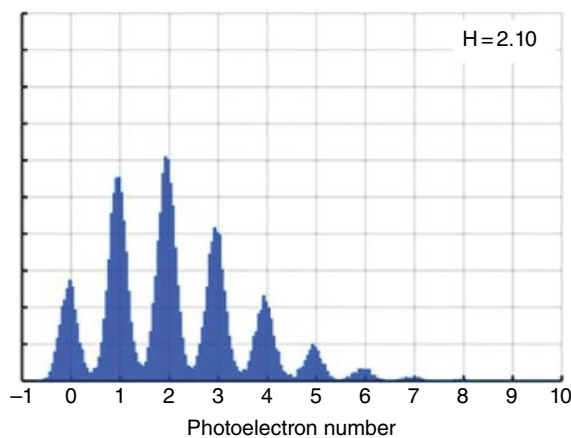


Figure 23.12 Photon-counting histogram (# occurrences vs. normalized readout voltage) showing clear quantization of photoelectrons. The peak heights correspond to the Poisson distribution for an average photoelectron arrival rate of $2.1e^-/\text{sample}$.

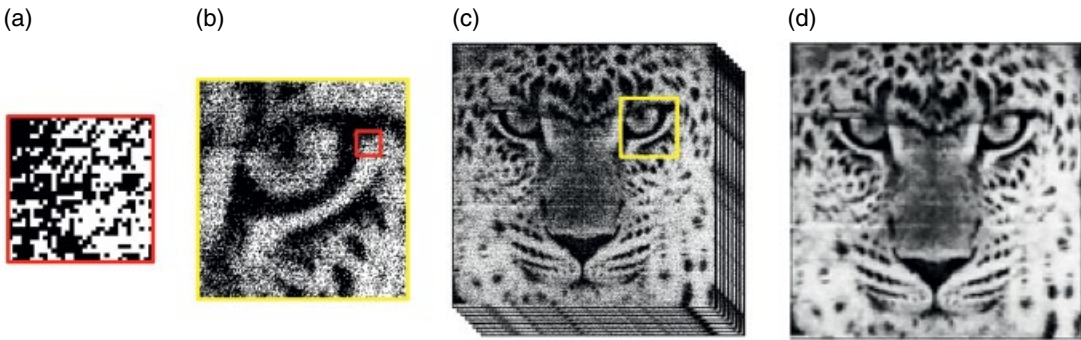


Figure 23.13 Data taken from a 1 Mpixel array on the QIS test chip. (a) Close-up of binary image data in one frame, (b) zoomed out version of (a), (c) further zoomed out and illustrating multiple binary frames that are combined to achieve the gray scale image in (d). Source: Optical Society of America.

structures. Both CMOS-image-sensor QIS technology and SPAD-QIS technology occupy important application areas [22].

Recently, CMOS image sensors that use QIS photon-counting technology have achieved 163 Mpixels in resolution and high dynamic range [23, 24]. The applications of QIS technology are currently being explored but include low-light imaging for security, defense, science, and possibly consumer devices.

23.6 Conclusion

CMOS image sensors continue to be used in an ever-increasing variety of applications. Some of these applications are useful in everyday life, some are for fun (photography, social media), some are for safety, and some continue to test the age-old balance between security and privacy. After 30 years, the future still looks bright for CMOS image sensors.

Acknowledgments

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References

- [1] (2022). <https://spectrum.ieee.org/chip-hall-of-fame-photobit-pb100>.
- [2] Teranishi, N., Watanabe, H., Ueda, T., and Sengoku, N. (2012). Evolution of optical structure in image sensors. *2012 International Electron Devices Meeting*, San Francisco, CA (10–13 December 2012), pp. 24.1.1–24.1.4. IEEE. <https://doi.org/10.1109/IEDM.2012.6479092>.
- [3] Teranishi, N., Kohono, A., Ishihara, Y. et al. (1982). No image lag photodiode structure in the interline CCD image sensor. *International Electron Devices Meeting*, San Francisco, CA (13–15 December 1982), pp. 324–327. IEEE. <https://doi.org/10.1109/IEDM.1982.190285>.
- [4] Fossum, E.R. and Hondongwa, D.B. (2014). A review of the pinned photodiode for CCD and CMOS image sensors. *IEEE Journal of the Electron Devices Society* 2 (3): 33–43. <https://doi.org/10.1109/JEDS.2014.2306412>.

- [5] White, M.H., Lampe, D.R., Mack, I.A., and Blaha, F.C. (1973). Characterization of charge-coupled device line and area-array imaging at low light levels. *Digest of Technical Papers – IEEE International Solid-State Circuits Conference* 16: <https://doi.org/10.1109/ISSCC.1973.1155159>.
- [6] Fossum, E.R. (1997). CMOS image sensors: electronic camera-on-a-chip. *IEEE Transactions on Electron Devices* 44 (10): 1689–1698. <https://doi.org/10.1109/16.628824>.
- [7] Theuwissen, A.J.P. (1995). *Solid-State Imaging with Charge-Coupled Devices*. Kluwer Academic Publishers. ISBN: ISBN 0-792-33456-6.
- [8] Tompsett, M.F. (1978). Charge transfer imaging devices. US Patent No. 4,085,456, issued 1978.
- [9] Fossum, E.R., Mendis, S., and Kemeny, S.E. (1995). Active pixel sensor with intra-pixel charge transfer. US Patent No. 5,471,515 issued 1995.
- [10] Fossum, E.R. (1993). Active pixel sensors: are CCDs dinosaurs? *Proc. SPIE 1900, Charge-Coupled Devices and Solid State Optical Sensors III*, San Jose, CA (12 July 1993). SPIE. <https://doi.org/10.1117/12.148585>.
- [11] Fossum, E.R. (2013). Camera-on-a-chip: technology transfer from saturn to your cell phone. *Technology and Innovation* 15 (3): 197–209. <https://doi.org/10.3727/194982413X13790020921744>.
- [12] Velichko, S. (2022). Overview of CMOS global shutter pixels. *IEEE Transactions on Electron Devices* 69 (6): 2806–2814. <https://doi.org/10.1109/TED.2021.3136148>.
- [13] (2022). <https://www.icinsights.com/news/bulletins/CMOS-Image-Sensors-Stall-In-Perfect-Storm-Of-2022/>.
- [14] Fontaine, R. (2019). The state-of-the-art of smartphone imagers. *Proc. 2019 Int. Image Sensor Workshop, Snowbird, Utah (23–27 June 2019)*. www.imagesensors.org.
- [15] Oike, Y. (2022). Evolution of image sensor architectures with stacked device technologies. *IEEE Transactions on Electron Devices* 69 (6): 2757–2765. <https://doi.org/10.1109/TED.2021.3097983>.
- [16] Wu, S.G., Chen, H.-L., Chien, H.-C. et al. (2022). A review of 3-dimensional wafer level stacked back-side illuminated CMOS image sensor process technologies. *IEEE Transactions on Electron Devices* 69 (6): 2766–2778. <https://doi.org/10.1109/TED.2022.3152977>.
- [17] Fossum, E.R. (2005). What to do with sub-diffraction-limit (SDL) pixels? – a proposal for a gigapixel digital film sensor (DFS). *Proceedings of the 2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Karuizawa (9–11 June 2005). IEEE. www.imagesensors.org.
- [18] Fossum, E.R., Ma, J., Masoodian, S. et al. (2016). The quanta image sensor: every photon counts. *Sensors* 16: 1260. <https://doi.org/10.3390/s16081260>.
- [19] Gyongy, I., Dutton, N.A.W., and Henderson, R.K. (2022). Direct time-of-flight single-photon imaging. *IEEE Transactions on Electron Devices* 69 (6): 2794–2805. <https://doi.org/10.1109/TED.2021.3131430>.
- [20] Morimoto, K., Iwata, J., Shinohara, M. et al. (2021). 3.2 megapixel 3D-stacked charge focusing SPAD for low-light imaging and depth sensing. *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA (11–16 December 2021), pp. 20.2.1–20.2.4. IEEE. <https://doi.org/10.1109/IEDM19574.2021.9720605>.
- [21] Ma, J., Masoodian, S., Starkey, D.A., and Fossum, E.R. (2017). Photon-number-resolving megapixel image sensor at room temperature without avalanche gain. *Optica* 4: 1474–1481. <https://doi.org/10.1364/OPTICA.4.001474>.
- [22] Ma, J., Chan, S., and Fossum, E.R. (2022). Review of quanta image sensors for ultralow-light imaging. *IEEE Transactions on Electron Devices* 69 (6): 2824–2839. <https://doi.org/10.1109/TED.2022.3166716>.
- [23] Ma, J., Zhang, D., Elgendy, O., and Masoodian, S. (2021). A photon-counting 4Mpixel stacked BSI quanta image sensor with 0.3e⁻ read noise and 100dB single-exposure dynamic range. *2021 Symposium on VLSI Circuits*, Kyoto (13–19 June 2021), pp. 1–2. IEEE. <https://doi.org/10.23919/VLSICircuits52068.2021.9492410>.
- [24] Ma, J., Zhang, D., Robledo, D. et al. (2022). Ultra-high-resolution quanta image sensor with reliable photon-number-resolving and high dynamic range capabilities. *Scientific Reports* 12 (1): 1–9. <https://doi.org/10.1038/s41598-022-17952-z>.